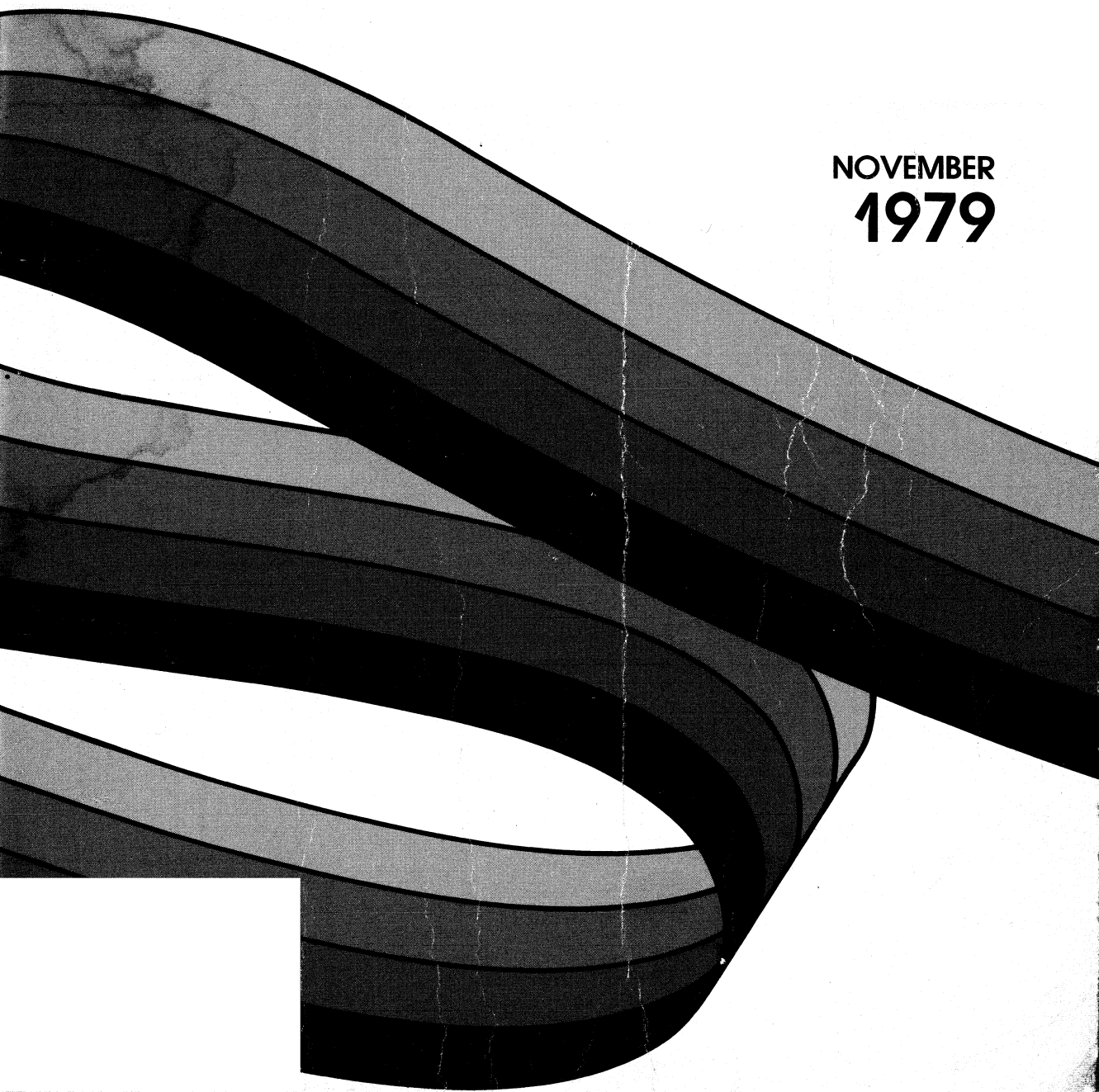




# FET Design Catalog

NOVEMBER  
1979







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### PARTS NOT READILY AVAILABLE IN EUROPE

The following device types are classified as *specials* (non-preferred parts). These devices are not readily available through European Sales Outlets. For further details and availability contact the Siliconix Sales Office or Franchised Distributor nearest you.

|                  |                  |        |
|------------------|------------------|--------|
| 2N 3368/69/70    | J230/31/32       | PN4416 |
| 2N3684/85/86/87  | K114-18          | PN5163 |
| 2N3909           | K1837-18         | U1837  |
| 2N4867A/68A/69A  | K210/11/12 (-18) | U1994  |
| 2N5078           | KK4416-18        |        |
| 2N5515-24        | MFE823           |        |
| 2N5555           | MPF102           |        |
| 2N5556/57/58     | MPF108           |        |
| 2N5653/54        | MPF109           |        |
| 2N5669/70        | MPF111           |        |
| JAN/JANTX Series | MPF112           |        |

### EUROPEAN HI-REL PARTS

The Following Devices Have Been Approved to BS CECC European Standards:

| Type Number      | BS CECC Specification                    |
|------------------|--|
| 2N3970/1/2       | BS CECC 50 012-001 (ISSUE 1, JUNE 1978)  |
| 2N4091/2/3       | BS CECC 50 012-002 (ISSUE 1, JUNE 1978)  |
| 2N4391/2/3       | BS CECC 50 012-004 (ISSUE 1, APRIL 1978) |
| 2N4856/7/8       | BS CECC 50 012-005 (ISSUE 1, JUNE 1978)  |
| 2N4859/60/61     | BS CECC 50 012-005 (ISSUE 1, JUNE 1978)  |
| 2N4856A/7A/8A    | BS CECC 50 012-006 (ISSUE 1, JUNE 1978)  |
| 2N 4859A/60A/61A | BS CECC 50 012-006 (ISSUE 1, JUNE 1978)  |

For Details on Other Products Submitted for Approval, Contact Your Nearest Siliconix Sales Office or Franchised Distributor.

## **FET Design Catalog**

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## how to use the FET Cross Reference and Index

*The following examples illustrate how the FET Cross Reference and Index should be used:*

**Case (1)** Recommended replacement offered by Siliconix is identical to Industry Part Number.

| Industry Part Number | Type and Classification | Recommended Replacement |
|----------------------|-------------------------|-------------------------|
| 2N3458               | N JFET                  | 2N3458                  |

**Case (2)** Recommended replacement offered by Siliconix is not identical to Industry Part Number.

| Industry Part Number | Type and Classification | Recommended Replacement |
|----------------------|-------------------------|-------------------------|
| 2N3457               | N JFET                  | 2N4338                  |

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison. Refer to appropriate page number listed under Data Sheet or Geometry column.

Type and classification abbreviations are described as follows:

|                                     |                                  |
|-------------------------------------|----------------------------------|
| CR (Current Limiter)                | JPAD (Plastic Pico Ampere Diode) |
| D (Dual)                            | N (N-Channel)                    |
| DPAD (Dual Pico Ampere Diode)       | P (P-Channel)                    |
| ENH (Enhancement-Mode Normally-Off) | PAD (Pico Ampere Diode)          |
| G (Gate)                            | VMOS (Vertical MOSFET)           |

# FET Cross Reference and Index



| Industry Part Number | Type and Classification | Recommended Replacement | Date Sheet Page | Geometry Page | Industry Part Number | Type and Classification | Recommended Replacement | Date Sheet Page | Geometry Page |
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| 2N5257               | N JFET                  | 2N5457                  |                 |               | 2N5562               | D N JFET                | U402                    |                 |               |
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| 2N5396               | N JFET                  | 2N4869A                 |                 |               | 2N5799               | P JFET                  | 2N2608                  |                 |               |
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| 2N6483               | D N JFET                | U401                    |                 |               | 204S                 | N JFET                  | 2N3821                  |                 |               |
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| 104M                 | N JFET                  | 2N5458                  |                 |               | 1325A                | N JFET                  | 2N4222                  |                 |               |
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| 2136U                | D N JFET                | 2N3957                  |                 |               | BFW54                | N JFET                  | 2N3822                  |                 |               |
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| 2139U                | D N JFET                | 2N3958                  |                 |               | BFW56                | N JFET                  | 2N4869                  |                 |               |
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| 2148U                | D N JFET                | 2N3958                  |                 |               | BSV22                | N JFET                  | 2N4416                  |                 |               |
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| A5T3822              | N JFET                  | K305-18                 |                 |               | C413N                | N JFET                  | 2N5434                  |                 |               |
| A5T3823              | N JFET                  | KK4416-18               |                 |               | C673                 | N JFET                  | 2N4341                  |                 |               |
| A5T3824              | N JFET                  | J302-18                 |                 |               | C674                 | N JFET                  | 2N4341                  |                 |               |
| A192                 | N JFET                  | 2N4416                  |                 |               | C680                 | N JFET                  | 2N4338                  |                 |               |
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| AD831                | D N JFET                | U421                    |                 |               | C681                 | N JFET                  | 2N4338                  |                 |               |
| AD832                | D N JFET                | U422                    |                 |               | C681A                | N JFET                  | 2N4338                  |                 |               |
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| AD833A               | D N JFET                | U423                    |                 |               | C682A                | N JFET                  | 2N4339                  |                 |               |
| AD835                | D N JFET                | 2N3921                  |                 |               | C683                 | N JFET                  | 2N4339                  |                 |               |
| AD836                | D N JFET                | 2N3921                  |                 |               | C683A                | N JFET                  | 2N4339                  |                 |               |
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| AD839                | D N JFET                | 2N4085                  |                 |               | C685                 | N JFET                  | 2N4220                  |                 |               |
| AD840                | D N JFET                | 2N5196                  |                 |               | C685A                | N JFET                  | 2N4220                  |                 |               |
| AD841                | D N JFET                | 2N5197                  |                 |               | C6690                | N JFET                  | 2N3458                  |                 |               |
| AD842                | D N JFET                | 2N5199                  |                 |               | C6691                | N JFET                  | 2N3458                  |                 |               |
| AD3954               | D N JFET                | 2N3954                  |                 |               | C6692                | N JFET                  | 2N3459                  |                 |               |
| AD3954A              | D N JFET                | 2N3954A                 |                 |               | CM600                | N JFET                  | 2N4092                  |                 |               |
| AD3955               | D N JFET                | 2N3955                  |                 |               | CM601                | N JFET                  | 2N4091                  |                 |               |
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| AD3957               | D N JFET                | 2N3957                  |                 |               | CM603                | N JFET                  | 2N4091                  |                 |               |
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| BC264B               | N JFET                  | 2N4304                  |                 |               | CM643                | N JFET                  | 2N4092                  |                 |               |
| BC264C               | N JFET                  | 2N4304                  |                 |               | CM644                | N JFET                  | 2N4092                  |                 |               |
| BC264D               | N JFET                  | KK4416-18               |                 |               | CM645                | N JFET                  | 2N4092                  |                 |               |
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| BFS67                | N JFET                  | 2N3821                  |                 |               | CM651                | N JFET                  | 2N5433                  |                 |               |
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| DPAD2  | D PAD N JFET            | DPAD2                   | 3-48            |               | E421                 | D N JFET                | U441                    |                 |               |
| DPAD5  | D PAD N JFET            | DPAD5                   | 3-48            |               | E430                 | D N JFET                | U430                    |                 |               |
|  |                         |                         |                 |               | E431                 | D N JFET                | U431                    |                 |               |
| DPAD10   | D PAD N JFET            | DPAD10                  | 3-48            |               | E500                 | CL N JFET               | J500                    |                 |               |
| DPAD20   | D PAD N JFET            | DPAD20                  | 3-48            |               | E501                 | CL N JFET               | J501                    |                 |               |
| DPAD50   | D PAD N JFET            | DPAD50                  | 3-48            |               | E502                 | CL N JFET               | J502                    |                 |               |
| DPAD100  | D PAD N JFET            | DPAD100                 | 3-48            |               | E503                 | CL N JFET               | J503                    |                 |               |
| DU4339   | D N JFET                | U235                    |                 |               | E504                 | CL N JFET               | J504                    |                 |               |
| DU4340   | D N JFET                | U235                    |                 |               | E505                 | CL N JFET               | J505                    |                 |               |
| E100   | N JFET                  | J203-18                 |                 |               | E506                 | CL N JFET               | J506                    |                 |               |
| E101   | N JFET                  | J201-18                 |                 |               | E507                 | CL N JFET               | J507                    |                 |               |
| E102   | N JFET                  | J202-18                 |                 |               | EPAD50               | DD N JFET               | JPAD50                  |                 |               |
| E103   | N JFET                  | J105-18                 |                 |               | EPAD100              | DD N JFET               | JPAD100                 |                 |               |
| E105   | N JFET                  | J105-18                 |                 |               | EPAD200              | DD N JFET               | JPAD200                 |                 |               |
| E106   | N JFET                  | J106-18                 |                 |               | EPAD500              | DD N JFET               | JPAD500                 |                 |               |
| E107   | N JFET                  | J107-18                 |                 |               | FE100                | N JFET                  | 2N3821                  |                 |               |
| E108   | N JFET                  | J108-18                 |                 |               | FE100A               | N JFET                  | 2N3821                  |                 |               |
| E109   | N JFET                  | J109-18                 |                 |               | FE102                | N JFET                  | 2N4119                  |                 |               |
| E110   | N JFET                  | J110-18                 |                 |               | FE102A               | N JFET                  | 2N4119                  |                 |               |
| E111   | N JFET                  | J111-18                 |                 |               | FE104                | N JFET                  | 2N4118                  |                 |               |
| E112   | N JFET                  | J112-18                 |                 |               | FE104A               | N JFET                  | 2N4118                  |                 |               |
| E113   | N JFET                  | J113-18                 |                 |               | FE200                | N JFET                  | 2N3821                  |                 |               |
| E114   | N JFET                  | K114-18                 |                 |               | FE202                | N JFET                  | 2N3821                  |                 |               |
| E174   | P JFET                  | J174-18                 |                 |               | FE204                | N JFET                  | 2N3821                  |                 |               |
| E175   | P JFET                  | J175-18                 |                 |               | FE300                | N JFET                  | 2N3822                  |                 |               |
| E176   | P JFET                  | J176-18                 |                 |               | FE302                | N JFET                  | 2N3821                  |                 |               |
| E177   | P JFET                  | J177-18                 |                 |               | FE304                | N JFET                  | 2N3821                  |                 |               |
| E201   | N JFET                  | J201-18                 |                 |               | FE0654A              | N JFET                  | 2N5486                  |                 |               |
| E202   | N JFET                  | J202-18                 |                 |               | FE0654B              | N JFET                  | 2N5485                  |                 |               |
| E203   | N JFET                  | J203-18                 |                 |               | FE3819               | N JFET                  | 2N3819                  |                 |               |
| E204   | N JFET                  | J204-18                 |                 |               | FE5457               | N JFET                  | 2N5457                  |                 |               |
| E210   | N JFET                  | K210-18                 |                 |               | FE5458               | N JFET                  | 2N5458                  |                 |               |
| E211   | N JFET                  | K211-18                 |                 |               | FE5459               | N JFET                  | 2N5459                  |                 |               |
| E212   | N JFET                  | K212-18                 |                 |               | FE5484               | N JFET                  | 2N5484                  |                 |               |
| E230   | N JFET                  | J230-18                 |                 |               | FE5485               | N JFET                  | 2N5485                  |                 |               |
| E231   | N JFET                  | J231-18                 |                 |               | FE5486               | N JFET                  | 2N5486                  |                 |               |
| E232   | N JFET                  | J232-18                 |                 |               | FM3954               | D N JFET                | 2N3954                  |                 |               |
| E270   | P JFET                  | J270-18                 |                 |               | FM3954A              | D N JFET                | 2N3954A                 |                 |               |
| E271   | P JFET                  | J271-18                 |                 |               | FM3955               | D N JFET                | 2N3955                  |                 |               |
| E300   | N JFET                  | K300-18                 |                 |               | FM3955A              | D N JFET                | 2N3955A                 |                 |               |
| E304   | N JFET                  | K304-18                 |                 |               | FM3956               | D N JFET                | 2N3956                  |                 |               |
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| E310   | N JFET                  | K310-18                 |                 |               | FT0654B              | N JFET                  | 2N5486                  |                 |               |
| E400   | D N JFET                | U410                    |                 |               | FT0654C              | N JFET                  | 2N4221                  |                 |               |
| E401   | D N JFET                | U411                    |                 |               | FT0654D              | N JFET                  | 2N4221                  |                 |               |
| E402   | D N JFET                | U410                    |                 |               | FT704                | P MOS ENH               | 3N163                   |                 |               |
| E410   | D N JFET                | U410                    |                 |               | GET5457              | N JFET                  | 2N5457                  |                 |               |
| E411   | D N JFET                | U411                    |                 |               | GET5458              | N JFET                  | 2N5458                  |                 |               |
| E412   | D N JFET                | U412                    |                 |               | GET5459              | N JFET                  | 2N5459                  |                 |               |
| E413   | D N JFET                | U410                    |                 |               | HDI61030             | P MOS ENH               | 3N163                   |                 |               |
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| KE3687               | N JFET                  | 2N3687                  |                 |               | MFE4009              | P JFET                  | 2N3329                  |                 |               |
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| NF533                | N JFET                  | 2N4339                  |                 |               | PF510                | P JFET                  | 2N5018                  |                 |               |
| NF580                | N JFET                  | 2N5432                  |                 |               | PF511                | P JFET                  | 2N5014                  |                 |               |
| NF581                | N JFET                  | 2N5432                  |                 |               | SU2078               | D N JFET                | U425                    |                 |               |
| NF582                | N JFET                  | 2N5433                  |                 |               | SU2079               | D N JFET                | U425                    |                 |               |
| NF583                | N JFET                  | 2N5434                  |                 |               | SU2098               | D N JFET                | 2N5197                  |                 |               |
| NF584                | N JFET                  | 2N5433                  |                 |               | SU2098A              | D N JFET                | 2N5197                  |                 |               |
| NF585                | N JFET                  | 2N4859                  |                 |               | SU2098B              | D N JFET                | 2N5196                  |                 |               |
| NF4302               | N JFET                  | 2N4302                  |                 |               | SU2099               | D N JFET                | 2N5197                  |                 |               |
| NF4303               | N JFET                  | 2N4303                  |                 |               | SU2099A              | D N JFET                | 2N5197                  |                 |               |
| NF4304               | N JFET                  | 2N4304                  |                 |               | SU2365               | D N JFET                | U401                    |                 |               |
| NF4445               | N JFET                  | 2N5432                  |                 |               | SU2365A              | D N JFET                | U401                    |                 |               |
| NF4446               | N JFET                  | 2N5433                  |                 |               | SU2366               | D N JFET                | U402                    |                 |               |
| NF4447               | N JFET                  | 2N5432                  |                 |               | SU2366A              | D N JFET                | U402                    |                 |               |
| NF4448               | N JFET                  | 2N5433                  |                 |               | SU2367               | D N JFET                | U403                    |                 |               |
| NF5163               | N JFET                  | 2N5163                  |                 |               | SU2367A              | D N JFET                | U403                    |                 |               |
| NF5457               | N JFET                  | 2N5457                  |                 |               | SU2368               | D N JFET                | U404                    |                 |               |
| NF5458               | N JFET                  | 2N5458                  |                 |               | SU2368A              | D N JFET                | U404                    |                 |               |
| NF5459               | N JFET                  | 2N5459                  |                 |               | SU2369               | D N JFET                | U405                    |                 |               |
| NF5484               | N JFET                  | 2N5484                  |                 |               | SU2369A              | D N JFET                | U405                    |                 |               |
| NF5485               | N JFET                  | 2N5485                  |                 |               | SU2410               | D N JFET                | U424                    |                 |               |
| NF5486               | N JFET                  | 2N5486                  |                 |               | SU2411               | D N JFET                | U425                    |                 |               |
| NF5555               | N JFET                  | 2N5555                  |                 |               | SU2412               | D N JFET                | U426                    |                 |               |
| NF5638               | N JFET                  | 2N5638                  |                 |               | TD5902               | D N JFET                | 2N5902                  |                 |               |
| NF5639               | N JFET                  | 2N5639                  |                 |               | TD5902               | D N JFET                | 2N5902                  |                 |               |
| NF5640               | N JFET                  | 2N5640                  |                 |               | TD5902A              | D N JFET                | 2N5902                  |                 |               |
| NF5653               | N JFET                  | 2N5653                  |                 |               | TD5903               | D N JFET                | 2N5903                  |                 |               |
| NF5654               | N JFET                  | 2N5654                  |                 |               | TD5903A              | D N JFET                | 2N5903                  |                 |               |
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| P1087-18             | P JFET                  | P1087-18                | 4-36            | 5-39          | TD5909               | D N JFET                | 2N5909                  |                 |               |
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| VMP21                | VMOS N ENH              | 2N6659                  |                 |               | VN90AA               | VMOS N ENH              | VN90AA                  |                 |               |
| VMP22                | VMOS N ENH              | 2N6661                  |                 |               | VN90AB               | VMOS N ENH              | VN90AB                  |                 |               |
| VN30AA               | VMOS N ENH              | VN30AA                  |                 |               | VN98AJ               | VMOS N ENH              | VN98AJ                  |                 |               |
| VN30AB               | VMOS N ENH              | VN30AB                  |                 |               | VN98AK               | VMOS N ENH              | VN98AK                  |                 |               |
| VN33AJ               | VMOS N ENH              | VN33AJ                  |                 |               | VN99AJ               | VMOS N ENH              | VN99AJ                  |                 |               |
| VN33AK               | VMOS N ENH              | VN33AK                  |                 |               | VN99AK               | VMOS N ENH              | VN99AK                  |                 |               |
| VN35AA               | VMOS N ENH              | VN35AA                  |                 |               | WK5457               | N JFET                  | 2N5457                  |                 |               |
| VN35AB               | VMOS N ENH              | VN35AB                  |                 |               | WK5458               | N JFET                  | 2N5458                  |                 |               |
| VN35AJ               | VMOS N ENH              | VN35AJ                  |                 |               | WK5459               | N JFET                  | 2N5459                  |                 |               |
| VN35AK               | VMOS N ENH              | VN35AK                  |                 |               |                      |                         |                         |                 |               |

# product information



Siliconix products are divided into three basic categories:

**Standard Products, Modified Standard Products, Custom Products**

- **Standard Products** All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.
- **Examples of Modified Standard Products are:**

  - Electrical Specials* Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.
  - Mechanical Specials* Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.
  - High Reliability Specials* Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. These options include MIL-750B. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.

In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

- **Custom Products** Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

*FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054, Telephone: (408) 988-8000.*

### FETs/Part Number Prefixes and Suffixes

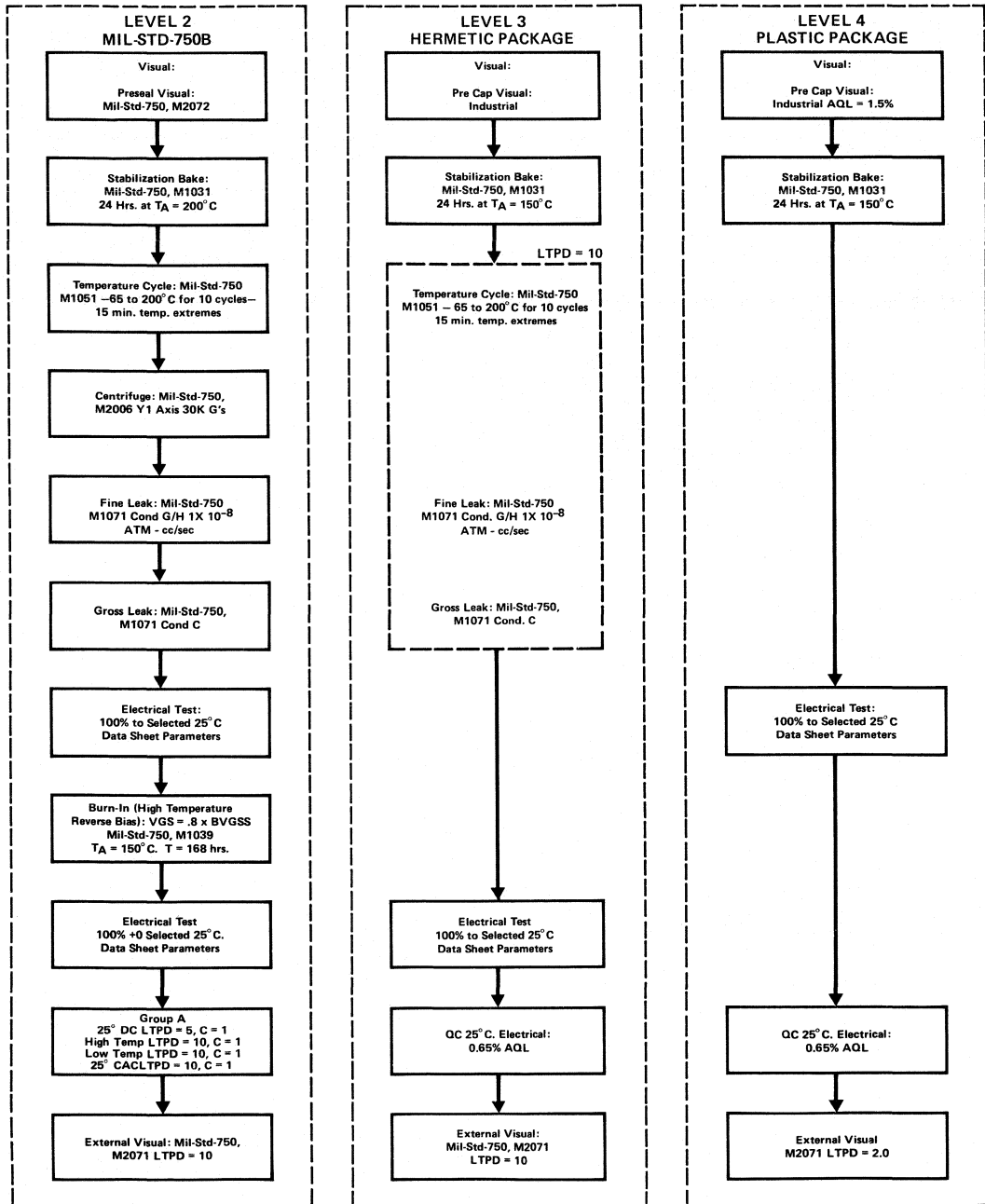
| Prefix | XXX   | XXXX                        |
|--------|---|-----------------------------|
| CR     | Si Standard N-Channel Current Regulator                   |                             |
| DPAD   | Si Standard Dual JFET Diode                               |                             |
| FN     | Special N-Channel JFET                                    | Special N-Channel JFET      |
| J      | Si Standard TO-92 Cased FET                               | Special TO-92 Cased FET     |
| JPAD   | Si Standard TO-92 Cased JFET Diode                        |                             |
| K      | Si Standard TO-92 Cased FET                               |                             |
| KK     | Si Standard TO-92 Cased FET                               |                             |
| M      | Si Standard MOSFET  |                             |
| MEM    | Si Standard MOSFET  |                             |
| MU     | Special MOSFET  |                             |
| PAD    | Si Standard JFET Diode                                    |                             |
| PF     | Special P-Channel JFET                                    |                             |
| PN     |   | Si Standard TO-92 Cased FET |
| SU     | Special P-Channel JFET                                    |                             |
| U      | Si Standard FET   | Si Standard FET             |
| VCR    | Si Standard N- and P-Channel Voltage Controlled Resistors |                             |
| VMP    | VMOS Power FET N-Channel                                  |                             |
| VN     |   | VMOS Power FET N-Channel    |
| 2N     |   | JEDEC-Registered Device     |
| 3N     | JEDEC-Registered Device                                   |                             |
| Suffix |   |                             |

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Std TO-92 Package with Center Lead Formed Toward Flat in TO-18 Pin Circle

The above prefix list does not include some second source products supplied by Siliconix. Refer to FET Cross Reference and Index or current price list for availability of these devices.

# process option flow chart



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Siliconix



# selector guides

index 2



## tips on selecting the right FET for your application



The "Product Specification," a short form version of technical data, will provide you direct reference to Siliconix part numbers and a condensed version of technical specifications

### IF YOU ARE NOT FAMILIAR WITH THE FET PARAMETERS YOU NEED:

1. Turn to page 2-2 "How to Choose the Correct FET for Your Application." Using this guide, determine the important FET parameters.
2. Next, turn to page 2-4 "JFET Geometry Selector Guide." Using this guide, choose the appropriate geometry.
3. Once you have chosen a geometry, turn to the "Geometry Characteristics" section 5 of the catalog. Here you make the choice of a suitable part number.
4. Now that you have the part number, you will find complete electrical specifications of these products in the "Data Sheets" sections 3 and 4 of the catalog.

### IF YOU ARE FAMILIAR WITH THE PARAMETERS YOU NEED:

1. Turn to the "Product Specifications" pages 2-6 through 2-16 to determine the proper part number(s).
2. Double-check your choices against the data sheets, and select the part most suited for your application.

# how to choose the correct FET for your application



| Application                  | Detail Application              | Important FET Parameters Required                             | Major Tradeoffs   | Unimportant FET Parameters  |
|------------------------------|---------------------------------|---|---|---|
| AMPLIFIER                    | Audio                           | Low noise ( $\bar{e}_n$ ), $g_{fs}/g_{os}$                    | Voltage amplification factor $\mu$<br>= $g_{fs}/g_{os}$<br>= $\Delta V_{DS}/\Delta V_{GS}$ @ $I_D = \text{const}$ | $R_{DS(on)}$<br>$V_{DS(on)}$<br>$I_D(off)$<br>Switching Times<br><br>Noise, $\bar{e}_n$ , NF while using high level signals<br><br>RF parameters while operating below RF frequencies<br><br>Capacitance & switching times while operating in audio and lower frequencies |
|                              | Buffer                          | Low $I_G$ , high $g_{fs}$                                     |   |   |
|                              | Differential                    | Good matching $V_{GS}$ , $g_{fs}$ , $I_{DSS}$ , $I_G$         |   |   |
|                              | High Input Impedance            | Very low $I_G$ (eg, MOSFET)                                   |   |   |
|                              | High Frequency                  | High $g_{fs}/C_{iss}$ ratio, NF, RF parameters                |   |   |
|                              | FET Input Op Amp                | Good matching $V_{GS}$ , $g_{fs}$ , $I_{DSS}$ , $I_G$         |   |   |
|                              | Low Distortion                  | High $V_{GS(off)}$ compared to signal amplitude               |   |   |
|                              | Low Supply Voltage              | Low $V_{GS(off)}$   |   |   |
|                              | Low Noise                       | Low $\bar{e}_n$ , $\bar{i}_n$ , low 1/f noise, low NF         |   |   |
|                              | Preamplifier                    | Operate near $I_{DZO}$ , high $g_{fs}/I_D$ ratio              |   |   |
| Video                        | High $g_{fs}/C_{iss}$ ratio, NF |   |   |   |
| CONSTANT CURRENT SOURCE      | Current Limiting                |   |   |   |
|                              | Reference Current Source        | Low $g_{oss}$ : low $V_{GS(off)}$ , high $BV_{GSS}$           |   | $g_{fs}$ , $R_{DS(on)}$ , $I_D(off)$ , $V_{DS(on)}$ switching times, RF parameters capacitance  |
|                              | Biasing                         |   |   |   |
| MIXERS                       | VHF                             | RF parameters, NF, high $g_{fs}/C_{iss}$ ratio, low $C_{rss}$ |   |   |
|                              | UHF                             |   |   |   |
|                              | Double Balanced                 | Matching characteristics                                      |   |   |
| OSCILLATORS                  | Class A                         | Good $g_{fs}$ at operating frequency                          |   |   |
|                              | Class C                         | Low $C_{iss}$ for VHF operation                               |   |   |
| SWITCHES                     | Analog Gates                    | Fast switching time   | $R_{DS(on)}$ vs Capacitance   | $g_{fs}$<br>$g_{os}$  |
|                              | Choppers                        | $r_{DS}/I_D(off)$ switching efficiency                        |   |   |
|                              | Commutators                     | Low $C_{iss}$   |   |   |
|                              | Digital                         | Fast switching time   |   |   |
|                              | Integrator Reset                | Very low $R_{DS(on)}$ , High $I_{DSS}$                        |   |   |
|                              | Sample and Hold                 | Low $C_{iss}$   |   |   |
| VOLTAGE CONTROLLED RESISTORS | Gain Control                    | High $V_{GS(off)}$ for wide dynamic range and low distortion  |   | $g_{fs}$ , $BV_{GSS}$ , $I_{DSS}$   |
|                              | Amplitude Stability             |   |   |   |
|                              | Attenuators                     |   |   |   |



# JFET geometry selector guide



Once you have chosen the major FET parameters, you will find selecting the optimum JFET geometry is easy. If you are familiar with Field Effect Transistors, start your selection using the characteristic graphs on page 2-4. You will find the  $V_{GS(off)}$  vs  $I_{DSS}$  graph the most meaningful, since it shows — in order of ascending active area — the complete line of Siliconix junction FETs.

To give you an idea how this guide works, let's find the most suitable geometry for a 70 ohm ON-resistance analog switch

which will be required to operate as close as 5 volts from the negative power supply. The power supply restraint requires a maximum  $V_{GS(off)}$  of 5 volts. Examining the  $R_{DS(on)}$  vs  $V_{GS(off)}$  figure, you will find the NC, NIP, and NVA geometries meet the  $R_{ON}$  and  $V_{GS(off)}$  requirements. In order to minimize your cost, choose the geometry having the least chip area, that is the NC. You will find characteristic data and part numbers in the Geometry Characteristics section of the catalog. Below are the most important parameter inter-relationships expressed in analytical form.

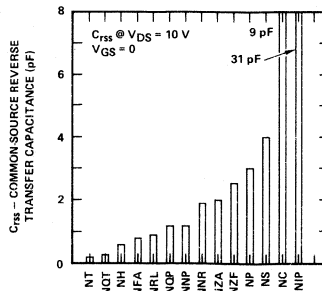
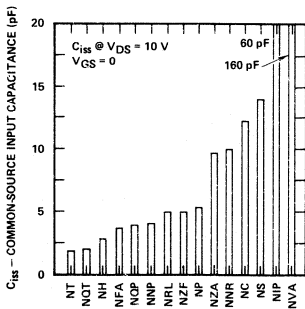
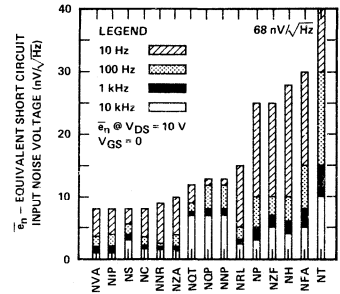
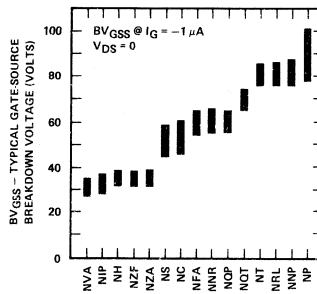
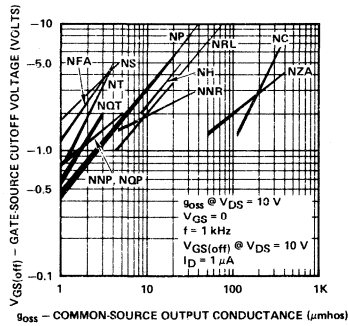
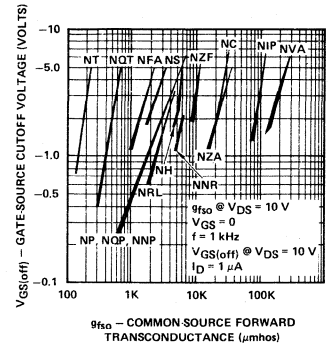
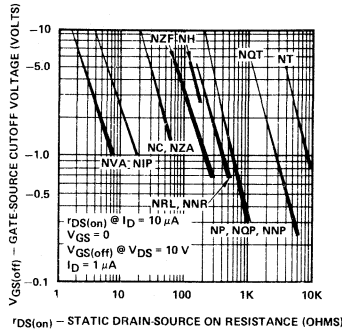
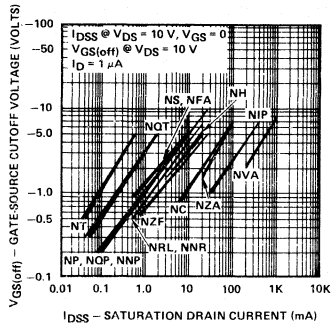
## USEFUL JFET PARAMETER RELATIONSHIPS (APPROX.)

|               |   |  |  |
|---------------|---|--|--|
| $g_{fs0}$     | = | $K \frac{I_{DSS}}{V_{GS(off)}}$                            | Forward transconductance as a function of $I_{DSS}$ and $V_{GS(off)}$ at zero gate-source voltage ( $K = 1.5$ to $2.5$ ; typically = $2$ for N-channel junction FET) |
| $g_{fs}$      | = | $g_{fs0} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$      | Variation of $g_{fs}$ with gate bias   |
| $g_{fs}$      | = | $g_{fs0} \sqrt{I_D / I_{DSS}}$                             | Variation of $g_{fs}$ with drain current   |
| $V_{GS(off)}$ | = | $\frac{2 I_{DSS}}{g_{fs0}}$                                | Gate-Source cutoff voltage in terms of $I_{DSS}$ and $g_{fs0}$   |
| $V_{DS}$      | ≈ | $V_{GS(off)} \left(\frac{I_D}{I_{DSS}}\right)^{1/2}$       | Drain voltage at which drain current saturates   |
| $r_{DS}$      | ≈ | $\frac{1}{g_{fs}}$   | Reciprocal relationship between drain-source resistance and forward transconductance. Accurate when $V_{DS} < V_{GS(off)}$ i.e. in the triode region                 |
| $r_{DS}$      | ≈ | $\frac{[V_{GS(off)}]^2}{K I_{DSS} [V_{GS(off)} - V_{GS}]}$ | $K = 1.5$ to $2.5$ Variation of drain resistance in the triode region  |
| $I_D$         | = | $I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$    | Variation of drain current with gate-source voltage. The square law transfer characteristic.   |

# JFET geometry selector guide (cont'd)



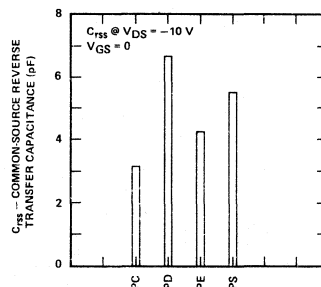
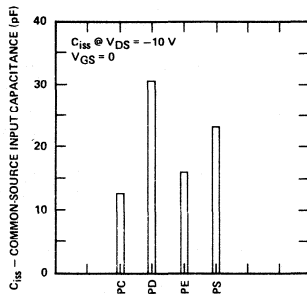
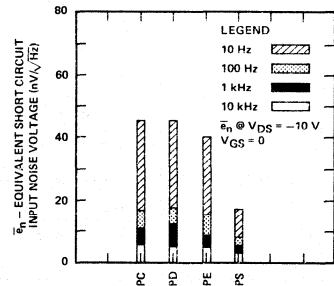
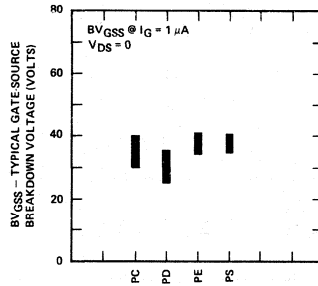
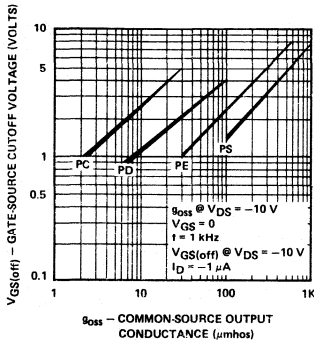
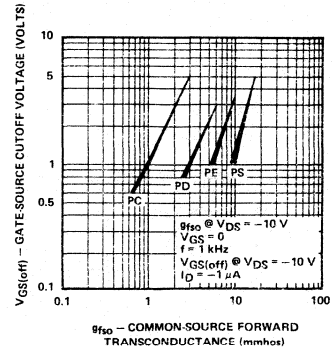
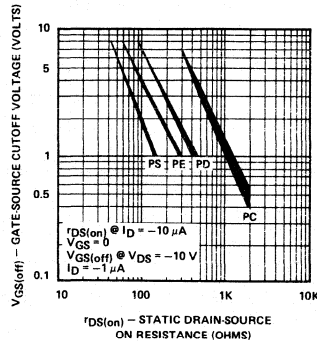
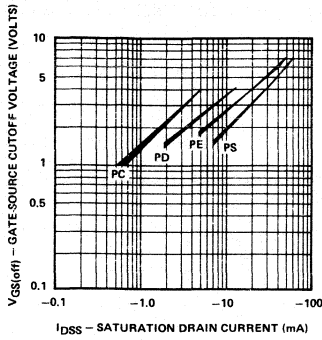
## n-channel JFETs



# JFET geometry selector guide (cont'd)



## p-channel JFET



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Siliconix

# Product Specifications



## N & P-Channel Single JFETs

| PART NUMBER | N or P | PACKAGE (TO- ) | LEAKAGE (nA, MAX.) |      | THRESHOLD VOLTAGE (V, MAX.) | BREAKDOWN VOLTAGE (V, MAX.) | SATURATION CURRENT (mA) |      | TRANS-CONDUCTANCE gfs (μmhos) |       | INPUT CAPACITANCE (pF, MAX.) | NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.) | RESISTANCE |              | GEOMETRY (Section 5) | DEVICE      |
|-------------|--------|----------------|--------------------|------|-----------------------------|-----------------------------|-------------------------|------|-------------------------------|-------|------------------------------|--|------------|--------------|----------------------|-------------|
|             |        |                | Gate               | Chnl |                             |                             | Min.                    | Max. | Min.                          | Max.  |                              |  | Gate Ω     | Chnl Ω, Max. |                      |             |
| 2N4117      | N      | 72             | 0.01               | —    | 1.8                         | 40                          | 0.03                    | 0.09 | 70                            | 210   | 3                            | —  | —          | —            | NT                   | LOW LEAKAGE |
| 2N4117A     | N      | 72             | 0.001              | —    | 1.8                         | 40                          | 0.03                    | 0.09 | 70                            | 210   | 3                            | —  | —          | —            | NT                   | LOW LEAKAGE |
| 2N4118      | N      | 72             | 0.01               | —    | 3.0                         | 40                          | 0.08                    | 0.24 | 80                            | 250   | 3                            | —  | —          | —            | NT                   | LOW LEAKAGE |
| 2N4118A     | N      | 72             | 0.001              | —    | 3.0                         | 40                          | 0.08                    | 0.24 | 90                            | 250   | 3                            | —  | —          | —            | NT                   | LOW LEAKAGE |
| 2N4119      | N      | 72             | 0.01               | —    | 6.0                         | 40                          | 0.2                     | 0.6  | 100                           | 330   | 3                            | —  | —          | —            | NT                   | LOW LEAKAGE |
| 2N4119A     | N      | 72             | 0.001              | —    | 6.0                         | 40                          | 0.2                     | 0.6  | 100                           | 330   | 3                            | —  | —          | —            | NT                   | LOW LEAKAGE |
| 2N3459      | N      | 18             | 0.25               | —    | 3.4                         | 50                          | 0.8                     | 4.0  | 1500                          | 6000  | 18                           | 4  | —          | 1M           | NP                   | LOW NOISE   |
| 2N3460      | N      | 18             | 0.25               | —    | 1.8                         | 50                          | 0.2                     | 1.0  | 800                           | 4500  | 18                           | 4  | —          | 1M           | NP                   | LOW NOISE   |
| 2N4220A     | N      | 72             | 0.1                | —    | 4.0                         | 30                          | 0.5                     | 3.0  | 1000                          | 4000  | 6                            | 2.5  | —          | 1M           | NRL                  | LOW NOISE   |
| 2N4221A     | N      | 72             | 0.1                | —    | 6.0                         | 30                          | 2.0                     | 6.0  | 2000                          | 5000  | 6                            | 2.5  | —          | 1M           | NRL                  | LOW NOISE   |
| 2N4222A     | N      | 72             | 0.1                | —    | 8.0                         | 30                          | 5.0                     | 15   | 2500                          | 6000  | 6                            | 2.5  | —          | 1M           | NRL                  | LOW NOISE   |
| 2N4338      | N      | 18             | 0.1                | —    | 1.0                         | 50                          | 0.6                     | 1.5  | 600                           | 1800  | 7                            | 1.0  | —          | 1M           | NP                   | LOW NOISE   |
| 2N4339      | N      | 18             | 0.1                | —    | 1.8                         | 50                          | 0.5                     | 1.5  | 800                           | 2400  | 7                            | 1.0  | —          | 1M           | NP                   | LOW NOISE   |
| 2N4340      | N      | 18             | 0.1                | —    | 3.0                         | 50                          | 1.2                     | 3.6  | 1300                          | 3000  | 7                            | 1.0  | —          | 1M           | NP                   | LOW NOISE   |
| 2N4341      | N      | 18             | 0.1                | —    | 6.0                         | 50                          | 3.0                     | 9.0  | 2000                          | 4000  | 7                            | 1.0  | —          | 1M           | NP                   | LOW NOISE   |
| 2N4867      | N      | 72             | 0.25               | —    | 2.0                         | 40                          | 0.4                     | 1.2  | 700                           | 2000  | 25                           | 20   | —          | —            | NS                   | LOW NOISE   |
| 2N4867A     | N      | 72             | 0.25               | —    | 2.0                         | 40                          | 0.4                     | 1.2  | 700                           | 2000  | 25                           | 10   | —          | —            | NS                   | LOW NOISE   |
| 2N4868      | N      | 72             | 0.25               | —    | 3.0                         | 40                          | 1.0                     | 3.0  | 1000                          | 3000  | 25                           | 20   | —          | —            | NS                   | LOW NOISE   |
| 2N4868A     | N      | 72             | 0.25               | —    | 3.0                         | 40                          | 1.0                     | 3.0  | 1000                          | 3000  | 25                           | 10   | —          | —            | NS                   | LOW NOISE   |
| 2N4869      | N      | 72             | 0.25               | —    | 5.0                         | 40                          | 2.5                     | 7.5  | 1300                          | 4000  | 25                           | 20   | —          | —            | NS                   | LOW NOISE   |
| 2N4869A     | N      | 72             | 0.25               | —    | 5.0                         | 40                          | 2.5                     | 7.5  | 1300                          | 4000  | 25                           | 10   | —          | —            | NS                   | LOW NOISE   |
| 2N5556      | N      | 72             | 0.1                | —    | 4.0                         | 30                          | 0.5                     | 2.5  | 1500                          | 6500  | 6                            | 35   | —          | —            | NRL                  | LOW NOISE   |
| 2N5557      | N      | 72             | 0.1                | —    | 5.0                         | 30                          | 2.0                     | 5.0  | 1500                          | 6500  | 6                            | 35   | —          | —            | NRL                  | LOW NOISE   |
| 2N5558      | N      | 72             | 0.1                | —    | 6.0                         | 30                          | 4.0                     | 10   | 1500                          | 6500  | 6                            | 35   | —          | —            | NRL                  | LOW NOISE   |
| J230        | N      | 92             | 0.25               | —    | 3.0                         | 40                          | 0.7                     | 3.0  | 1000                          | 2500  | —                            | 30   | —          | —            | NS                   | LOW NOISE   |
| J230-18     | N      | 92             | 0.25               | —    | 3.0                         | 40                          | 0.7                     | 3.0  | 1000                          | 2500  | —                            | 30   | —          | —            | NS                   | LOW NOISE   |
| J231        | N      | 92             | 0.25               | —    | 5.0                         | 40                          | 2.0                     | 6.0  | 1500                          | 3000  | —                            | 30   | —          | —            | NS                   | LOW NOISE   |
| J231-18     | N      | 92             | 0.25               | —    | 5.0                         | 40                          | 2.0                     | 6.0  | 1500                          | 3000  | —                            | 30   | —          | —            | NS                   | LOW NOISE   |
| J232        | N      | 92             | 0.25               | —    | 6.0                         | 40                          | 5.0                     | 10   | 2500                          | 4000  | —                            | 30   | —          | —            | NS                   | LOW NOISE   |
| J232-18     | N      | 92             | 0.25               | —    | 6.0                         | 40                          | 5.0                     | 10   | 2500                          | 4000  | —                            | 30   | —          | —            | NS                   | LOW NOISE   |
| J270-18     | P      | 92             | 0.2                | —    | 2.0                         | 30                          | 2.0                     | 15   | 6000                          | 15000 | —                            | —  | —          | —            | PS                   | LOW NOISE   |
| 2N3819      | N      | 92             | 2.0                | —    | 8.0                         | 25                          | 2.0                     | 20   | 2000                          | 6500  | 8.0                          | —  | —          | —            | NRL                  | RF AMP      |
| 2N3823      | N      | 72             | 0.5                | —    | 8.0                         | 30                          | 4.0                     | 20   | 3500                          | 6500  | 6                            | 2.5  | —          | 1K           | NRL                  | RF AMP      |
| 2N4223      | N      | 72             | 0.25               | —    | 8.0                         | 30                          | 3.0                     | 18   | 3000                          | 7000  | 6                            | 5.0  | —          | 1K           | NRL                  | RF AMP      |
| 2N4224      | N      | 72             | 0.5                | —    | 8.0                         | 30                          | 2.0                     | 20   | 2000                          | 7500  | 6                            | —  | —          | —            | NRL                  | RF AMP      |
| 2N4416      | N      | 72             | 0.1                | —    | 6.0                         | 30                          | 5.0                     | 15   | 4500                          | 7500  | 4                            | 2.0  | —          | 1K           | NH                   | RF AMP      |
| 2N4416A     | N      | 72             | 0.1                | —    | 6.0                         | 35                          | 5.0                     | 15   | 4500                          | 7500  | 4                            | 2.0  | —          | 1K           | NH                   | RF AMP      |
| 2N5078      | N      | 72             | 0.25               | —    | 8.0                         | 30                          | 4.0                     | 25   | 4500                          | 10000 | 6                            | 3.0  | —          | 1K           | —                    | RF AMP      |

# Product Specifications (cont'd)



## N & P-Channel Single JFETs

| PART NUMBER | N or P | PACKAGE (TO- ) | LEAKAGE (nA, MAX.) |      | THRESHOLD VOLTAGE (V, MAX.) | BREAKDOWN VOLTAGE (V, MAX.) | SATURATION CURRENT (mA) |      | TRANS-CONDUCTANCE gfs (μmhos) |        | INPUT CAPACITANCE (pF, MAX.) | NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.) | RESISTANCE |              | GEOMETRY (Section 5) | DEVICE |
|-------------|--------|----------------|--------------------|------|-----------------------------|-----------------------------|-------------------------|------|-------------------------------|--------|------------------------------|--|------------|--------------|----------------------|--------|
|             |        |                | Gate               | Chnl |                             |                             | Min.                    | Max. | Min.                          | Max.   |                              |  | Gate       | Chnl Ω, Max. |                      |        |
| 2N5484      | N      | 92             | 1.0                | —    | 3.0                         | 25                          | 1.0                     | 5.0  | 3000                          | 6000   | 5                            | 3.0  | 1K         | —            | NH                   |        |
| 2N5485      | N      | 92             | 1.0                | —    | 4.0                         | 25                          | 4.0                     | 10   | 3500                          | 7000   | 5                            | 2.0  | 1K         | —            | NH                   |        |
| 2N5486      | N      | 92             | 1.0                | —    | 6.0                         | 25                          | 8.0                     | 20   | 4000                          | 8000   | 5                            | 2.0  | 1K         | —            | NH                   |        |
| 2N5668      | N      | 92             | 2.0                | —    | 4.0                         | 25                          | 1.0                     | 5.0  | 1500                          | 6500   | 7                            | 2.5  | 1K         | —            | NH                   |        |
| 2N5669      | N      | 92             | 2.0                | —    | 6.0                         | 25                          | 4.0                     | 10   | 2000                          | 6500   | 7                            | 2.5  | 1K         | —            | NH                   |        |
| 2N5670      | N      | 92             | 2.0                | —    | 8.0                         | 25                          | 8.0                     | 20   | 3000                          | 7500   | 7.0                          | 2.5  | 1K         | —            | NH                   |        |
| J210        | N      | 92             | 0.1                | —    | 3.0                         | 25                          | 2.0                     | 15   | 4000                          | 12000  | —                            | —  | —          | —            | NZF                  |        |
| J211        | N      | 92             | 0.1                | —    | 4.5                         | 25                          | 7.0                     | 20   | 7000                          | 12000  | —                            | —  | —          | —            | NZF                  |        |
| J212        | N      | 92             | 0.1                | —    | 6.0                         | 25                          | 15                      | 40   | 7000                          | 12000  | —                            | —  | —          | —            | NZF                  |        |
| J270        | P      | 92             | 0.2                | —    | 2.0                         | 30                          | 2.0                     | 15   | 6000                          | 15000  | —                            | —  | —          | —            | PS                   |        |
| J271        | P      | 92             | 0.2                | —    | 4.5                         | 30                          | 6.0                     | 50   | 8000                          | 18000  | —                            | —  | —          | —            | PS                   |        |
| J300        | N      | 92             | 0.5                | —    | 6.0                         | 25                          | 6.0                     | 30   | 4500                          | 9000   | 5.5                          | —  | —          | —            | NZF                  |        |
| J304        | N      | 92             | 0.1                | —    | 6.0                         | 30                          | 5.0                     | 15   | 4500                          | 7500   | —                            | —  | —          | —            | NH                   |        |
| J305        | N      | 92             | 0.1                | —    | 3.0                         | 30                          | 1.0                     | 8.0  | 3000                          | —      | —                            | —  | —          | —            | NH                   |        |
| J308        | N      | 92             | 1.0                | —    | 6.5                         | 25                          | 12                      | 60   | 8000                          | 20000  | 7.5                          | —  | —          | —            | NZA                  |        |
| J309        | N      | 92             | 1.0                | —    | 4.0                         | 25                          | 12                      | 30   | 10000                         | 20000  | 7.5                          | —  | —          | —            | NZA                  |        |
| J310        | N      | 92             | 1.0                | —    | 6.5                         | 25                          | 24                      | 60   | 8000                          | 18000  | 7.5                          | —  | —          | —            | NZA                  |        |
| K210-18     | N      | 92             | 0.1                | —    | 3.0                         | 25                          | 2.0                     | 15   | 4000                          | 12000  | —                            | —  | —          | —            | NZF                  |        |
| K211-18     | N      | 92             | 0.1                | —    | 4.5                         | 25                          | 7.0                     | 20   | 7000                          | 12000  | —                            | —  | —          | —            | NZF                  |        |
| K212-18     | N      | 92             | 0.1                | —    | 6.0                         | 25                          | 15                      | 40   | 7000                          | 12000  | —                            | —  | —          | —            | NZF                  |        |
| K300-18     | N      | 92             | 0.5                | —    | 6.0                         | 25                          | 6.0                     | 30   | 4500                          | 9000   | 5.5                          | —  | —          | —            | NZF                  |        |
| K304-18     | N      | 92             | 0.1                | —    | 6.0                         | 30                          | 5.0                     | 15   | 4500                          | 7500   | —                            | —  | —          | —            | NH                   |        |
| K305-18     | N      | 92             | 0.1                | —    | 3.0                         | 30                          | 1.0                     | 8.0  | 3000                          | —      | —                            | —  | —          | —            | NH                   |        |
| K308-18     | N      | 92             | 1.0                | —    | 6.5                         | 25                          | 12                      | 60   | 8000                          | 20000  | 7.5                          | —  | —          | —            | NZA                  |        |
| K309-18     | N      | 92             | 1.0                | —    | 4.0                         | 25                          | 12                      | 30   | 10000                         | 20000  | 7.5                          | —  | —          | —            | NZA                  |        |
| K310-18     | N      | 92             | 1.0                | —    | 6.5                         | 25                          | 24                      | 60   | 8000                          | 18000  | 7.5                          | —  | —          | —            | NZA                  |        |
| KK4416-18   | N      | 92             | 0.25               | —    | 8.0                         | 30                          | 4.0                     | 25   | 4500                          | 10000  | 6.0                          | 3.0  | 1K         | —            | NH                   |        |
| PN4416      | N      | 92             | 1.0                | —    | 6.0                         | 30                          | 5.0                     | 15   | 4500                          | 7500   | 4.0                          | 2.0  | 1K         | —            | NH                   |        |
| MPF102      | N      | 92             | 2.0                | —    | 7.5                         | 25                          | 2.0                     | 20   | 2000                          | 7500   | 7.0                          | —  | —          | —            | NH                   |        |
| MPF108      | N      | 92             | 1.0                | —    | 8.0                         | 25                          | 1.5                     | 24   | 2000                          | 7500   | 6.5                          | 2.5  | 1M         | —            | NH                   |        |
| MPF112      | N      | 92             | 100                | —    | 10                          | 25                          | 1.0                     | 25   | 1000                          | 7500   | —                            | —  | —          | —            | NH                   |        |
| U308        | N      | 52             | 0.15               | —    | 6.0                         | 25                          | 12                      | 60   | 10000                         | 20000  | 7.5                          | —  | —          | —            | NZA                  |        |
| U309        | N      | 52             | 0.15               | —    | 4.0                         | 25                          | 12                      | 30   | 10000                         | 20000  | 7.5                          | —  | —          | —            | NZA                  |        |
| U310        | N      | 52             | 0.15               | —    | 6.0                         | 25                          | 24                      | 60   | 10000                         | 18000  | 7.5                          | —  | —          | —            | NZA                  |        |
| U311        | N      | 72             | 0.15               | —    | 6.0                         | 25                          | 20                      | 60   | 10000                         | 20000  | 7.5                          | —  | —          | —            | NZA                  |        |
| U312        | N      | 52             | 0.1                | —    | 6.0                         | 25                          | 10                      | 30   | 6000                          | 10000  | 5.0                          | —  | —          | —            | NZF                  |        |
| U320        | N      | 39             | 3.0                | —    | 10                          | 25                          | 100                     | 500  | 75000                         | 200000 | 30                           | —  | —          | —            | NIP                  |        |
| U321        | N      | 39             | 3.0                | —    | 4.0                         | 25                          | 80                      | 250  | 75000                         | 200000 | 30                           | —  | —          | —            | NIP                  |        |

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# Product Specifications (cont'd)



## N & P-Channel Single JFETs

| PART NUMBER | N or P | PACKAGE (TO- ) | LEAKAGE (nA, MAX.) |      | THRESHOLD VOLTAGE (V, MAX.) | BREAKDOWN VOLTAGE (V, MAX.) | SATURATION CURRENT (mA) |      | TRANS-CONDUCTANCE gfs (μmhos) |        | INPUT CAPACITANCE (pF, MAX.) | NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.) | RESISTANCE |              | GEOMETRY (Section 5) | DEVICE |
|-------------|--------|----------------|--------------------|------|-----------------------------|-----------------------------|-------------------------|------|-------------------------------|--------|------------------------------|--|------------|--------------|----------------------|--------|
|             |        |                | Gate               | Chnl |                             |                             | Min.                    | Max. | Min.                          | Max.   |                              |  | Gate Ω     | Chnl Ω, Max. |                      |        |
| U322        | N      | 39             | 3.0                | -    | 10                          | 25                          | 200                     | 700  | 75000                         | 200000 | 30                           | -  | -          | NIP          |                      |        |
| U1837       | N      | 92             | 0.25               | -    | 8.0                         | 30                          | 4.0                     | 25   | 4500                          | 10000  | 6.0                          | 3.0  | 1K         | NH           |                      |        |
| U1837-18    | N      | 92             | 0.25               | -    | 8.0                         | 30                          | 4.0                     | 25   | 4500                          | 10000  | 6.0                          | 3.0  | 1K         | NH           |                      |        |
| U1994       | N      | 92             | 0.1                | -    | 6.0                         | 30                          | 5.0                     | 15   | 4500                          | 7500   | 4.0                          | -  | -          | NH           |                      |        |
| 2N3824      | N      | 72             | 0.1                | 0.1  | 8.0                         | 50                          | -                       | -    | -                             | -      | 6.0                          | -  | -          | NRL          |                      |        |
| 2N3966      | N      | 72             | 0.1                | 1.0  | 6.0                         | 30                          | 2.0                     | -    | -                             | -      | 6.0                          | -  | -          | NH           |                      |        |
| 2N3966      | N      | 72             | 0.1                | 6.0  | 6.0                         | 30                          | 5.0                     | -    | -                             | -      | 6.0                          | -  | -          | NH           |                      |        |
| 2N3970      | N      | 18             | 0.25               | 0.25 | 10                          | 40                          | 50                      | 150  | -                             | -      | 25                           | -  | -          | NC           |                      |        |
| 2N3971      | N      | 18             | 0.25               | 0.25 | 5.0                         | 40                          | 25                      | 75   | -                             | -      | 25                           | -  | -          | NC           |                      |        |
| 2N3972      | N      | 18             | 0.25               | 0.25 | 3.0                         | 40                          | 30                      | 30   | -                             | -      | 25                           | -  | -          | NC           |                      |        |
| 2N4091      | N      | 18             | 0.2                | 0.2  | 10                          | 40                          | 30                      | 30   | -                             | -      | 16                           | -  | -          | NC           |                      |        |
| 2N4092      | N      | 18             | 0.2                | 0.2  | 7.0                         | 40                          | 15                      | -    | -                             | -      | 16                           | -  | -          | NC           |                      |        |
| 2N4093      | N      | 18             | 0.2                | 0.2  | 5.0                         | 40                          | 8.0                     | -    | -                             | -      | 16                           | -  | -          | NC           |                      |        |
| 2N4391      | N      | 18             | 0.1                | 0.1  | 10                          | 40                          | 50                      | 150  | -                             | -      | 14                           | -  | -          | NC           |                      |        |
| 2N4392      | N      | 18             | 0.1                | 0.1  | 5.0                         | 40                          | 25                      | 75   | -                             | -      | 14                           | -  | -          | NC           |                      |        |
| 2N4393      | N      | 18             | 0.1                | 0.1  | 3.0                         | 40                          | 5.0                     | 30   | -                             | -      | 14                           | -  | -          | NC           |                      |        |
| 2N4856      | N      | 18             | 0.25               | 0.25 | 10                          | 40                          | 50                      | -    | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4856A     | N      | 18             | 0.25               | 0.25 | 10                          | 40                          | 50                      | -    | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4857      | N      | 18             | 0.25               | 0.25 | 6.0                         | 40                          | 20                      | 100  | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4857A     | N      | 18             | 0.25               | 0.25 | 6.0                         | 40                          | 20                      | 100  | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4858      | N      | 18             | 0.25               | 0.25 | 4.0                         | 40                          | 8.0                     | 80   | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4858A     | N      | 18             | 0.25               | 0.25 | 4.0                         | 40                          | 8.0                     | 80   | -                             | -      | 10                           | -  | -          | NC           |                      |        |
| 2N4859      | N      | 18             | 0.25               | 0.25 | 10                          | 30                          | 50                      | -    | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4859A     | N      | 18             | 0.25               | 0.25 | 10                          | 30                          | 50                      | -    | -                             | -      | 10                           | -  | -          | NC           |                      |        |
| 2N4860      | N      | 18             | 0.25               | 0.25 | 6.0                         | 30                          | 20                      | 100  | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4860A     | N      | 18             | 0.25               | 0.25 | 6.0                         | 30                          | 20                      | 100  | -                             | -      | 10                           | -  | -          | NC           |                      |        |
| 2N4861      | N      | 18             | 0.25               | 0.25 | 4.0                         | 30                          | 8.0                     | 80   | -                             | -      | 18                           | -  | -          | NC           |                      |        |
| 2N4861A     | N      | 18             | 0.25               | 0.25 | 4.0                         | 30                          | 8.0                     | 80   | -                             | -      | 10                           | -  | -          | NC           |                      |        |
| 2N5018      | P      | 18             | 2.0                | 10.0 | 10                          | 30                          | 10                      | -    | -                             | -      | 45                           | -  | -          | PS           |                      |        |
| 2N5019      | P      | 18             | 2.0                | 10.0 | 5.0                         | 30                          | 5.0                     | -    | -                             | -      | 45                           | -  | -          | PS           |                      |        |
| 2N5114      | P      | 18             | 0.5                | 0.5  | 10                          | 30                          | 30                      | 90   | -                             | -      | 25                           | -  | -          | PS           |                      |        |
| 2N5115      | P      | 18             | 0.5                | 0.5  | 6.0                         | 30                          | 15                      | 60   | -                             | -      | 25                           | -  | -          | PS           |                      |        |
| 2N5116      | P      | 18             | 0.5                | 0.5  | 4.0                         | 30                          | 5.0                     | 25   | -                             | -      | 25                           | -  | -          | PS           |                      |        |
| 2N5432      | N      | 52             | 0.2                | 0.2  | 10                          | 25                          | 150                     | -    | -                             | -      | 30                           | -  | -          | NIP          |                      |        |
| 2N5433      | N      | 52             | 0.2                | 0.2  | 9.0                         | 25                          | 100                     | -    | -                             | -      | 30                           | -  | -          | NIP          |                      |        |
| 2N5434      | N      | 52             | 0.2                | 0.2  | 4.0                         | 25                          | 30                      | -    | -                             | -      | 30                           | -  | -          | NH           |                      |        |
| 2N5555      | N      | 92             | 1.0                | 10.0 | 10                          | 25                          | 15                      | -    | -                             | -      | 10                           | -  | -          | NH           |                      |        |
| 2N5638      | N      | 92             | 1.0                | 1.0  | 12                          | 30                          | 50                      | -    | -                             | -      | 10                           | -  | -          | NC           |                      |        |
| 2N5639      | N      | 92             | 1.0                | 1.0  | 8.0                         | 30                          | 25                      | -    | -                             | -      | 10                           | -  | -          | NC           |                      |        |

# Product Specifications (cont'd)



## N & P-Channel Single JFETs

| PART NUMBER | N or P | PACKAGE (TO- ) | LEAKAGE (nA, MAX.) |      | THRESHOLD VOLTAGE (V, MAX.) | BREAKDOWN VOLTAGE (V, MAX.) | SATURATION CURRENT (mA) |      | TRANS-CONDUCTANCE gfs (μmhos) |      | INPUT CAPACITANCE (pF, MAX.) | NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.) | RESISTANCE |              | GEOMETRY (Section 5) | DEVICE |
|-------------|--------|----------------|--------------------|------|-----------------------------|-----------------------------|-------------------------|------|-------------------------------|------|------------------------------|--|------------|--------------|----------------------|--------|
|             |        |                | Gate               | Chnl |                             |                             | Min.                    | Max. | Min.                          | Max. |                              |  | Gate Ω     | Chnl Ω, Max. |                      |        |
| 2N5640      | N      | 92             | 1.0                | 1.0  | 6.0                         | 30                          | 5.0                     | -    | -                             | -    | 10                           | -  | -          | 100          | NC                   | NC     |
| 2N5653      | N      | 92             | 1.0                | 1.0  | 12                          | 30                          | 40                      | -    | -                             | -    | 10                           | -  | -          | 50           | NC                   | NC     |
| 2N5654      | N      | 92             | 1.0                | 1.0  | 8.0                         | 30                          | 15                      | -    | -                             | -    | 10                           | -  | -          | 100          | NC                   | NC     |
| J105        | N      | 92             | 3.0                | 3.0  | 10.0                        | 25                          | 500                     | -    | -                             | -    | -                            | -  | -          | 3.0          | NVA                  | NVA    |
| J105-18     | N      | 92             | 3.0                | 3.0  | 10                          | 25                          | 500                     | -    | -                             | -    | -                            | -  | -          | 3.0          | NVA                  | NVA    |
| J106        | N      | 92             | 3.0                | 3.0  | 6.0                         | 25                          | 200                     | -    | -                             | -    | -                            | -  | -          | 6.0          | NVA                  | NVA    |
| J106-18     | N      | 92             | 3.0                | 3.0  | 6.0                         | 25                          | 200                     | -    | -                             | -    | -                            | -  | -          | 6.0          | NVA                  | NVA    |
| J107        | N      | 92             | 3.0                | 3.0  | 4.5                         | 25                          | 100                     | -    | -                             | -    | -                            | -  | -          | 8.0          | NVA                  | NVA    |
| J107-18     | N      | 92             | 3.0                | 3.0  | 4.5                         | 25                          | 100                     | -    | -                             | -    | -                            | -  | -          | 8.0          | NVA                  | NVA    |
| J108        | N      | 92             | 3.0                | 3.0  | 10                          | 25                          | 80                      | -    | -                             | -    | -                            | -  | -          | 8.0          | NIP                  | NIP    |
| J108-18     | N      | 92             | 3.0                | 3.0  | 10                          | 25                          | 80                      | -    | -                             | -    | -                            | -  | -          | 8.0          | NIP                  | NIP    |
| J109        | N      | 92             | 3.0                | 3.0  | 6.0                         | 25                          | 40                      | -    | -                             | -    | -                            | -  | -          | 12           | NIP                  | NIP    |
| J109-18     | N      | 92             | 3.0                | 3.0  | 6.0                         | 25                          | 40                      | -    | -                             | -    | -                            | -  | -          | 12           | NIP                  | NIP    |
| J110        | N      | 92             | 3.0                | 3.0  | 4.0                         | 25                          | 10                      | -    | -                             | -    | -                            | -  | -          | 18           | NIP                  | NIP    |
| J110-18     | N      | 92             | 3.0                | 3.0  | 4.0                         | 25                          | 10                      | -    | -                             | -    | -                            | -  | -          | 18           | NIP                  | NIP    |
| J111        | N      | 92             | 1.0                | 1.0  | 10                          | 35                          | 20                      | -    | -                             | -    | -                            | -  | -          | 30           | NC                   | NC     |
| J111-18     | N      | 92             | 1.0                | 1.0  | 10                          | 35                          | 20                      | -    | -                             | -    | -                            | -  | -          | 30           | NC                   | NC     |
| J112        | N      | 92             | 1.0                | 1.0  | 5.0                         | 35                          | 5.0                     | -    | -                             | -    | -                            | -  | -          | 50           | NC                   | NC     |
| J112-18     | N      | 92             | 1.0                | 1.0  | 5.0                         | 35                          | 5.0                     | -    | -                             | -    | -                            | -  | -          | 50           | NC                   | NC     |
| J113        | N      | 92             | 1.0                | 1.0  | 3.0                         | 35                          | 2.0                     | -    | -                             | -    | -                            | -  | -          | 100          | NC                   | NC     |
| J113-18     | N      | 92             | 1.0                | 1.0  | 3.0                         | 35                          | 2.0                     | -    | -                             | -    | -                            | -  | -          | 100          | NC                   | NC     |
| J114        | N      | 92             | 1.0                | 1.0  | 10                          | 25                          | 15                      | -    | -                             | -    | -                            | -  | -          | 150          | NIF                  | NIF    |
| J174        | P      | 92             | 1.0                | 1.0  | 10                          | 30                          | 20                      | 100  | -                             | -    | -                            | -  | -          | 85           | PS                   | PS     |
| J174-18     | P      | 92             | 1.0                | 1.0  | 10                          | 30                          | 20                      | 100  | -                             | -    | -                            | -  | -          | 85           | PS                   | PS     |
| J175        | P      | 92             | 1.0                | 1.0  | 6.0                         | 30                          | 7.0                     | 60   | -                             | -    | -                            | -  | -          | 125          | PS                   | PS     |
| J175-18     | P      | 92             | 1.0                | 1.0  | 6.0                         | 30                          | 7.0                     | 60   | -                             | -    | -                            | -  | -          | 125          | PS                   | PS     |
| J176        | P      | 92             | 1.0                | 1.0  | 4.0                         | 30                          | 2.0                     | 25   | -                             | -    | -                            | -  | -          | 250          | PS                   | PS     |
| J176-18     | P      | 92             | 1.0                | 1.0  | 4.0                         | 30                          | 2.0                     | 25   | -                             | -    | -                            | -  | -          | 250          | PS                   | PS     |
| J177        | P      | 92             | 1.0                | 1.0  | 2.25                        | 30                          | 1.5                     | 20   | -                             | -    | -                            | -  | -          | 300          | PS                   | PS     |
| J177-18     | P      | 92             | 1.0                | 1.0  | 2.25                        | 30                          | 1.5                     | 20   | -                             | -    | -                            | -  | -          | 300          | PS                   | PS     |
| K114-18     | N      | 92             | 1.0                | 1.0  | 10                          | 25                          | 15                      | -    | -                             | -    | -                            | -  | -          | 150          | NZF                  | NZF    |
| PN4391      | N      | 92             | 1.0                | 1.0  | 10                          | 40                          | 50                      | 150  | -                             | -    | -                            | -  | -          | 30           | NC                   | NC     |
| PN4391-18   | N      | 92             | 1.0                | 1.0  | 10                          | 40                          | 50                      | 150  | -                             | -    | -                            | -  | -          | 30           | NC                   | NC     |
| PN4392      | N      | 92             | 1.0                | 1.0  | 5.0                         | 40                          | 25                      | 75   | -                             | -    | -                            | -  | -          | 60           | NC                   | NC     |
| PN4392-18   | N      | 92             | 1.0                | 1.0  | 5.0                         | 40                          | 25                      | 75   | -                             | -    | -                            | -  | -          | 60           | NC                   | NC     |
| PN4393      | N      | 92             | 1.0                | 1.0  | 3.0                         | 40                          | 5.0                     | 30   | -                             | -    | -                            | -  | -          | 100          | NC                   | NC     |
| PN4393-18   | N      | 92             | 1.0                | 1.0  | 3.0                         | 40                          | 5.0                     | 30   | -                             | -    | -                            | -  | -          | 100          | NC                   | NC     |
| P1086       | P      | 92             | 2.0                | 10.0 | 10                          | 30                          | 10                      | -    | -                             | -    | -                            | -  | -          | 75           | PS                   | PS     |
| P1086-18    | P      | 92             | 2.0                | 10.0 | 10                          | 30                          | 10                      | -    | -                             | -    | -                            | -  | -          | 75           | PS                   | PS     |

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# Product Specifications (cont'd)



## N & P-Channel Single JFETs

| PART NUMBER | N or P | PACKAGE (TO- ) | LEAKAGE (nA, MAX.) |      | THRESHOLD VOLTAGE (V, MAX.) | BREAKDOWN VOLTAGE (V, MAX.) | SATURATION CURRENT (mA) |      | TRANS-CONDUCTANCE gfs (μmhos) |       | INPUT CAPACITANCE (pF, MAX.) | NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.) | RESISTANCE |              | GEOMETRY (Section 5) | DEVICE |
|-------------|--------|----------------|--------------------|------|-----------------------------|-----------------------------|-------------------------|------|-------------------------------|-------|------------------------------|--|------------|--------------|----------------------|--------|
|             |        |                | Gate               | Chnl |                             |                             | Min.                    | Max. | Min.                          | Max.  |                              |  | Gate Ω     | Chnl Ω, Max. |                      |        |
| P1087       | P      | 92             | 2.0                | 10.0 | 5.0                         | 30                          | 5.0                     | —    | —                             | —     | 45                           | —  | —          | PS           |                      |        |
| P1087-18    | P      | 92             | 2.0                | 10.0 | 5.0                         | 30                          | 5.0                     | —    | —                             | —     | 45                           | —  | —          | PS           |                      |        |
| U200        | N      | 18             | 1.0                | 1.0  | 3.0                         | 30                          | 3.0                     | 25   | —                             | —     | 30                           | —  | —          | NC           |                      |        |
| U201        | N      | 18             | 1.0                | 1.0  | 5.0                         | 30                          | 15                      | 75   | —                             | —     | 30                           | —  | —          | NC           |                      |        |
| U202        | N      | 18             | 1.0                | 1.0  | 10                          | 30                          | 30                      | 150  | —                             | —     | 30                           | —  | —          | NC           |                      |        |
| U290        | N      | 52             | 1.0                | 1.0  | 10                          | 30                          | 500                     | —    | —                             | —     | 60                           | —  | —          | NVA          | 2.5                  |        |
| U291        | N      | 52             | 1.0                | 1.0  | 4.5                         | 30                          | 200                     | —    | —                             | —     | 60                           | —  | —          | NVA          | 7.0                  |        |
| U304        | P      | 18             | 0.5                | 0.5  | 10                          | 30                          | 90                      | —    | —                             | —     | 27                           | —  | —          | PS           | 85                   |        |
| U305        | P      | 18             | 0.5                | 0.5  | 6.0                         | 30                          | 15                      | 60   | —                             | —     | 27                           | —  | —          | PS           | 110                  |        |
| U306        | P      | 18             | 0.5                | 0.5  | 4.0                         | 30                          | 5.0                     | 25   | —                             | —     | 27                           | —  | —          | PS           | 175                  |        |
| U1897       | N      | 92             | 0.4                | 0.2  | 10                          | 40                          | 30                      | —    | —                             | —     | 16                           | —  | —          | NC           | 30                   |        |
| U1897-18    | N      | 92             | 0.4                | 0.2  | 10                          | 40                          | 30                      | —    | —                             | —     | 16                           | —  | —          | NC           | 30                   |        |
| U1898       | N      | 92             | 0.4                | 0.2  | 7.0                         | 40                          | 15                      | —    | —                             | —     | 16                           | —  | —          | NC           | 30                   |        |
| U1898-18    | N      | 92             | 0.4                | 0.2  | 7.0                         | 40                          | 15                      | —    | —                             | —     | 16                           | —  | —          | NC           | 30                   |        |
| U1899       | N      | 92             | 0.4                | 0.2  | 5.0                         | 40                          | 8.0                     | —    | —                             | —     | 16                           | —  | —          | NC           | 80                   |        |
| U1899-18    | N      | 92             | 0.4                | 0.2  | 5.0                         | 40                          | 8.0                     | —    | —                             | —     | 16                           | —  | —          | NC           | 80                   |        |
| 2N2608      | P      | 18             | 10                 | —    | 4.0                         | 30                          | 0.9                     | 4.5  | 1000                          | —     | 17                           | —  | —          | PC           | 1M                   |        |
| 2N2609      | P      | 18             | 30                 | —    | 4.0                         | 30                          | 2.0                     | 10.0 | 2500                          | —     | 30                           | —  | —          | PD           | 1M                   |        |
| 2N2843      | P      | 18             | 10                 | —    | 1.7                         | 30                          | 0.2                     | 1.0  | 540                           | —     | 17                           | —  | —          | PC           | 1M                   |        |
| 2N2844      | P      | 18             | 30                 | —    | 1.7                         | 30                          | 0.44                    | 2.2  | 1400                          | —     | 30                           | —  | —          | PD           | 1M                   |        |
| 2N3329      | P      | 72             | 10                 | —    | 5.0                         | 20                          | 1.0                     | 3.0  | 1000                          | 2000  | 20                           | —  | —          | PC           | 1M                   |        |
| 2N3330      | P      | 72             | 10                 | —    | 6.0                         | 20                          | 2.0                     | 6.0  | 1500                          | 3000  | 20                           | —  | —          | PC           | 1M                   |        |
| 2N3331      | P      | 72             | 10                 | —    | 8.0                         | 20                          | 5.0                     | 15   | 2000                          | 4000  | 20                           | —  | —          | PC           | 1M                   |        |
| 2N3332      | P      | 72             | 10                 | —    | 6.0                         | 20                          | 1.0                     | 6.0  | 1000                          | 2200  | 20                           | —  | —          | PC           | 1M                   |        |
| 2N3368      | N      | 18             | 5.0                | —    | 11.5                        | 40                          | 2.0                     | 12   | 1000                          | 4000  | 20                           | —  | —          | NP           | NP                   |        |
| 2N3369      | N      | 18             | 5.0                | —    | 6.5                         | 40                          | 0.5                     | 2.5  | 600                           | 2500  | 20                           | —  | —          | NP           | NP                   |        |
| 2N3370      | N      | 18             | 5.0                | —    | 3.2                         | 40                          | 0.1                     | 0.6  | 300                           | 2500  | 20                           | —  | —          | NP           | NP                   |        |
| 2N3382      | P      | 72             | 15                 | —    | 5.0                         | 30                          | 3.0                     | 30   | 4500                          | 12500 | 20                           | —  | —          | PE           | PE                   |        |
| 2N3384      | P      | 72             | 15                 | —    | 5.0                         | 30                          | 15.0                    | 30   | 7500                          | 12500 | —                            | —  | —          | PE           | PE                   |        |
| 2N3386      | P      | 72             | 15                 | —    | 9.5                         | 30                          | 15.0                    | 50   | 7500                          | 15000 | —                            | —  | —          | PE           | PE                   |        |
| 2N3436      | N      | 18             | 0.5                | —    | 9.8                         | 50                          | 3.0                     | 15   | 2500                          | 10000 | 18                           | —  | —          | NP           | NP                   |        |
| 2N3437      | N      | 18             | 0.5                | —    | 4.8                         | 50                          | 0.8                     | 4.0  | 1500                          | 6000  | 18                           | —  | —          | NP           | NP                   |        |
| 2N3438      | N      | 18             | 0.5                | —    | 2.3                         | 50                          | 0.2                     | 1.0  | 800                           | 4500  | 18                           | —  | —          | NP           | NP                   |        |
| 2N3458      | N      | 18             | 0.25               | —    | 7.8                         | 50                          | 3.0                     | 15   | 2500                          | 10000 | 18                           | —  | —          | NP           | NP                   |        |
| 2N3684      | N      | 72             | 0.1                | —    | 5.0                         | 50                          | 2.5                     | 7.5  | 2000                          | 3000  | 4                            | —  | —          | NFA          | NFA                  |        |
| 2N3685      | N      | 72             | 0.1                | —    | 3.5                         | 50                          | 1.0                     | 3.0  | 1500                          | 2500  | 4                            | —  | —          | NFA          | NFA                  |        |
| 2N3686      | N      | 72             | 0.1                | —    | 2.0                         | 50                          | 0.4                     | 1.2  | 1000                          | 2000  | 4                            | —  | —          | NFA          | NFA                  |        |
| 2N3687      | N      | 72             | 0.1                | —    | 1.2                         | 50                          | 0.1                     | 0.5  | 500                           | 1500  | 4                            | —  | —          | NFA          | NFA                  |        |



# Product Specifications (cont'd)



## N & P-Channel Single JFETs

| DEVICE  |                      | GENERAL PURPOSE  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| GEOMETRY (Section 5)  |                      | NRL<br>NRL<br>PC<br>NRL<br>NRL<br>NRL<br>NRL<br>NRL<br>NRL<br>NRL<br>NP<br>NP<br>NP<br>NP<br>NP<br>NP<br>NP<br>NP<br>PS<br>NP<br>NP<br>NP<br>NP<br>NP<br>NP<br>NP<br>NP<br>—<br>NRL<br>NRL   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| RESISTANCE  | Chnl $\Omega$ , Max. | —  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|   | Gate $\Omega$        | —<br>—<br>—<br>—<br>—<br>—<br>1M<br>1M<br>100M<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>1M<br>1M<br>1M<br>1M<br>1M<br>1M<br>1M<br>—<br>1M<br>—  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| NOISE VOLTAGE (nV/ $\sqrt{\text{Hz}}$ , MAX.) or (NF, dB, MAX.) |                      | 200<br>200<br>—<br>—<br>—<br>—<br>3.0<br>3.0<br>3.0<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>2.0<br>2.0<br>2.0<br>2.0<br>2.0<br>3.0<br>2.0<br>50.0<br>2.5<br>—  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| INPUT CAPACITANCE (pF, MAX.)                                    |                      | 6<br>6<br>32<br>6<br>6<br>6<br>7<br>7<br>7<br>5.0<br>5.0<br>5.0<br>5.0<br>5.0<br>5.0<br>5.0<br>5.0<br>—<br>6<br>6.0<br>6.0<br>6.0<br>6.0<br>6.0<br>6.0<br>6.0<br>20<br>7.0<br>—  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| TRANS-CONDUCTANCE $g_{fs}$ ( $\mu\text{hos}$ )                  | Max.                 | 4500<br>6500<br>5000<br>4000<br>5000<br>6000<br>5000<br>5500<br>6000<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>18000<br>—<br>—<br>—<br>—<br>—<br>—<br>—<br>9000<br>6000<br>—   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|   | Min.                 | 1500<br>3000<br>1000<br>1000<br>2000<br>2500<br>1000<br>1500<br>2000<br>500<br>500<br>1000<br>1000<br>1500<br>1500<br>—<br>—<br>8000<br>1000<br>1000<br>2000<br>2000<br>1000<br>1000<br>2000<br>800<br>500   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SATURATION CURRENT (mA)   | Max.                 | 2.5<br>10<br>15<br>3.0<br>6.0<br>15<br>5.0<br>9.0<br>16<br>—<br>—<br>—<br>1.00<br>4.5<br>4.5<br>20<br>20<br>—<br>—<br>50<br>5.0<br>5.0<br>10<br>10<br>15<br>15<br>40.0<br>24<br>20   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|   | Min.                 | 0.5<br>2.0<br>0.3<br>0.5<br>2.0<br>5.0<br>1.0<br>2.0<br>4.0<br>0.2<br>0.2<br>0.9<br>0.9<br>4.0<br>4.0<br>—<br>—<br>6.0<br>0.5<br>0.5<br>4.0<br>4.0<br>0.5<br>0.5<br>1.0<br>0.5<br>0.5<br>10  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| BREAKDOWN VOLTAGE (V, MAX.)                                     |                      | 50<br>50<br>20<br>30<br>30<br>30<br>25<br>25<br>40<br>40<br>40<br>40<br>25<br>25<br>30<br>30<br>30<br>30<br>30<br>30<br>30<br>25<br>25<br>20<br>20   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| THRESHOLD VOLTAGE (V, MAX.)                                     |                      | 4.0<br>6.0<br>8.0<br>4.0<br>6.0<br>8.0<br>6.0<br>7.0<br>8.0<br>1.5<br>1.5<br>4.0<br>4.0<br>10<br>10<br>2.0<br>2.0<br>4.5<br>4.0<br>4.0<br>6.0<br>6.0<br>10.0<br>10<br>8.0<br>8.0<br>10   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| LEAKAGE (nA; MAX.)  | Chnl                 | —  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|   | Gate                 | 0.1<br>0.1<br>10<br>0.1<br>0.1<br>0.1<br>1.0<br>1.0<br>1.0<br>0.1<br>0.1<br>0.1<br>0.1<br>0.1<br>0.2<br>1.0<br>1.0<br>1.0<br>1.0<br>1.0<br>1.0<br>1.0<br>1.0<br>1.0<br>1.0<br>1.0<br>100   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PACKAGE (TO- )  |                      | 72<br>72<br>72<br>72<br>72<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92<br>92   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| N or P  |                      | N<br>N<br>P<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>P<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N<br>N   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PART NUMBER   |                      | 2N3821<br>2N3822<br>2N3909<br>2N4220<br>2N4221<br>2N4222<br>2N5457<br>2N5458<br>2N5459<br>J201<br>J201-18<br>J202<br>J202-18<br>J203<br>J203-18<br>J204<br>J204-18<br>J271-18<br>PN4302<br>PN4302-18<br>PN4303<br>PN4303-18<br>PN4304<br>PN4304-18<br>PN5163<br>MPF109<br>MPF111 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

# Product Specifications (cont'd)



## N-Channel Dual JFETs

| PART NUMBER | N or P | PACKAGE (TO- ) | LEAKAGE (nA, MAX.) |      | THRESHOLD VOLTAGE (V, MAX.) | BREAKDOWN VOLTAGE (V, MAX.) | SATURATION CURRENT (mA) |      | TRANS-CONDUCTANCE gfs (μmhos) |      | INPUT CAPACITANCE (pF, MAX.) | NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.) | THRESHOLD               |                     | OUTPUT CONDUCTANCE g <sub>os</sub> (μmhos, MAX.) | GEOMETRY (Section 5) | DEVICE |
|-------------|--------|----------------|--------------------|------|-----------------------------|-----------------------------|-------------------------|------|-------------------------------|------|------------------------------|--|-------------------------|---------------------|--|----------------------|--------|
|             |        |                | Gate               |      |                             |                             | Min.                    | Max. | Min.                          | Max. |                              |  | Static Match (mV, Max.) | Temp Tracking μV/°C |  |                      |        |
| 2N5196      | N      | 71             | 0.025              | 0.7  | 4.0                         | 50                          | 0.7                     | 7.0  | 1000                          | —    | 6.0                          | 20   | 5.0                     | 50                  | NNP or NP-D                                      |                      |        |
| 2N5197      | N      | 71             | 0.025              | 0.7  | 4.0                         | 50                          | 0.7                     | 7.0  | 1000                          | —    | 6.0                          | 20   | 10                      | 50                  | NNP or NP-D                                      |                      |        |
| 2N5198      | N      | 71             | 0.025              | 0.7  | 4.0                         | 50                          | 0.7                     | 7.0  | 1000                          | —    | 6.0                          | 20   | 20                      | 50                  | NNP or NP-D                                      |                      |        |
| 2N5199      | N      | 71             | 0.025              | 0.7  | 4.0                         | 50                          | 0.7                     | 7.0  | 1000                          | —    | 6.0                          | 20   | 40                      | 50                  | NNP or NP-D                                      |                      |        |
| 2N5545      | N      | 71             | 0.1                | 0.5  | 4.5                         | 50                          | 0.5                     | 8.0  | 1500                          | —    | 6.0                          | 200  | 10                      | 25                  | NNP or NP-D                                      |                      |        |
| 2N5546      | N      | 71             | 0.1                | 0.5  | 4.5                         | 50                          | 0.5                     | 8.0  | 1500                          | —    | 6.0                          | 200  | 20                      | 25                  | NNP or NP-D                                      |                      |        |
| 2N5547      | N      | 71             | 0.1                | 0.5  | 4.5                         | 50                          | 0.5                     | 8.0  | 1500                          | —    | 6.0                          | 200  | 40                      | 25                  | NNP or NP-D                                      |                      |        |
| 2N5902      | N      | 78             | 0.005              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.2  | 5.0                     | 1.0                 | NT   |                      |        |
| 2N5903      | N      | 78             | 0.005              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.2  | 10                      | 1.0                 | NT   |                      |        |
| 2N5904      | N      | 78             | 0.005              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.2  | 20                      | 1.0                 | NT   |                      |        |
| 2N5905      | N      | 78             | 0.005              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.2  | 40                      | 1.0                 | NT   |                      |        |
| 2N5906      | N      | 78             | 0.002              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.1  | 5.0                     | 1.0                 | NT   |                      |        |
| 2N5907      | N      | 78             | 0.002              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.1  | 10                      | 1.0                 | NT   |                      |        |
| 2N5908      | N      | 78             | 0.002              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.1  | 20                      | 1.0                 | NT   |                      |        |
| 2N5909      | N      | 78             | 0.002              | 0.03 | 4.5                         | 40                          | 0.03                    | 0.5  | 70                            | —    | 3.0                          | 0.1  | 40                      | 1.0                 | NT   |                      |        |
| U401        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 10                      | 2.0                 | NNR  |                      |        |
| U402        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 20                      | 2.0                 | NNR  |                      |        |
| U403        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 25                      | 2.0                 | NNR  |                      |        |
| U404        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 25                      | 2.0                 | NNR  |                      |        |
| U405        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 25                      | 2.0                 | NNR  |                      |        |
| U406        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 40                      | 2.0                 | NNR  |                      |        |
| U421        | N      | 78             | 0.0002             | 0.06 | 2.0                         | 40                          | 0.06                    | 1.0  | 300                           | —    | 3.0                          | 10   | 10                      | 0.5                 | NQT  |                      |        |
| U422        | N      | 78             | 0.0002             | 0.06 | 2.0                         | 40                          | 0.06                    | 1.0  | 300                           | —    | 3.0                          | 10   | 15                      | 0.5                 | NQT  |                      |        |
| U423        | N      | 78             | 0.0002             | 0.06 | 2.0                         | 40                          | 0.06                    | 1.0  | 300                           | —    | 3.0                          | 10   | 25                      | 0.5                 | NQT  |                      |        |
| U424        | N      | 78             | 0.001              | 0.06 | 3.0                         | 40                          | 0.06                    | 1.8  | 300                           | —    | 3.0                          | 10   | 40                      | 0.5                 | NQT  |                      |        |
| U425        | N      | 78             | 0.001              | 0.06 | 3.0                         | 40                          | 0.06                    | 1.8  | 300                           | —    | 3.0                          | 10   | 15                      | 1.0                 | NQT  |                      |        |
| U426        | N      | 78             | 0.001              | 0.06 | 3.0                         | 40                          | 0.06                    | 1.8  | 300                           | —    | 3.0                          | 10   | 25                      | 1.0                 | NQT  |                      |        |
| 2N5515      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 30   | 5.0                     | 1.0                 | NS   |                      |        |
| 2N5516      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 30   | 10                      | 1.0                 | NS   |                      |        |
| 2N5517      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 30   | 20                      | 1.0                 | NS   |                      |        |
| 2N5518      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 30   | 40                      | 1.0                 | NS   |                      |        |
| 2N5519      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 30   | 80                      | 1.0                 | NS   |                      |        |
| 2N5520      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 15   | 5.0                     | 1.0                 | NS   |                      |        |
| 2N5521      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 15   | 10                      | 1.0                 | NS   |                      |        |
| 2N5522      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 15   | 20                      | 1.0                 | NS   |                      |        |
| 2N5523      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 15   | 40                      | 1.0                 | NS   |                      |        |
| 2N5524      | N      | 71             | 0.25               | 0.5  | 4.0                         | 40                          | 0.5                     | 7.5  | 1000                          | —    | 25                           | 15   | 80                      | 1.0                 | NS   |                      |        |
| U401        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 10                      | 2.0                 | NNR  |                      |        |
| U402        | N      | 71             | 0.025              | 0.5  | 2.5                         | 50                          | 0.5                     | 10   | 2000                          | —    | 8.0                          | 20   | 10                      | 2.0                 | NNR  |                      |        |

# Product Specifications (cont'd)



## N-Channel Dual JFETs

| PART NUMBER | N or P | PACKAGE (TO- ) | LEAKAGE (nA, MAX.) |     | THRESHOLD VOLTAGE (V, MAX.) | BREAKDOWN VOLTAGE (V, MAX.) | SATURATION CURRENT (mA) |       | TRANS-CONDUCTANCE gfs (μmhos) |      | INPUT CAPACITANCE (pF, MAX.) | NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.) | THRESHOLD               |                     | OUTPUT CONDUCTANCE gas (μmhos, MAX.) | GEOMETRY (Section 5) | DEVICE |
|-------------|--------|----------------|--------------------|-----|-----------------------------|-----------------------------|-------------------------|-------|-------------------------------|------|------------------------------|--|-------------------------|---------------------|--------------------------------------|----------------------|--------|
|             |        |                | Gate               |     |                             |                             | Min.                    | Max.  | Min.                          | Max. |                              |  | Static Match (mV, Max.) | Temp Tracking μV/°C |                                      |                      |        |
| U404        | N      | 71             | 0.025              | 10  | 2.5                         | 50                          | 0.5                     | 2000  | —                             | 8.0  | 20                           | 15   | 25                      | 2.0                 | NNR                                  | LOW NOISE            |        |
| U405        | N      | 71             | 0.025              | 10  | 2.5                         | 50                          | 0.5                     | 2000  | —                             | 8.0  | 20                           | 20   | 40                      | 2.0                 | NNR                                  | LOW NOISE            |        |
| U406        | N      | 71             | 0.025              | 10  | 2.5                         | 50                          | 0.5                     | 2000  | —                             | 8.0  | 20                           | 40   | 80                      | 2.0                 | NNR                                  | LOW NOISE            |        |
| 2N5564      | N      | 71             | 0.1                | 30  | 3.0                         | 40                          | 5.0                     | 7500  | —                             | 12   | 50                           | 5.0  | 10                      | 45                  | NC                                   | RF AMPLIFIER         |        |
| 2N5565      | N      | 71             | 0.1                | 30  | 3.0                         | 40                          | 5.0                     | 7500  | —                             | 12   | 50                           | 10   | 25                      | 45                  | NC                                   | RF AMPLIFIER         |        |
| 2N5566      | N      | 71             | 0.1                | 30  | 3.0                         | 40                          | 5.0                     | 7500  | —                             | 12   | 50                           | 20   | 20                      | 45                  | NC                                   | RF AMPLIFIER         |        |
| 2N5911      | N      | 78             | 0.1                | 30  | 3.0                         | 40                          | 7.0                     | 5000  | —                             | 3.0  | 20                           | 10   | 20                      | 100                 | NZF                                  | RF AMPLIFIER         |        |
| 2N5912      | N      | 78             | 0.1                | 30  | 3.0                         | 40                          | 7.0                     | 5000  | —                             | 3.0  | 20                           | 15   | 40                      | 100                 | NZF                                  | RF AMPLIFIER         |        |
| U257        | N      | 78             | 0.1                | 30  | 3.0                         | 40                          | 5.0                     | 5000  | —                             | 5.0  | 30                           | 100  | —                       | 150                 | NZA                                  | RF AMPLIFIER         |        |
| U430        | N      | 99             | 0.15               | 30  | 4.0                         | 25                          | 12                      | 10000 | —                             | 7.5  | 12                           | —  | —                       | 150                 | NZA                                  | RF AMPLIFIER         |        |
| U431        | N      | 99             | 0.15               | 30  | 6.0                         | 25                          | 24                      | 10000 | —                             | 7.5  | 10                           | —  | —                       | 150                 | NZA                                  | RF AMPLIFIER         |        |
| U440        | N      | 71             | 0.50               | 60  | 6.0                         | 25                          | 6.0                     | 4500  | —                             | —    | —                            | 10   | —                       | 200                 | NZF                                  | RF AMPLIFIER         |        |
| U441        | N      | 71             | 0.50               | 60  | 6.0                         | 25                          | 6.0                     | 4500  | —                             | —    | —                            | 20   | —                       | 200                 | NZF                                  | RF AMPLIFIER         |        |
| U442        | N      | 71             | 0.50               | 60  | 6.0                         | 25                          | 6.0                     | 4500  | —                             | —    | —                            | 20   | —                       | 200                 | NZF                                  | RF AMPLIFIER         |        |
| 2N3921      | N      | 71             | 1.0                | 10  | 3.0                         | 50                          | 1.0                     | 1500  | —                             | 18   | 2.0                          | 5.0  | 10                      | 35                  | NNR or NRL-D                         | GENERAL PURPOSE      |        |
| 2N3922      | N      | 71             | 1.0                | 10  | 3.0                         | 50                          | 1.0                     | 1500  | —                             | 18   | 2.0                          | 5.0  | 25                      | 35                  | NNR or NRL-D                         | GENERAL PURPOSE      |        |
| 2N3954      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 0.5                          | 5.0  | 10                      | 35                  | NFA                                  | GENERAL PURPOSE      |        |
| 2N3954A     | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 0.5                          | 5.0  | 5.0                     | 35                  | NFA                                  | GENERAL PURPOSE      |        |
| 2N3955      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 0.5                          | 10   | 25                      | 35                  | NFA                                  | GENERAL PURPOSE      |        |
| 2N3955A     | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 0.5                          | 10   | 15                      | 35                  | NFA                                  | GENERAL PURPOSE      |        |
| 2N3956      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 0.5                          | 15   | 50                      | 35                  | NFA                                  | GENERAL PURPOSE      |        |
| 2N3957      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 0.5                          | 20   | 75                      | 35                  | NFA                                  | GENERAL PURPOSE      |        |
| 2N3958      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 0.5                          | 25   | 100                     | 35                  | NFA                                  | GENERAL PURPOSE      |        |
| 2N4084      | N      | 71             | 1.0                | 3.0 | 3.0                         | 50                          | 1.0                     | 1500  | —                             | 18   | 2                            | 15   | 10                      | 35                  | NNR or NRL-D                         | GENERAL PURPOSE      |        |
| 2N4085      | N      | 71             | 1.0                | 3.0 | 3.0                         | 50                          | 1.0                     | 1500  | —                             | 18   | 2                            | 15   | 25                      | 35                  | NNR or NRL-D                         | GENERAL PURPOSE      |        |
| 2N5045      | N      | 71             | 0.25               | 4.5 | 5.0                         | 50                          | 0.5                     | 1500  | —                             | 8.0  | 200                          | 5.0  | 67                      | 25                  | NNR or NRL-D                         | GENERAL PURPOSE      |        |
| 2N5046      | N      | 71             | 0.25               | 4.5 | 5.0                         | 50                          | 0.5                     | 1500  | —                             | 8.0  | 200                          | 10   | 133                     | 25                  | NNR or NRL-D                         | GENERAL PURPOSE      |        |
| 2N5047      | N      | 71             | 0.25               | 4.5 | 5.0                         | 50                          | 0.5                     | 1500  | —                             | 8.0  | 200                          | 15   | 200                     | 25                  | NNR or NRL-D                         | GENERAL PURPOSE      |        |
| 2N5452      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 20                           | 5.0  | 5.0                     | 1.0                 | NFA                                  | GENERAL PURPOSE      |        |
| 2N5453      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 20                           | 10   | 10                      | 1.0                 | NFA                                  | GENERAL PURPOSE      |        |
| 2N5454      | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 4.0  | 20                           | 15   | 25                      | 1.0                 | NFA                                  | GENERAL PURPOSE      |        |
| U231        | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 6.0  | 80                           | 5.0  | 10                      | 35                  | NNP or NP-D                          | GENERAL PURPOSE      |        |
| U232        | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 6.0  | 80                           | 10   | 25                      | 35                  | NNP or NP-D                          | GENERAL PURPOSE      |        |
| U233        | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 6.0  | 80                           | 15   | 50                      | 35                  | NNP or NP-D                          | GENERAL PURPOSE      |        |
| U234        | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 6.0  | 80                           | 20   | 75                      | 35                  | NNP or NP-D                          | GENERAL PURPOSE      |        |
| U235        | N      | 71             | 0.1                | 4.5 | 5.0                         | 50                          | 0.5                     | 1000  | —                             | 6.0  | 80                           | 25   | 100                     | 35                  | NNP or NP-D                          | GENERAL PURPOSE      |        |
| U410        | N      | 71             | 0.2                | 3.5 | 4.0                         | 40                          | 0.5                     | 1000  | —                             | —    | 13                           | 10   | 10                      | 20                  | NQP                                  | GENERAL PURPOSE      |        |
| U411        | N      | 71             | 0.2                | 3.5 | 4.0                         | 40                          | 0.5                     | 1000  | —                             | —    | 13                           | 20   | 25                      | 20                  | NQP                                  | GENERAL PURPOSE      |        |
| U412        | N      | 71             | 0.2                | 3.5 | 4.0                         | 40                          | 0.5                     | 1000  | —                             | —    | 13                           | 40   | 80                      | 20                  | NQP                                  | GENERAL PURPOSE      |        |

2



### Low Leakage Diodes

| Part Number | Package (TO- ) | Diode  | Reverse Current (pA, Max.) | Breakdown Voltage (Volts) |      | Forward Voltage Drop (pF, Max.) | Capacitance |
|-------------|----------------|--------|----------------------------|---------------------------|------|---------------------------------|-------------|
|             |                |        |                            | Min.                      | Max. |                                 |             |
| DPAD1       | 72             | Dual   | 1                          | 45                        | 120  | 1.5                             | 0.8         |
| DPAD2       | 72             | Dual   | 2                          | 45                        | 120  | 1.5                             | 0.8         |
| DPAD5       | 72             | Dual   | 5                          | 45                        | 120  | 1.5                             | 0.8         |
| DPAD10      | 72             | Dual   | 10                         | 35                        | —    | 1.5                             | 2.0         |
| DPAD20      | 72             | Dual   | 20                         | 35                        | —    | 1.5                             | 2.0         |
| DPAD50      | 72             | Dual   | 50                         | 35                        | —    | 1.5                             | 2.0         |
| DPAD100     | 72             | Dual   | 100                        | 35                        | —    | 1.5                             | 2.0         |
| JPAD50      | TO-92/TO-106   | Single | 20                         | 35                        | —    | 1.5                             | 2.0         |
| JPAD100     | TO-92/TO-106   | Single | 50                         | 35                        | —    | 1.5                             | 2.0         |
| JPAD200     | TO-92/TO-106   | Single | 100                        | 35                        | —    | 1.5                             | 2.0         |
| JPAD500     | TO-92/TO-106   | Single | 500                        | 35                        | —    | 1.5                             | 2.0         |
| PAD1        | 18             | Single | 1                          | 45                        | 120  | 1.5                             | 0.8         |
| PAD2        | 18             | Single | 2                          | 45                        | 120  | 1.5                             | 0.8         |
| PAD5        | 18             | Single | 5                          | 45                        | 120  | 1.5                             | 0.8         |
| PAD10       | 18             | Single | 10                         | 35                        | —    | 1.5                             | 2.0         |
| PAD20       | 18             | Single | 20                         | 35                        | —    | 1.5                             | 2.0         |
| PAD50       | 18             | Single | 50                         | 35                        | —    | 1.5                             | 2.0         |
| PAD100      | 18             | Single | 100                        | 35                        | —    | 1.5                             | 2.0         |

### Voltage Controlled Resistors

| Part Number | N or P | Package (TO- ) | Breakdown Voltage (Volts, Min.) | Threshold Voltage (Volts) |      | Resistance (Channel $\Omega$ ) |      | Geometry |
|-------------|--------|----------------|---------------------------------|---------------------------|------|--------------------------------|------|----------|
|             |        |                |                                 | Min.                      | Max. | Min.                           | Max. |          |
| VCR2N       | N      | 18             | 15                              | 3.5                       | 7.0  | 20                             | 60   | NC       |
| VCR3P       | P      | 72             | 15                              | 3.5                       | 7.0  | 70                             | 200  | PE       |
| VCR4N       | N      | 18             | 15                              | 3.5                       | 7.0  | 200                            | 600  | NP       |
| VCR5P       | P      | 72             | 15                              | 3.5                       | 7.0  | 300                            | 900  | PC       |
| VCR7N       | N      | 72             | 15                              | 2.5                       | 5.0  | 4000                           | 8000 | NT       |

### P-Channel MOSFETS

| Part Number | Package (TO- ) | Operating Mode | Threshold Voltage (Volts, Max.) | Resistance Channel ( $\Omega$ , Max.) | Leakage Channel On (mA) |      | Leakage Channel Off (nA, Max.) | Breakdown Voltage (Volts, Max.) | Input Capacitance (pF, Max.) | Reverse Capacitance (pF, Max.) | Geometry |
|-------------|----------------|----------------|---------------------------------|---------------------------------------|-------------------------|------|--------------------------------|---------------------------------|------------------------------|--------------------------------|----------|
|             |                |                |                                 |                                       | Min.                    | Max. |                                |                                 |                              |                                |          |
| 3N163       | 72             | ENH            | 5.0                             | 250                                   | 5.0                     | 30   | —                              | 40                              | 2.5                          | 0.7                            | MRA      |
| 3N164       | 72             | ENH            | 5.0                             | 300                                   | 3.0                     | 30   | —                              | 30                              | 2.5                          | 0.7                            | MRA      |
| MFE823      | 18             | ENH            | 6.0                             | —                                     | 3.0                     | —    | 20                             | 25                              | 6.0                          | 1.5                            | MRA      |



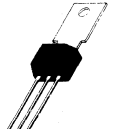
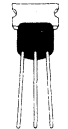
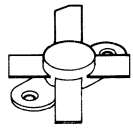
Current Regulator Diodes

| Part Number | Package (TO- ) | Forward Current (mA) | Forward Current Tolerance (%) | Limiting Voltage (Volts, Max.) | Peak Operating Voltage (Volts, Max.) | Dynamic Impedance (MΩ, Max.) | Forward Capacitance (pF, typ) | Geometry |
|-------------|----------------|----------------------|-------------------------------|--------------------------------|--------------------------------------|------------------------------|-------------------------------|----------|
| CR022       | 18             | 0.22                 | 10                            | 1.00                           | 100                                  | 13                           | —                             | NKL      |
| CR024       | 18             | 0.24                 | 10                            | 1.00                           | 100                                  | 10                           | —                             | NKL      |
| CR027       | 18             | 0.27                 | 10                            | 1.00                           | 100                                  | 9.0                          | —                             | NKL      |
| CR030       | 18             | 0.30                 | 10                            | 1.00                           | 100                                  | 8.0                          | —                             | NKL      |
| CR033       | 18             | 0.33                 | 10                            | 1.00                           | 100                                  | 6.6                          | —                             | NKL      |
| CR039       | 18             | 0.39                 | 10                            | 1.05                           | 100                                  | 4.1                          | —                             | NKL      |
| CR043       | 18             | 0.43                 | 10                            | 1.05                           | 100                                  | 3.3                          | —                             | NKL      |
| CR047       | 18             | 0.47                 | 10                            | 1.10                           | 100                                  | 2.7                          | —                             | NKL      |
| CR056       | 18             | 0.56                 | 10                            | 1.20                           | 100                                  | 1.9                          | —                             | NKL      |
| CR062       | 18             | 0.62                 | 10                            | 1.30                           | 100                                  | 1.55                         | —                             | NKL      |
| CR068       | 18             | 0.68                 | 10                            | 1.15                           | 100                                  | 1.35                         | —                             | NKM      |
| CR075       | 18             | 0.75                 | 10                            | 1.20                           | 100                                  | 1.15                         | —                             | NKM      |
| CR082       | 18             | 0.82                 | 10                            | 1.25                           | 100                                  | 1.00                         | —                             | NKM      |
| CR091       | 18             | 0.91                 | 10                            | 1.29                           | 100                                  | 0.88                         | —                             | NKM      |
| CR100       | 18             | 1.00                 | 10                            | 1.35                           | 100                                  | 0.80                         | —                             | NKM      |
| CR110       | 18             | 1.10                 | 10                            | 1.40                           | 100                                  | 0.70                         | —                             | NKM      |
| CR120       | 18             | 1.20                 | 10                            | 1.45                           | 100                                  | 0.64                         | —                             | NKM      |
| CR130       | 18             | 1.30                 | 10                            | 1.50                           | 100                                  | 0.58                         | —                             | NKM      |
| CR140       | 18             | 1.40                 | 10                            | 1.55                           | 100                                  | 0.54                         | —                             | NKM      |
| CR150       | 18             | 1.50                 | 10                            | 1.60                           | 100                                  | 0.51                         | —                             | NKM      |
| CR160       | 18             | 1.60                 | 10                            | 1.65                           | 100                                  | 0.475                        | —                             | NKO      |
| CR180       | 18             | 1.80                 | 10                            | 1.75                           | 100                                  | 0.42                         | —                             | NKO      |
| CR200       | 18             | 2.00                 | 10                            | 1.85                           | 100                                  | 0.395                        | —                             | NKO      |
| CR220       | 18             | 2.20                 | 10                            | 1.95                           | 100                                  | 0.37                         | —                             | NKO      |
| CR240       | 18             | 2.40                 | 10                            | 2.00                           | 100                                  | 0.345                        | —                             | NKO      |
| CR270       | 18             | 2.70                 | 10                            | 2.15                           | 100                                  | 0.32                         | —                             | NKO      |
| CR300       | 18             | 3.00                 | 10                            | 2.25                           | 100                                  | 0.30                         | —                             | NKO      |
| CR330       | 18             | 3.30                 | 10                            | 2.35                           | 100                                  | 0.28                         | —                             | NKO      |
| CR360       | 18             | 3.60                 | 10                            | 2.50                           | 100                                  | 0.265                        | —                             | NKO      |
| CR390       | 18             | 3.90                 | 10                            | 2.60                           | 100                                  | 0.255                        | —                             | NKO      |
| CR430       | 18             | 4.30                 | 10                            | 2.75                           | 100                                  | 0.245                        | —                             | NKO      |
| CR470       | 18             | 4.70                 | 10                            | 2.90                           | 100                                  | 0.235                        | —                             | NKO      |
| J500        | 92             | 0.24                 | 20                            | 1.20                           | 50                                   | 5.0                          | 2                             | NCL      |
| J501        | 92             | 0.33                 | 20                            | 1.30                           | 50                                   | 3.0                          | 2                             | NCL      |
| J502        | 92             | 0.43                 | 20                            | 1.50                           | 50                                   | 2.0                          | 2                             | NCL      |
| J503        | 92             | 0.56                 | 20                            | 1.70                           | 50                                   | 1.4                          | 2                             | NCL      |
| J504        | 92             | 0.75                 | 20                            | 1.90                           | 50                                   | 1.0                          | 2                             | NCL      |
| J505        | 92             | 1.00                 | 20                            | 2.10                           | 50                                   | 0.6                          | 2                             | NCL      |
| J506        | 92             | 1.40                 | 20                            | 2.50                           | 50                                   | 0.4                          | 2                             | NCL      |
| J507        | 92             | 1.80                 | 20                            | 2.80                           | 50                                   | 0.25                         | 2                             | NCL      |
| J508        | 92             | 2.40                 | 20                            | 3.10                           | 50                                   | 0.25                         | 2                             | NCL      |
| J509        | 92             | 3.00                 | 20                            | 3.50                           | 50                                   | 0.20                         | 2                             | NCL      |
| J510        | 92             | 3.60                 | 20                            | 3.90                           | 50                                   | 0.20                         | 2                             | NCL      |
| J511        | 92             | 4.70                 | 20                            | 4.20                           | 50                                   | 0.15                         | 2                             | NCL      |

# Product Specifications



## VMOS Power FETs

| RDS(on)  | BREAKDOWN VOLTAGE |                  |        |           |                  |                            |                  |           |       |                  | PACKAGE          |  |
|--|-------------------|------------------|--------|-----------|------------------|----------------------------|------------------|-----------|-------|------------------|------------------|--|
|  | 35 V              |                  | 40 V   |           | 60 V             |                            | 80 V             |           | 90 V  |                  |                  |  |
|  | ZENER             | NON-ZENER        | ZENER  | NON-ZENER | ZENER            | NON-ZENER                  | ZENER            | NON-ZENER | ZENER | NON-ZENER        |                  |  |
| 0.4<br>1.8<br>2.5<br>3.0<br>3.5<br>4.0<br>4.5<br>5.0 | 2N6656<br>VN35AA  | VN33AJ<br>VN35AJ |        |           | 2N6657<br>VN67AA | VN64GA<br>VN66AJ<br>VN67AJ |                  | VN89AA    |       | 2N6658<br>VN90AA | VN98AJ<br>VN99AJ | <br>TO-3      |
| 1.8<br>2.5<br>3.0<br>3.5<br>4.0<br>4.5<br>5.0        | 2N6659<br>VN35AB  | VN33AK<br>VN35AK |        |           | 2N6660<br>VN67AB | VN66AK<br>VN67AK           |                  | VN89AB    |       | 2N6661<br>VN90AB | VN98AK<br>VN99AK | <br>TO-39     |
| 3.0<br>3.5<br>4.0<br>4.5<br>5.0                      |                   |                  | VN46AF |           | VN66AF<br>VN67AF |                            | VN88AF<br>VN89AF |           |       |                  |                  | <br>TO-202AA  |
| 5.0  |                   |                  |        |           | VN10KM           |                            |                  |           |       |                  |                  | <br>TO-237   |
| 3.0  |                   |                  |        |           |                  | VMP4                       |                  |           |       |                  |                  | <br>380-SOE |

Detailed Technical Specifications for the VMOS Power FETs listed above *are not* included in this data book.

Please contact your nearest Siliconix Sales Office for a VMOS Design Catalog.

# Die Process Information



Siliconix is a large volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

## Physical Data

- Physical layout and dimensions are presented in the die topography section.
- Each die is passivated with approximately 8,000 angstroms of non-crystalline glass.
- All die are gold backed. Gold backing is approximately 1,500 angstroms thick.
- Die metallization is deposited aluminum approximately 12,000 angstroms thick.

## Die Screening Criteria

**Electrical Probe** — Die are 100% probed in wafer form at 25°C to DC criteria.

**Visual Criteria** — Die are supplied with 100% visual sort to the criteria of MIL-Std-750 method 2072.

## Packaging

Die are supplied in dust proof, anti-static waffle packs. (see illustration)

## Assembly

- Chips supplied in waffle packs normally do not require cleaning. Wafers should be cleaned after sawing or scribing, and fracturing.
- Chips should be handled with a vacuum pick-up with protected tip or with tweezers gripping the chip on its sides.
- When handling MOSFET chips, particularly non-gate protected types, steps must be taken to prevent damage by static discharge. In some extreme cases, handling precautions may be necessary for junction FET chips.
- Chips can be die attached either eutectically or by conductive epoxy when lower temperatures are necessary. Gold silicon eutectic occurs at temperatures between 385°C and 425°C.
- Bonding of wires from chip pads to posts can be achieved by thermocompression gold wire or ultrasonic aluminum wire bonded.

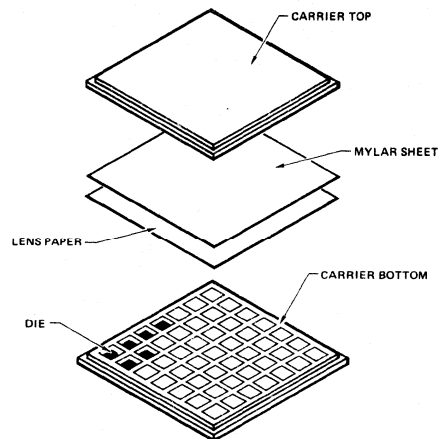
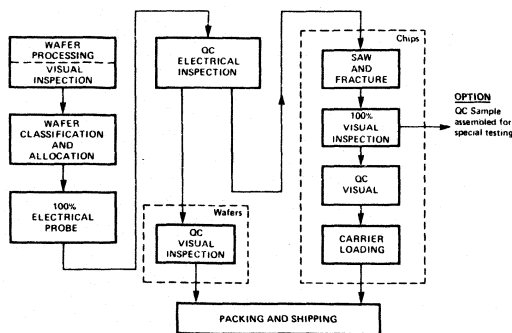
## Options

- **SEM** — Scanning electron microscope examination and control in accordance with MIL-Std-883 Method 2018 can be ordered on chips and wafers.
- **Wafer qualification to unprobed parameters** — sample testing of purchased chips to demonstrate capability to perform at data sheet temperature extremes by use of LTPD techniques can be provided.
- **Hot probe** — Siliconix has a chip processor/distributor with hot probe capability available.

## Chip Packaging

Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.

## Chip and Wafer Processing



NOTE: CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 1

## pc board layout and construction for low leakage applications



In order to realize the full capability of these devices in circuits that are sensitive to very low currents, considerable care should be exercised in PC board layout and construction techniques. If proper care is not taken, board leakage currents can easily become much larger than the leakage currents of the devices themselves, especially under conditions of high temperature and humidity. Excessive leakage currents can be produced by poor quality boards, socket leakage, poor board layout, imperfectly cleaned boards, or improperly applied or cured protective coatings.

It is important to start with quality PC boards which have high resistivity and low susceptance to moisture. Boards of teflon or polycarbonate composition exhibit these attributes and are preferred. Glass-epoxy boards are less desirable because they will absorb moisture, and if used must be protected with a conformal coating.

The use of sockets should be avoided wherever possible since the pin-to-pin isolation is often not great enough to prevent small leakage currents from occurring. These currents can significantly degrade device performance in low leakage applications. If sockets cannot be avoided use the highest quality available, preferably teflon.

In laying out PC boards, care should be taken to keep pins and runs which are sensitive to very low currents away from pins and runs which will be at significantly higher or lower voltages. The most common leakage current problems occur between pins sensitive to low current levels and nearby pins at or near one of the supply voltages. Thus, if the isolation between critical pins and nearby high or low voltage pins is increased, leakage is minimized.

In order to reduce leakage currents, it is very important that all PC boards and experimental breadboards be thoroughly cleaned with a solvent after construction. A recommended procedure is to wash each board in an ultrasonic cleaning bath of alcohol, trichloroethylene, or some other commercial solvent, and to blow dry with compressed air. The purpose of this is to remove all skin oils (the greatest cause of leakage in improperly cleaned boards), solder fluxes, and other films and residues left over from the construction process which can cause gross leakage problems and erratic device behavior, especially at temperatures above 85°C.

For best results, the thoroughly cleaned boards should be protected against dirt, conductive films, and humidity by the application of a conformal coating. Urethane and Dow Corning's R-4-3117 Silicone are easy to use and offer sufficient protection under most operating conditions. Epoxy results in a more durable coating but care must be taken to insure that it is cured properly; an improperly cured layer of epoxy will make the high temperature leakage problem worse. Union Carbide's Parylene also results in a relatively durable coating.

The ultimate leakage protection method consists of printed circuit metalization guard rings driven from a low impedance buffer amplifier whose output is at the same potential as the pin being protected. This completely eliminates board surface leakage at critical pins by removing any difference in potential, but it is difficult to implement due to the extra buffer amplifier required and the tight PC board metalization spacings encountered.



# **data sheets metal**

**index 3**



# p-channel JFETs designed for . . .



**Performance Curves PC PD**  
See Section 5

2N2608 2N2609

## ■ General Purpose Amplifiers

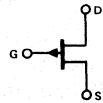
### BENEFITS

- JAN Approved Version Available

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3) . . . . . 30 V  
 Gate Current, Forward Biased (Note 1) . . . . . 50 mA  
 Total Device Dissipation (Derate 2 mW/°C) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C

TO-18  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                                 | 2N2608               |  | 2N2609 |       | Unit | Test Conditions  |      |  |             |
|--|----------------------|--|--------|-------|------|--|------|--|-------------|
|  | Min                  | Max                                    | Min    | Max   |      |  |      |  |             |
| 1<br>2<br>S<br>T<br>A<br>T<br>I<br>C<br>I<br>C | I <sub>GSS</sub>     | Gate Reverse Current (Note 2)          | 10     | 30    | nA   | V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V                      |      |  |             |
|  |                      |  | 10     | 30    | μA   | V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 0, T <sub>A</sub> = 150°C |      |  |             |
| 3  | BV <sub>GSS</sub>    | Gate-Source Breakdown Voltage          | 30     | 30    | V    | I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0 V                       |      |  |             |
| 4  | V <sub>GS(off)</sub> | Gate-Source Cutoff Voltage             | 1      | 4     | V    | V <sub>DS</sub> = -5 V, I <sub>D</sub> = 1 μA                      |      |  |             |
| 5  | I <sub>DSS</sub>     | Saturation Drain Current               | -0.90  | -4.50 | -2   | -10  | mA   | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0 V                      |             |
| 6<br>D<br>Y<br>N<br>A<br>M<br>I<br>C           | g <sub>fs</sub>      | Common-Source Forward Transconductance | 1000   | 2500  |      |  | μmho | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0 V                      | f = 1 kHz   |
| 7  | C <sub>iss</sub>     | Common-Source Input Capacitance        |        | 17    |      | 30   | pF   | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 1 V                      | f = 140 kHz |
| 8  | NF                   | Noise Figure                           |        | 3     |      | 3  | dB   | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1M Ω | f = 1 kHz   |

\*JEDEC Registered Data

PC

PD

#### NOTES:

1. Not JEDEC Registered
2. I<sub>GSS</sub> is JEDEC Registered at V<sub>GS</sub> = 5 V
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

3

Siliconix

# p-channel JFETs designed for . . .



**Performance Curves PC PD**  
**See Section 5**

## ■ Small-Signal Amplifiers

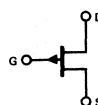
### BENEFITS

- Low Supply Voltage Operation  
 $V_{GS(off)}$  Typically 1.2 V

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3) . . . . . 30 V  
 Gate Current, Forward Biased (Note 1) . . . . . 50 mA  
 Total Device Dissipation (Derate 2mW/°C) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C

TO-18  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic |                      | 2N2843                        |       | 2N2844 |       | Unit | Test Conditions  |             |
|----------------|----------------------|-------------------------------|-------|--------|-------|------|--|-------------|
|                |                      | Min                           | Max   | Min    | Max   |      |  |             |
| 1              | I <sub>GSS</sub>     | Gate Reverse Current (Note 2) |       | 10     |       | nA   | V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0                        |             |
|                |                      |                               |       | 10     |       | μA   | V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 0, T <sub>A</sub> = 150°C |             |
| 3              | BV <sub>GSS</sub>    | 30                            |       | 30     |       | V    | I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0                         |             |
| 4              | V <sub>GS(off)</sub> |                               | 1.7   |        | 1.7   | V    | V <sub>DS</sub> = -5 V, I <sub>D</sub> = -1 μA                     |             |
| 5              | I <sub>DSS</sub>     | -200                          | -1000 | -440   | -2200 | μA   | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0                        |             |
| 6              | g <sub>fs</sub>      | 540                           |       | 1400   |       | μmho | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0                        | f = 1 kHz   |
| 7              | C <sub>iss</sub>     |                               | 17    |        | 30    | pF   | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 1 V                      | f = 140 kHz |
| 8              | NF                   |                               | 3     |        | 3     | dB   | V <sub>DS</sub> = -5 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1M Ω | f = 1 kHz   |

PC PD

\*JEDEC Registered Data

**NOTES:**

1. Not JEDEC Registered
2. I<sub>GSS</sub> is JEDEC Registered at V<sub>GS</sub> = 5 V.
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

# p-channel JFETs designed for . . .



**Performance Curves PC**  
See Section 5

- Small-Signal Amplifiers
- Analog Multipliers
- Modulators

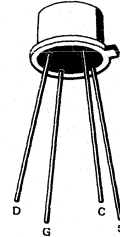
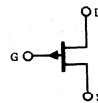
**BENEFITS**

- Ease of Amplifier Design  
     $I_{DSS}$  &  $G_{fs}$  Closely Specified

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain and Gate-Source Voltage (Note 1) . . . . . 20 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at (or below)  
 25°C Free-Air Temperature (Note 2) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 230°C

TO-72  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic |  | 2N3329 |      | 2N3330 |      | 2N3331 |      | 2N3332 |      | Unit   | Test Conditions   |            |
|----------------|--|--------|------|--------|------|--------|------|--------|------|--|---|------------|
|                |  | Min    | Max  | Min    | Max  | Min    | Max  | Min    | Max  |  |   |            |
| 1              | I <sub>GSS</sub> Gate Reverse Current                      |        | 0.01 |        | 0.01 |        | 0.01 |        | 0.01 | μA   | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0                               |            |
| 2              |  |        | 10   |        | 10   |        | 10   |        | 10   |  | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0, T <sub>A</sub> = 150°C       |            |
| 3              | BV <sub>GSS</sub> Gate-Source Breakdown Voltage            | 20     |      | 20     |      | 20     |      | 20     |      | V  | I <sub>G</sub> = 10 μA, V <sub>DS</sub> = 0                               |            |
| 4              | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage            |        | 5    |        | 6    |        | 8    |        | 6    |  | V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 μA                          |            |
| 5              | I <sub>DSS</sub> Saturation Drain Current                  | -1     | -3   | -2     | -6   | -5     | -15  | -1     | -6   | mA   | V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0                              |            |
| 6              | r <sub>DS(on)</sub> Drain-Source ON Resistance             |        | 1000 |        | 800  |        | 600  |        |      |  | I <sub>D</sub> = -100 μA, V <sub>GS</sub> = 0                             |            |
| 7              | g <sub>is</sub> Common-Source Input Conductance            |        | 0.2  |        | 0.2  |        | 0.2  |        | 0.2  | μmho   | V <sub>DS</sub> = -10 V   | f = 1 kHz  |
| 8              | g <sub>rs</sub> Common-Source Reverse Transfer Conductance |        | 0.1  |        | 0.1  |        | 0.1  |        | 0.1  |  |   |            |
| 9              | g <sub>os</sub> Common-Source Output Conductance           |        | 20   |        | 40   |        | 100  |        | 20   |  |   |            |
| 10             | g <sub>fs</sub> Common-Source Forward Transconductance     | 1000   | 2000 | 1500   | 3000 | 2000   | 4000 | 1000   | 2200 |  |   |            |
| 11             | g <sub>fs</sub> Common-Source Forward Transconductance     |        | 900  |        | 1350 |        | 1800 |        | 900  |  |   | f = 10 MHz |
| 12             | C <sub>iss</sub> Common-Source Input Capacitance           |        | 20   |        | 20   |        | 20   |        | 20   | pF   | V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 1 V                            |            |
| 13             | NF Noise Figure  |        | 3    |        | 3    |        | 4    |        | 1    |  | V <sub>DS</sub> = -5 V, I <sub>D</sub> = -1 mA<br>R <sub>gen</sub> = 1 MΩ |            |
| 14             | NF Noise Figure  |        |      |        |      |        |      |        | 5    | V <sub>DS</sub> = -5 V, I <sub>D</sub> = -1 mA<br>R <sub>gen</sub> = 10 MΩ |   | f = 10 Hz  |

\*JEDEC registered data

PC

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2.0 mW/°C

2N3329 2N3330 2N3331 2N3332

3

Siliconix

# n-channel JFETs designed for . . .



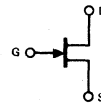
**Performance Curves NP**  
See Section 5

## ■ Small-Signal Low Power Applications

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|   |     |               |
|---|-----|---------------|
| Gate-Drain or Gate-Source Voltage (Note 1)  | ... | -40 V         |
| Gate Current                                | ... | 10 mA         |
| Total Device Dissipation at (or below) 25°C |     |               |
| Free-Air Temperature (Note 2)               | ... | 300 mW        |
| Storage Temperature Range                   | ... | -65 to +175°C |
| Maximum Operating Temperature               | ... | 150°C         |

TO-18  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                                  |                            | 2N3368       |  | 2N3369      |             | 2N3370    |                       | Unit | Test Conditions              |       |                              |                     |           |
|---|----------------------------|--------------|--|-------------|-------------|-----------|-----------------------|------|------------------------------|-------|------------------------------|---------------------|-----------|
|   |                            | Min          | Max                                    | Min         | Max         | Min       | Max                   |      |                              |       |                              |                     |           |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10 | S<br>T<br>A<br>T<br>I<br>C | IGSS         | Gate Reverse Current                   | -5          | -5          | -5        | -5                    | nA   | VGS = -30 V, VDS = 0         | 100°C |                              |                     |           |
|   |                            |              |  | -1.5        | -1.5        | -1.5      | -1.5                  | µA   |                              |       |                              |                     |           |
|   |                            | BVGSS        | Gate-Source Breakdown Voltage          | -40         | -40         | -40       | -40                   | V    | IG = -1 µA, VDS = 0          |       |                              |                     |           |
|   |                            | VGS(off)     | Gate-Source Cutoff Voltage             | -11.5       | -6.5        | -3.2      | -3.2                  | V    | VDS = 20 V, ID = 1 µA        |       |                              |                     |           |
| ID(off)   | Drain Cutoff Current       | 5<br>(-12.0) | 5<br>(-7.0)                            | 5<br>(-3.5) | 5<br>(-3.5) | nA<br>(V) | VDS = 20 V, VGS = ( ) |      |                              |       |                              |                     |           |
| IDSS  | Saturation Drain Current   | 2.0          | 12.0                                   | 0.5         | 2.5         | 0.1       | 0.6                   | mA   | VDS = 30 V (Note 3), VGS = 0 |       |                              |                     |           |
| D<br>Y<br>N<br>A<br>M<br>I<br>C                 |                            | gfs          | Common-Source Forward Transconductance | 1000        | 4000        | 600       | 2500                  | 300  | 2500                         | µmho  | VDS = 30 V (Note 3), VGS = 0 | f = 1 kHz           |           |
|   |                            | goss         | Common-Source Output Conductance       |             | 80          |           | 30                    |      | 15                           |       | pF                           | VDS = 30 V, VGS = 0 | f = 1 MHz |
|   |                            | Coss         | Common-Source Output Capacitance       |             | 3           |           | 3                     |      | 3                            |       |                              |                     |           |
|   |                            | Ciss         | Common-Source Input Capacitance        |             | 20          |           | 20                    |      | 20                           |       |                              |                     |           |

\*JEDEC registered data.

NP

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 150°C free-air temperature at rate of 2.1 mW/°C.
3. To minimize heating on high IDSS units, this parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

# p-channel JFETs designed for . . .



Performance Curves PE  
See Section 5

- Analog Switches
- Choppers
- Commutators
- Amplifiers

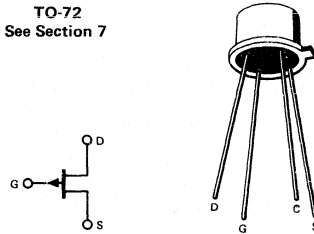
### BENEFITS

- Low Insertion Loss  
 $R_{DS(on)} < 150 \Omega$  (2N3386)

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|  |               |
|--|---------------|
| Gate-Drain Voltage (Note 1)              | 30 V          |
| Gate-Source Voltage (Note 1)             | 30 V          |
| Gate Current                             | 50 mA         |
| Storage Temperature Range                | -65 to +200°C |
| Total Dissipation at 25°C $T_A$ (Note 2) | 300 mW        |

TO-72  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  | 2N3382 |           | 2N3384 |           | 2N3386 |              | Unit      | Test Conditions                     |                                   |
|---|--------|-----------|--------|-----------|--------|--------------|-----------|-------------------------------------|-----------------------------------|
|   | Min    | Max       | Min    | Max       | Min    | Max          |           |                                     |                                   |
| 1   $I_{GSS}$   Gate Reverse Current  |        | 15        |        | 15        |        | 15           | nA        | $V_{GS} = 30 V$<br>$V_{DS} = 0$     |                                   |
| 2   $I_{GSS}$   Gate Reverse Current  |        | 15        |        | 15        |        | 15           | $\mu A$   | $V_{GS} = 5 V$<br>$V_{DS} = 0$      | $T_A = 150^\circ C$               |
| 3   $BV_{GSS}$   Gate-Source Breakdown Voltage                                | 30     |           | 30     |           | 30     |              | V         | $I_G = 1 \mu A$<br>$V_{DS} = 0$     |                                   |
| 4   $V_{GS(off)}$   Gate-Source Cutoff Voltage (Note 3)                       | 1.0    | 5.0       | 4.0    | 5.0       | 4.0    | 9.5          |           | $V_{DS} = -5 V$<br>$I_D = -1 \mu A$ |                                   |
| 5   $I_{DSS}$   Saturation Drain Current (Note 3)                             | -3.0   | -30.0     | -15.0  | -30.0     | -15.0  | -50.0        | mA        | $V_{DS} = -10 V$<br>$V_{GS} = 0$    |                                   |
| 6   $I_{D(off)}$   Drain Cutoff Current                                       |        | -2<br>(6) |        | -2<br>(6) |        | -2.5<br>(10) | nA<br>(V) | $V_{DS} = -5 V$<br>$V_{GS} = ( )$   |                                   |
| 7   $r_{ds(on)}$   Drain-Source ON Resistance                                 |        | 300       |        | 180       |        | 150          | $\Omega$  | $V_{GS} = 0$<br>$V_{DS} = 0$        | $f = 1 kHz$                       |
| 8   $g_{fs}$   Common-Source Forward Transconductance (Note 3)                | 4500   | 12,500    | 7500   | 12,500    | 7500   | 15,000       | $\mu mho$ | $V_{DS} = -10 V$<br>$V_{GS} = 0$    |                                   |
| 9   $C_{sgs} + C_{dgs}$   Source-Gate Capacitance Plus Drain-Gate Capacitance |        | 6.0       |        | 6.0       |        | 6.0          | pF        | $V_{DS} = 0$<br>$V_{GS} = 10 V$     | $f = 140 kHz$                     |
| 10   $C_{iss}$   Common-Source Input Capacitance                              | 16 Typ |           |        |           |        |              |           |                                     | $V_{DS} = -5 V$<br>$V_{GS} = 1 V$ |

\*JEDEC registered data.

PE

### NOTE:

1. Due to symmetrical geometry, units may be operated with source and drain leads interchanged.
2. Derate linearly to +175°C at 2 mW/°C
3. Pulswidth = 2 ms, duty cycle  $\leq 3\%$ .

2N3382 2N3384 2N3386

3

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NP**  
**See Section 5**

- **Small-Signal Amplifiers**
- **Switches**

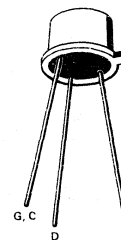
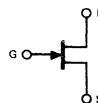
**BENEFITS**

- Operates from High Supply Voltages  
 $BV_{GSS} > 50 \text{ V}$

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -50 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at (or below) 25°C  
 Free-Air Temperature (Note 2) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C

**TO-18**  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic |          | 2N3436                                 |     | 2N3437 |                | 2N3438 |               | Unit      | Test Conditions               |           |  |
|----------------|----------|--|-----|--------|----------------|--------|---------------|-----------|-------------------------------|-----------|--|
|                |          | Min                                    | Max | Min    | Max            | Min    | Max           |           |                               |           |  |
| 1              | IGSS     | Gate Reverse Current                   |     |        | -0.5           |        | -0.5          | nA        | VGS = -30 V, VDS = 0<br>150°C |           |  |
|                |          |  |     |        | -1.0           |        | -1.0          | µA        |                               |           |  |
| 3              | BVGSS    | Gate-Source Breakdown Voltage          |     | -50    |                | -50    |               | V         | IG = -1 µA, VDS = 0           |           |  |
| 4              | ID(off)  | Drain Cutoff Current                   |     |        | 1.0<br>(-10.0) |        | 1.0<br>(-5.0) | nA<br>(V) | VDS = 20 V, VGS = ( )         |           |  |
| 5              | VGS(off) | Gate-Source Cutoff Voltage             |     |        | -9.8           |        | -4.8          | V         | VDS = 20 V, ID = 1 µA         |           |  |
| 6              | IDSS     | Saturation Drain Current               |     | 3.0    | 15.0           | 0.8    | 4.0           | 0.2       | 1.0                           | mA        | VDS = 20 V, VGS = 0  |
| 7              | gfs      | Common-Source Forward Transconductance |     | 2500   | 10,000         | 1500   | 6000          | 800       | 4500                          | µmho      | VDS = 20 V, VGS = 0<br>f = 1 kHz                             |
| 8              | goss     | Common-Source Output Conductance       |     |        | 35             |        | 20            |           | 5                             |           | VDS = 30 V, VGS = 0<br>f = 1 MHz                             |
| 9              | Coss     | Common-Source Output Capacitance       |     |        | 6              |        | 6             |           | 6                             | pF        |  |
| 10             | Ciss     | Common-Source Input Capacitance        |     |        | 18<br>(10)     |        | 18<br>(6)     |           | 18<br>(4)                     | pF<br>(V) |  |
| 11             | NF       | Noise Figure                           |     |        | 2              |        | 2             |           | 2                             | dB        | VDS = 10 V, VGS = 0,<br>Rgen = 1 meg, BW = 6 Hz<br>f = 1 kHz |

\*JEDEC Registered Data.

**NP**

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.



# n-channel JFETs designed for . . .



Performance Curves NP  
See Section 5

## ■ Small-Signal Low Noise Amplifiers

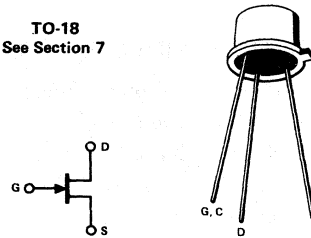
### BENEFITS

- Operates from High Supply Voltages  
 $BV_{GSS} > 50 \text{ V}$

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -50 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at (or below) 25°C  
 Free-Air Temperature (Note 2) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C

TO-18  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic             |                                 | 2N3458       |  | 2N3459 |           | 2N3460     |           | Unit      | Test Conditions       |           |   |                      |           |
|----------------------------|---------------------------------|--------------|--|--------|-----------|------------|-----------|-----------|-----------------------|-----------|---|----------------------|-----------|
|                            |                                 | Min          | Max                                    | Min    | Max       | Min        | Max       |           |                       |           |   |                      |           |
| 1<br>2<br>3<br>4<br>5<br>6 | S<br>T<br>A<br>T<br>I<br>C      | IGSS         | Gate Reverse Current                   |        | -0.25     | -0.25      | -0.25     | nA        | VGS = -30 V, VDS = 0  | 150°C     |   |                      |           |
|                            |                                 |              |  |        | -0.5      | -0.5       | -0.5      | µA        |                       |           |   |                      |           |
|                            |                                 | BVGSS        | Gate-Source Breakdown Voltage          |        | -50       | -50        | -50       | V         | IG = -1 µA, VDS = 0   |           |   |                      |           |
| 4                          | D<br>Y<br>N<br>A<br>M<br>I<br>C | ID(off)      | Drain Cutoff Current                   |        | 1<br>(-8) | 1<br>(-4)  | 1<br>(-2) | nA<br>(V) | VDS = 20 V, VGS = ( ) |           |   |                      |           |
| 5                          |                                 | VGS(off)     | Gate-Source Cutoff Voltage             |        | -7.8      | -3.4       | -1.8      | V         | VDS = 20 V, ID = 1 µA |           |   |                      |           |
| 6                          |                                 | IDSS         | Drain Current at Zero Gate Voltage     |        | 3.0       | 15.0       | 0.8       | 4.0       | 0.2                   | 1.0       | mA  | VDS = 20 V, VGS = 0  |           |
| 7                          | D<br>Y<br>N<br>A<br>M<br>I<br>C | gfs          | Common-Source Forward Transconductance |        | 2500      | 10,000     | 1500      | 6000      | 800                   | 4500      | µmho  | VDS = 20 V, VGS = 0  | f = 1 kHz |
| 8                          |                                 | goss         | Common-Source Output Conductance       |        |           | 35         |           | 20        |                       | 5         |   | VDS = 30 V, VGS = 0  | f = 1 MHz |
| 9                          |                                 | Coss         | Common-Source Output Capacitance       |        |           | 5          |           | 5         |                       | 5         | pF  |                      |           |
| 10                         |                                 | Ciss         | Common-Source Input Capacitance        |        |           | 18<br>(10) |           | 18<br>(6) |                       | 18<br>(4) | pF<br>(V)                                       | VGS = 0 V, VDS = ( ) | f = 1 MHz |
| 11                         | NF                              | Noise Figure |  |        | 6         |            | 4         |           | 4                     | dB        | VDS = 10 V, VGS = 0,<br>Rgen = 1 meg, BW = 6 Hz | f = 20 Hz            |           |

\* JEDEC registered data.

NP

NOTES:

- Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
- Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.

2N3458 2N3459 2N3460

3

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NFA**  
**See Section 5**

- **Low Noise Amplifiers**
- **Choppers**
- **Switches**

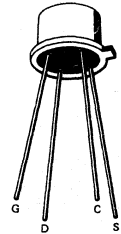
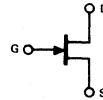
**BENEFITS**

- Operates from High Supply Voltages  
BV<sub>GSS</sub> > 50 V

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |     |               |
|---|-----|---------------|
| Gate-Drain or Gate-Source Voltage (Note 2)            | ... | -50 V         |
| Gate Current or Drain Current                         | ... | 50 mA         |
| Total Device Dissipation<br>(Derate 2 mW/°C to 175°C) | ... | 350 mW        |
| Storage Temperature Range                             | ... | -65 to +200°C |

**TO-72**  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic  | 2N3684 |      | 2N3685 |      | 2N3686 |      | 2N3687 |      | Unit   | Test Conditions   |            |
|---|--------|------|--------|------|--------|------|--------|------|--------|---|------------|
|   | Min    | Max  | Min    | Max  | Min    | Max  | Min    | Max  |        |   |            |
| 1   I <sub>GSS</sub>   Gate Reverse Current                             |        | -0.1 |        | -0.1 |        | -0.1 |        | -0.1 | nA     | V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0  | 150°C      |
| 2   |        | -0.5 |        | -0.5 |        | -0.5 |        | -0.5 | µA     |   |            |
| 3   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage                   | -50    |      | -50    |      | -50    |      | -50    |      | V      | I <sub>G</sub> = -1 µA, V <sub>DS</sub> = 0   |            |
| 4   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage                   | -2     | -5   | -1     | -3.5 | -0.6   | -2   | -0.3   | -1.2 |        | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA                                       |            |
| 5   I <sub>DSS</sub>   Saturation Drain Current                         | 2.5    | 7.5  | 1      | 3    | 0.4    | 1.2  | 0.1    | 0.5  | mA     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0   |            |
| 6   r <sub>DS(on)</sub>   Drain-Source ON Resistance (Note 1)           |        | 600  |        | 800  |        | 1200 |        | 2400 | ohm    | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 0  |            |
| 7   g <sub>fs</sub>   Common-Source Forward Transconductance            | 2000   | 3000 | 1500   | 2500 | 1000   | 2000 | 500    | 1500 | µmho   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0   | f = 1 kHz  |
| 8   g <sub>os</sub>   Common-Source Output Conductance                  |        | 50   |        | 25   |        | 10   |        | 5    |        |   |            |
| 9   C <sub>rss</sub>   Common-Source Reverse Transfer Capacitance       |        | 1.2  |        | 1.2  |        | 1.2  |        | 1.2  | pF     |   |            |
| 10   C <sub>iss</sub>   Common-Source Input Capacitance                 |        | 4    |        | 4    |        | 4    |        | 4    |        |   |            |
| 11   ē <sub>n</sub>   Equivalent Short Circuit Input Spot Noise Voltage |        | 0.15 |        | 0.15 |        | 0.15 |        | 0.15 | µV/√Hz | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0   | f = 20 Hz  |
| 12   NF   Noise Figure  |        | 0.5  |        | 0.5  |        | 0.5  |        | 0.5  | dB     | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0<br>R <sub>gen</sub> = 10 meg, BW = 6 Hz | f = 100 Hz |

\*JEDEC registered data

**NFA**

**NOTES:**

1. Not JEDEC registered data
2. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

# n-channel JFETs designed for . . .



**Performance Curves NRL**  
See Section 5

- **Small-Signal Amplifiers**
- **Oscillators**

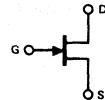
**BENEFITS**

- Operates from High Supply Voltages  
 $BV_{GSS} > 50 \text{ V}$

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |     |               |
|---|-----|---------------|
| Gate-Drain or Gate-Source Voltage (Note 1)  | ... | -50 V         |
| Gate Current                                | ... | 10 mA         |
| Total Device Dissipation at (or below) 25°C |     |               |
| Free-Air Temperature (Note 2)               | ... | 300 mW        |
| Storage Temperature Range                   | ... | -65 to +200°C |
| Lead Temperature                            | ... | 300°C         |
| (1/16" from case for 10 seconds)            |     |               |

TO-72  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | 2N3821  |                               | 2N3822 |      | Unit | Test Conditions |   |   |             |           |
|--|---|-------------------------------|--------|------|------|-----------------|---|---|-------------|-----------|
|  | Min   | Max                           | Min    | Max  |      |                 |   |   |             |           |
| 1<br>2<br>3<br>4<br>5<br>6<br>S<br>T<br>A<br>T<br>I<br>C   | IGSS  | Gate Reverse Current          |        | -0.1 | -0.1 | nA              | VGS = -30 V, VDS = 0<br>150°C   |   |             |           |
|  |   |                               |        | -0.1 | -0.1 | µA              |   |   |             |           |
| 7<br>8<br>9<br>10<br>11<br>D<br>Y<br>N<br>A<br>M<br>I<br>C | BVGS  | Gate-Source Breakdown Voltage |        | -50  | -50  | V               | IG = -1 µA, VDS = 0<br>VDS = 15 V, ID = 0.5 nA<br>VDS = 15 V, ID = 50 µA<br>VDS = 15 V, ID = 200 µA |   |             |           |
|  | VGS(off)  | Gate-Source Cutoff Voltage    |        | -4   | -6   |                 |   |   |             |           |
|  | VGS   | Gate-Source Voltage           |        | -0.5 | -2   |                 |   |   |             |           |
|  |   |                               |        | -1   | -4   |                 |   |   |             |           |
| IDSS   | Saturation Drain Current (Note 3)               |                               | 0.5    | 2.5  | 2    | 10              | mA  | VDS = 15 V, VGS = 0                             |             |           |
| 9fs  | Common-Source Forward Transconductance (Note 3) |                               | 1500   | 4500 | 3000 | 6500            | µmho  | VDS = 15 V, VGS = 0                             | f = 1 kHz   |           |
| vfs  | Common-Source Forward Transadmittance           |                               | 1500   |      | 3000 |                 |   |   | f = 100 MHz |           |
| 9os  | Common-Source Output Conductance (Note 3)       |                               |        | 10   |      | 20              |   |   | f = 1 kHz   |           |
| Ciss   | Common-Source Input Capacitance                 |                               |        | 6    |      | 6               |   |   | pF          | f = 1 MHz |
| Crss   | Common-Source Reverse Transfer Capacitance      |                               |        | 3    |      | 3               |   |   |             |           |
| NF   | Noise Figure                                    |                               |        | 5    |      | 5               | dB  | VDS = 15 V, VGS = 0,<br>Rgen = 1 meg, BW = 5 Hz | f = 10 Hz   |           |
| en   | Equivalent Short-Circuit Input Noise Voltage    |                               |        | 200  |      | 200             | nV/√Hz  | VDS = 15 V, VGS = 0, BW = 5 Hz                  |             |           |

**3**

\*JEDEC Registered Data.

**NRL**

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

**Siliconix**

**2N3821 2N3822**

# n-channel JFET designed for . . .



Performance Curves NRL  
See Section 5

- VHF Amplifiers
- Oscillators
- Mixers

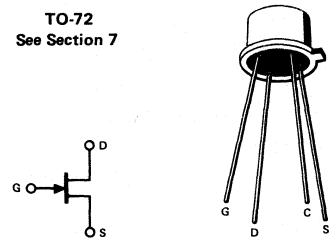
**BENEFITS**

- Low Noise  
NF < 2.5 dB @ 100 MHz

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -30 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at (or below) 25°C  
 Free-Air Temperature (Note 2) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature (1/16" From Case for 10 Sec) . . . 300°C

TO-72  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic             |   | Min   | Max   | Unit  | Test Conditions  |  |                    |   |
|----------------------------|---|---|-------|-------|--|--|--------------------|---|
| 1<br>2<br>3<br>4<br>5<br>6 | S<br>T<br>A<br>T<br>I<br>C                | I <sub>GSS</sub> Gate Reverse Current                       |       | -0.5  | nA   | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0         | 150°C              |   |
|                            |   | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | -30   |       |  |  |                    |   |
|                            |   | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage             |       | -8    |  | V  |                    | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.5 nA |
| 5                          | V <sub>GS</sub> Gate-Source Voltage       | -1.0  | -7.5  |       |  | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 400 μA      |                    |   |
| 6                          | I <sub>DSS</sub> Saturation Drain Current | 4   | 20    | mA    |  | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 3) |                    |   |
| 7                          | D<br>Y<br>N<br>A<br>M<br>I<br>C           | g <sub>fs</sub> Common-Source Forward Transconductance      | 3,500 | 6,500 | μmho   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0          | f = 1 kHz (Note 3) |   |
| 8                          |   | y <sub>fs</sub>   Common-Source Forward Transadmittance     | 3,200 |       |  |  | f = 200 MHz        |   |
| 9                          |   | g <sub>os</sub> Common-Source Output Conductance            |       | 35    |  |  | f = 1 kHz (Note 3) |   |
| 10                         |   | g <sub>iss</sub> Common-Source Input Conductance            |       | 800   |  |  | f = 200 MHz        |   |
| 11                         |   | g <sub>oss</sub> Common-Source Output Conductance           |       | 200   |  |  |                    |   |
| 12                         |   | C <sub>iss</sub> Common-Source Input Capacitance            |       | 6     |  |  | pF                 | f = 1 MHz                                       |
| 13                         |   | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |       | 2     |  |  |                    |   |
| 14                         | NF Noise Figure                           |   | 2.5   | dB    | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0<br>R <sub>G</sub> = 1 kΩ | f = 100 MHz  |                    |   |

\*JEDEC Registered Data

NRL

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

# n-channel JFET designed for . . .



**Performance Curves NRL**  
See Section 5

2N3824

- High Speed Commutators
- Choppers

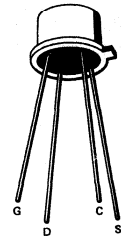
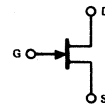
**BENEFITS**

- Low Insertion Loss  
 $r_{ds(on)} < 250 \Omega$
- High Off-Isolation  
 $I_{D(off)} < 0.1 \text{ nA}$

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |               |
|--|---------------|
| Gate-Drain or Gate-Source Voltage (Note 1)           | -50 V         |
| Gate Current   | 10 mA         |
| Total Device Dissipation at (or below) 25°C          |               |
| Free-Air Temperature (Note 2)                        | 300 mW        |
| Storage Temperature Range                            | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) | 300°C         |

TO-72  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                                 |  | Min | Max  | Unit          | Test Conditions   |
|--|--|-----|------|---------------|---|
| 1<br>2<br>3<br>4<br>S<br>T<br>A<br>T<br>I<br>C | $I_{GSS}$ Gate Reverse Current                       |     | -0.1 | nA            | $V_{GS} = -30 \text{ V}, V_{DS} = 0$<br>150°C           |
|  |  |     | -0.1 | $\mu\text{A}$ |   |
| 3  | $BV_{GSS}$ Gate-Source Breakdown Voltage             | -50 |      | V             | $I_G = -1 \mu\text{A}, V_{DS} = 0$                      |
| 4  | $I_{D(off)}$ Drain Cutoff Current                    |     | 0.1  | nA            | $V_{DS} = 15 \text{ V}, V_{GS} = -8 \text{ V}$<br>150°C |
|  |  |     | 0.1  | $\mu\text{A}$ |   |
| 5<br>D<br>Y<br>N<br>A<br>M<br>I<br>C           | $r_{ds(on)}$ Drain-Source ON Resistance              |     | 250  | $\Omega$      | $V_{GS} = 0 \text{ V}, I_D = 0$<br>f = 1 kHz            |
| 6  | $C_{iss}$ Common-Source Input Capacitance            |     | 6    | pF            | $V_{DS} = 15 \text{ V}, V_{GS} = 0$<br>f = 1 MHz        |
| 7  | $C_{rss}$ Common-Source Reverse Transfer Capacitance |     | 3    | pF            |   |

\*JEDEC registered data.

NRL

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

3

Siliconix

# p-channel JFET designed for . . .



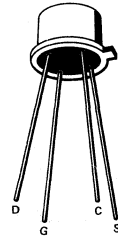
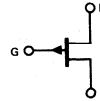
Performance Curves PC  
See Section 5

## ■ General Purpose Amplifiers

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 20 V  
 Drain-Source Voltage . . . . . -20 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at (or below)  
 25°C Free-Air Temperature (Note 2) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature 1/16" From Case For 10 Sec . . . . 300°C

TO-72  
See Section 7



### \* ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                  |  | 2N3909 |       | Unit | Test Conditions   |            |
|---------------------------------|--|--------|-------|------|---|------------|
|                                 |  | Min    | Max   |      |   |            |
| S<br>T<br>A<br>T<br>I<br>C      | 1   I <sub>GSS</sub>   Gate Reverse Current                        |        | 10    | nA   | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0<br><br>T = 100°C  |            |
|                                 | 2  |        | 1     | μA   |   |            |
|                                 | 3   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage              | 20     |       |      | I <sub>G</sub> = 10 μA, V <sub>DS</sub> = 0<br><br>V <sub>DS</sub> = -10 V, I <sub>D</sub> = -10 μA<br><br>V <sub>DS</sub> = -10 V, I <sub>D</sub> = -30 μA |            |
|                                 | 4   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage              |        | 8.0   | V    |   |            |
|                                 | 5   V <sub>GS</sub>   Gate-Source Voltage                          | 0.3    | 7.9   |      |   |            |
|                                 | 6   I <sub>DSS</sub>   Saturation Drain Current                    | -0.3   | -15   | mA   |   |            |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | 7   g <sub>fs</sub>   Common-Source Forward Transconductance       | 1,000  | 5,000 |      | V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0  |            |
|                                 | 8   g <sub>os</sub>   Common-Source Output Conductance             |        | 100   | μmho |   | f = 1 kHz  |
|                                 | 9    y <sub>fs</sub>     Common-Source Forward Transadmittance     | 900    |       |      |   | f = 10 MHz |
|                                 | 10   C <sub>iss</sub>   Common-Source Input Capacitance            |        | 32    | pF   |   | f = 1 MHz  |
|                                 | 11   C <sub>rss</sub>   Common-Source Reverse Transfer Capacitance |        | 16    |      |   |            |

\*JEDEC registered data

PC

**Notes**

- 1 Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
- 2 Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

# monolithic dual n-channel JFETs designed for . . .



2N3921 2N3922 2N4084 2N4085

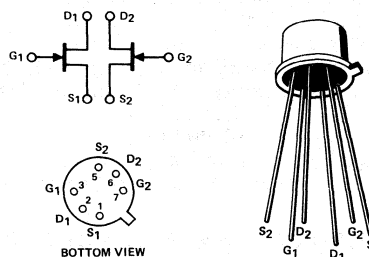
## ■ Differential Amplifiers

**Performance Curves NNR**  
See Section 5

### BENEFITS

- Minimum System Error and Calibration  
5 mV Offset Maximum (2N3921)
- Simplifies Amplifier Design  
Low Output Conductance

TO-71  
See Section 7



### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation  
 (Derate 1.7 mW/°C to 200°C) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C

### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic |   | Min  | Max  | Unit | Test Conditions                              |  |
|----------------|---|------|------|------|--|--|
| 1              | IGSS Gate Reverse Current                           |      | -1   | nA   | VGS = -30 V, VDS = 0<br>100°C                |  |
| 2              |   |      | -1   | µA   |  |  |
| 3              | BVDGO Drain-Gate Breakdown Voltage                  | 50   |      |      | ID = 1 µA, IS = 0                            |  |
| 4              | VGS(off) Gate-Source Cutoff Voltage                 |      | -3   | V    | VDS = 10 V, ID = 1 nA                        |  |
| 5              | VGS Gate-Source Voltage                             | -0.2 | -2.7 |      | VDS = 10 V, ID = 100 µA                      |  |
| 6              | IG Gate Operating Current                           |      | -250 | pA   | VDG = 10 V, ID = 700 µA<br>100°C             |  |
| 7              |   |      | -25  | nA   |  |  |
| 8              | IDSS Saturation Drain Current (Note 1)              | 1    | 10   | mA   | VDS = 10 V, VGS = 0                          |  |
| 9              | 9fs Common-Source Forward Transconductance (Note 1) | 1500 | 7500 | µmho | VDS = 10 V, VGS = 0<br>f = 1 kHz             |  |
| 10             | 9os Common-Source Output Conductance                |      | 35   |      |  |  |
| 11             | Ciss Common-Source Input Capacitance                |      | 18   | pF   |  |  |
| 12             | Crss Common-Source Reverse Transfer Capacitance     |      | 6    |      | VDG = 10 V, ID = 700 µA<br>f = 1 kHz         |  |
| 13             | 9fs Common-Source Forward Transconductance          | 1500 |      | µmho |  |  |
| 14             | 9os Common-Source Output Conductance                |      | 20   |      |  |  |
| 15             | NF Spot Noise Figure                                |      | 2    | dB   | VDS = 10 V, VGS = 0<br>f = 1 kHz, RG = 1 meg |  |

| Characteristic |  | 2N3921 |     | 2N3922 |     | 2N4084 |     | 2N4085 |     | Unit  | Test Conditions  |  |  |  |
|----------------|--|--------|-----|--------|-----|--------|-----|--------|-----|-------|--|--|--|--|
|                |  | Min    | Max | Min    | Max | Min    | Max | Min    | Max |       | VDG = 10 V, ID = 700 µA<br>TA = 0°C<br>TB = 100°C<br>f = 1 kHz |  |  |  |
| 16             | VGS1-VGS2  Differential Gate-Source Voltage  |        | 5   |        | 5   |        | 15  |        | 15  | mV    |  |  |  |  |
| 17             | $\frac{\Delta VGS1-VGS2 }{\Delta T}$ Gate-Source Differential Voltage Change with Temperature (Note 2) |        | 10  |        | 25  |        | 10  |        | 25  | µV/°C |  |  |  |  |
| 18             | $\frac{9fs1}{9fs2}$ Transconductance Ratio (Note 3)  | 0.95   | 1.0 | 0.95   | 1.0 | 0.95   | 1.0 | 0.95   | 1.0 | -     |  |  |  |  |

\*JEDEC registered data.

#### NOTES:

1. Pulse test duration = 2 ms.
2. Measured at end points, TA and TB.
3. Assumes smaller value in numerator.

NNR  
NRL-D

3

Siliconix

# matched dual n-channel JFETs designed for . . .



## Performance Curves NFA See Section 5

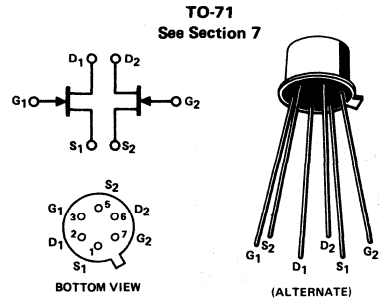
### BENEFITS

- High Accuracy & Stability  
Offset Less Than 5 mV (2N3954, 54A)  
Drift Less Than 5  $\mu\text{V}/^\circ\text{C}$  (2N3954A)
- Wide Dynamic Range  
 $I_G$  Specified @  $V_{DS} = 20\text{ V}$
- Low Capacitance  
 $C_{iss} < 4\text{ pF}$

- Low and Medium Frequency Differential Amplifiers
- High Input Impedance Amplifiers

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|   |                    |
|---|--------------------|
| Any Case-To-Lead Voltage . . . . .                          | $\pm 100\text{ V}$ |
| Gate-Drain or Gate-Source Voltage . . . . .                 | $-50\text{ V}$     |
| Gate-To-Gate Voltage . . . . .                              | $\pm 100\text{ V}$ |
| Gate Current . . . . .                                      | 50 mA              |
| Total Device Dissipation 85°C (Each Side) . . . . .         | 250 mW             |
| Case Temperature (Both Sides) . . . . .                     | 500 mW             |
| Power Derating (Each Side) . . . . .                        | 2.86 mW/°C         |
| (Both Sides) . . . . .                                      | 4.3 mW/°C          |
| Storage Temperature Range . . . . .                         | -65 to +125°C      |
| Lead Temperature (1/16" from case for 10 seconds) . . . . . | 300°C              |



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | 2N3954                                |  | 2N3954A |      | 2N3955 |      | 2N3955A |      | Unit | Test Conditions  |
|--|---------------------------------------|--|---------|------|--------|------|---------|------|------|--|
|  | Min                                   | Max  | Min     | Max  | Min    | Max  | Min     | Max  |      |  |
| 1   2   <b>S</b><br><b>T</b><br><b>A</b><br><b>T</b><br><b>I</b><br><b>C</b>                           | IGSS                                  | Gate Reverse Current                                     |         | -100 | -100   | -100 | -100    | -100 | pA   | VGS = -30 V,<br>VDS = 0<br>TA = 125°C  |
|  |                                       | Gate-Source Breakdown Voltage                            |         | -50  | -50    | -50  | -50     | -50  | nA   |  |
| 3   4   <b>D</b><br><b>N</b><br><b>A</b><br><b>M</b><br><b>I</b><br><b>C</b>                           | BVGS                                  | Gate-Source Cutoff Voltage                               |         | -1.0 | -4.5   | -1.0 | -4.5    | -1.0 | -4.5 | VDS = 0,<br>IG = -1 $\mu\text{A}$<br>VDS = 20 V,<br>ID = 1 nA<br>VDS = 0,<br>IG = 1 mA |
|  | VGS(off)                              | Gate-Source Forward Voltage                              |         | 2.0  | 2.0    | 2.0  | 2.0     | 2.0  | V    |  |
| 5   6   <b>D</b><br><b>N</b><br><b>A</b><br><b>M</b><br><b>I</b><br><b>C</b>                           | VGS(f)                                | Gate-Source Voltage                                      |         | -0.5 | -4.2   | -0.5 | -4.2    | -0.5 | -4.2 | VDS = 20 V<br>ID = 50 $\mu\text{A}$<br>ID = 200 $\mu\text{A}$                          |
|  | VGS                                   | Gate Operating Current                                   |         | -50  | -50    | -50  | -50     | -50  | pA   |  |
| 7   8   <b>D</b><br><b>N</b><br><b>A</b><br><b>M</b><br><b>I</b><br><b>C</b>                           | IG                                    | Saturation Drain Current                                 |         | -250 | -250   | -250 | -250    | -250 | nA   | VDS = 20 V,<br>ID = 200 $\mu\text{A}$<br>TA = 125°C                                    |
|  | IDSS                                  | 0.5  | 5.0     | 0.5  | 5.0    | 0.5  | 5.0     | 0.5  | 5.0  |  |
| 9   10   <b>D</b><br><b>N</b><br><b>A</b><br><b>M</b><br><b>I</b><br><b>C</b>                          | 11   12   $g_{fs}$                    | Common-Source Forward Transconductance                   |         | 1000 | 3000   | 1000 | 3000    | 1000 | 3000 | VDS = 20 V,<br>VGS = 0<br>f = 1 kHz<br>f = 200 MHz                                     |
|  |                                       | Common-Source Output Conductance                         |         | 35   | 35     | 35   | 35      | 35   | 35   |  |
| 13   14   <b>D</b><br><b>N</b><br><b>A</b><br><b>M</b><br><b>I</b><br><b>C</b>                         | 13   14   $g_{os}$                    | Common-Source Input Capacitance                          |         | 4.0  | 4.0    | 4.0  | 4.0     | 4.0  | pF   | VDS = 20 V,<br>VGS = 0<br>f = 1 kHz<br>f = 1 MHz                                       |
|  | 15   16   $C_{iss}$                   | Common-Source Reverse Transfer Capacitance               |         | 1.2  | 1.2    | 1.2  | 1.2     | 1.2  |      |  |
| 17   18   <b>D</b><br><b>N</b><br><b>A</b><br><b>M</b><br><b>I</b><br><b>C</b>                         | 17   18   $C_{rss}$                   | Drain-Gate Capacitance                                   |         | 1.5  | 1.5    | 1.5  | 1.5     | 1.5  | dB   | VDS = 20 V,<br>VGS = 0,<br>RG = 10 $\text{M}\Omega$<br>f = 100 Hz                      |
|  | 19   20   NF                          | Common Source Spot Noise Figure                          |         | 0.5  | 0.5    | 0.5  | 0.5     | 0.5  |      |  |
| 21   22   <b>M</b><br><b>A</b><br><b>T</b><br><b>C</b><br><b>H</b><br><b>I</b><br><b>N</b><br><b>G</b> | 18   19   $ I_{G1} - I_{G2} $         | Differential Gate Current                                |         | 10   | 10     | 10   | 10      | 10   | nA   | VDS = 20 V,<br>ID = 200 $\mu\text{A}$<br>T = 125°C                                     |
|  | 19   20   $I_{DSS1}/I_{DSS2}$         | Saturation Drain Current Ratio (Note 1)                  |         | 0.95 | 1.0    | 0.95 | 1.0     | 0.95 |      |  |
| 20   21   <b>M</b><br><b>A</b><br><b>T</b><br><b>C</b><br><b>H</b><br><b>I</b><br><b>N</b><br><b>G</b> | 20   21   $ V_{GS1} - V_{GS2} $       | Differential Gate-Source Voltage                         |         | 5.0  | 5.0    | 10.0 | 5.0     | 5.0  | mV   | VDS = 20 V,<br>ID = 200 $\mu\text{A}$<br>T = 25°C to -55°C<br>T = 25°C to 125°C        |
|  | 21   22   $\Delta V_{GS1} - V_{GS2} $ | Gate-Source Differential Voltage Change with Temperature |         | 0.8  | 0.4    | 2.0  | 1.2     | 1.5  |      |  |
| 23   24   $g_{fs1}/g_{fs2}$  | Transconductance Ratio (Note 1)       |  | 0.97    | 1.0  | 0.97   | 1.0  | 0.97    | 1.0  | -    | f = 1 kHz  |

\*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NFA



# matched dual n-channel JFETs designed for . . .



**Performance Curves NFA**  
See Section 5

- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

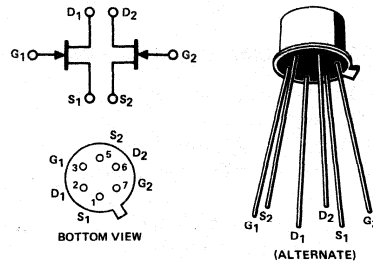
**BENEFITS**

- Wide Dynamic Range  
I<sub>G</sub> Specified @ V<sub>DS</sub> = 20 V
- Low Capacitance  
C<sub>iss</sub> < 4 pF

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |               |
|---|---------------|
| Any Lead-To-Case Voltage . . . . .                          | ±100 V        |
| Gate-Drain or Gate-Source Voltage . . . . .                 | -50 V         |
| Gate-To-Gate Voltage . . . . .                              | ±100 V        |
| Gate Current . . . . .                                      | 50 mA         |
| Total Device Dissipation 85°C (Each Side), . . . . .        | 250 mW        |
| Case Temperature (Both Sides) . . . . .                     | 500 mW        |
| Power Derating (Each Side) . . . . .                        | 2.86 mW/°C    |
| (Both Sides) . . . . .                                      | 4.3 mW/°C     |
| Storage Temperature Range . . . . .                         | -65 to +250°C |
| Lead Temperature (1/16" from case for 10 seconds) . . . . . | 300°C         |

**TO-71**  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic             | 2N3956                               |                      | 2N3957 |      | 2N3958 |      | Unit | Test Conditions |   |   |   |   |   |  |
|----------------------------|--------------------------------------|----------------------|--------|------|--------|------|------|-----------------|---|---|---|---|---|--|
|                            | Min                                  | Max                  | Min    | Max  | Min    | Max  |      |                 |   |   |   |   |   |  |
| S<br>T<br>A<br>T<br>I<br>C | 1                                    | I <sub>GSS</sub>     |        | -100 |        | -100 |      | -100            | pA  | V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0    | T <sub>A</sub> = 150°C  |   |   |  |
|                            | 2                                    |                      |        | -500 |        | -500 |      | -500            |   |   |   | V   | V <sub>DS</sub> = 0 V, I <sub>G</sub> = -1 μA |  |
|                            | 3                                    | BV <sub>GSS</sub>    | -50    |      | -50    |      | -50  |                 | V   | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA   |   |   |   |  |
|                            | 4                                    | V <sub>GS(off)</sub> | -1.0   | -4.5 | -1.0   | -4.5 | -1.0 | -4.5            |   |   | V   |   |   | V <sub>DS</sub> = 0 V, I <sub>G</sub> = 1 mA |
|                            | 5                                    | V <sub>GS(f)</sub>   |        | 2.0  |        | 2.0  |      | 2.0             |   |   |   |   |   |  |
|                            | 6                                    | V <sub>GS</sub>      |        | -4.2 |        | -4.2 |      | -4.2            | V   | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA |   |   |   |  |
|                            | 7                                    |                      | -0.5   | -4.0 | -0.5   | -4.0 | -0.5 | -4.0            |   |   | pA  | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA |   |  |
| 8                          | I <sub>G</sub>                       |                      | -50    |      | -50    |      | -50  | nA              | T <sub>A</sub> = 125°C                      |   |   |   |   |  |
| 9                          |                                      |                      | -250   |      | -250   |      | -250 |                 |   | mA  | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0                           |   |   |  |
| 10                         | I <sub>DSS</sub>                     | 0.5                  | 5.0    | 0.5  | 5.0    | 0.5  | 5.0  | μmho            | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 |   |   |   |   |  |
| 11                         | y <sub>fs</sub>                      | 1000                 | 3000   | 1000 | 3000   | 1000 | 3000 |                 |   | pF  | f = 1 kHz   |   |   |  |
| 12                         | g <sub>os</sub>                      |                      | 35     |      | 35     |      | 35   | pF              | f = 200 MHz                                 |   |   |   |   |  |
| 13                         | C <sub>iss</sub>                     |                      | 4.0    |      | 4.0    |      | 4.0  |                 |   | pF  | f = 1 kHz   |   |   |  |
| 14                         | C <sub>rss</sub>                     |                      | 1.2    |      | 1.2    |      | 1.2  | dB              | f = 1 MHz                                   |   |   |   |   |  |
| 15                         | C <sub>dgo</sub>                     |                      | 1.5    |      | 1.5    |      | 1.5  |                 |   | dB  | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, R <sub>G</sub> = 10 MΩ |   |   |  |
| 16                         | NF                                   |                      | 0.5    |      | 0.5    |      | 0.5  | nA              | f = 100 Hz                                  |   |   |   |   |  |
| 17                         | I <sub>G1</sub> -I <sub>G2</sub>     |                      | 10     |      | 10     |      | 10   |                 |   | -   | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA                       |   |   |  |
| 18                         | I <sub>DSS1</sub> /I <sub>DSS2</sub> | 0.95                 | 1.0    | 0.90 | 1.0    | 0.85 | 1.0  | mV              | T = 25°C to -55°C                           |   |   |   |   |  |
| 19                         | V <sub>GS1</sub> -V <sub>GS2</sub>   |                      | 15     |      | 20     |      | 25   |                 |   | mV  | T = 25°C to 125°C   |   |   |  |
| 20                         | Δ V <sub>GS1</sub> -V <sub>GS2</sub> |                      | 4.0    |      | 6.0    |      | 8.0  | -               | f = 1 kHz                                   |   |   |   |   |  |
| 21                         |                                      |                      | 5.0    |      | 7.5    |      | 10.0 |                 |   | -   | f = 1 kHz   |   |   |  |
| 22                         | g <sub>fs1</sub> /g <sub>fs2</sub>   | 0.95                 | 1.0    | 0.90 | 1.0    | 0.85 | 1.0  |                 |   |   |   |   |   |  |
| 23                         |                                      |                      |        |      |        |      |      |                 |   |   |   |   |   |  |

\*JEDEC registered data

**NOTE:**

1. Assumes smaller value in numerator.

**NFA**

2N3956 2N3957 2N3958

3

Siliconix

# n-channel JFET designed for . . .



## Performance Curves NH See Section 5

- Analog Switches
- Choppers
- Commutators

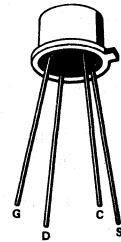
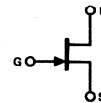
### BENEFITS

- Low Insertion Loss, No Offset Voltage  
 $R_{DS(on)} < 220 \Omega$
- Short Switching Aperture Times  
 $C_{rss} < 1.5 \text{ pF}$   
 $t_{(on)} + t_{(off)} < 50 \text{ ns Typical}$

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|   |                    |
|---|--------------------|
| Gate-Drain or Gate-Source Voltage                       | .....-30 V         |
| Gate Current  | ..... 10 mA        |
| Total Device Dissipation<br>(25°C Free-Air Temperature) | ..... 300 mW       |
| Power Derating  | ..... 1.7 mW/°C    |
| Storage Temperature Range                               | .....-55 to +200°C |
| Operating Temperature Range                             | .....-55 to +175°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)    | .....300°C         |

TO-72  
See Section 7



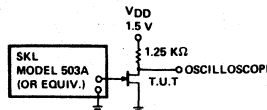
### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic |  | Min | Typ  | Max  | Unit          | Test Conditions  |
|----------------|--|-----|------|------|---------------|--|
| 1              | $I_{GSS}$ Gate Reverse Current                       |     |      | -0.1 | nA            | $V_{GS} = -20 \text{ V}, V_{DS} = 0$   |
| 2              | $V_{GS(off)}$ Gate-Source Cutoff Voltage             | -4  |      | -6.0 | V             | $V_{DS} = 10 \text{ V}, I_D = 10 \text{ nA}$   |
| 3              | $BV_{GSS}$ Gate-Source Breakdown Voltage             | -30 |      |      |               | $I_G = -1 \mu\text{A}, V_{DS} = 0$   |
| 4              | $I_{DSS}$ Saturation Drain Current (Note 1)          | 2.0 |      |      | mA            | $V_{DS} = 20 \text{ V}, V_{GS} = 0$  |
| 5              | $I_{D(off)}$ Drain Cutoff Current                    |     |      | 1.0  | nA            | $V_{DS} = 10 \text{ V}, V_{GS} = -7 \text{ V}$<br>$T_A = 150^\circ\text{C}$  |
| 6              |  |     |      | 2.0  | $\mu\text{A}$ |  |
| 7              | $r_{DS(on)}$ Static Drain-Source ON Resistance       |     |      | 220  | $\Omega$      | $V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0$  |
| 8              | $V_{DS(on)}$ Drain-Source ON Voltage                 |     |      | 0.25 | V             | $I_D = 1 \text{ mA}, V_{GS} = 0$   |
| 9              | $I_{DGO}$ Drain Reverse Current                      |     |      | 0.1  | nA            | $V_{DG} = 20 \text{ V}, I_S = 0$<br>$T_A = 150^\circ\text{C}$  |
| 10             |  |     |      | 0.2  | $\mu\text{A}$ |  |
| 11             | $r_{ds(on)}$ Drain-Source ON Resistance              |     |      | 220  | $\Omega$      | $V_{GS} = 0, I_D = 0$<br>$f = 1 \text{ kHz}$   |
| 12             | $C_{iss}$ Common-Source Input Capacitance            |     | 3.1  | 6.0  | pF            | $V_{DS} = 20 \text{ V}, V_{GS} = 0$<br>$f = 1 \text{ MHz}$   |
| 13             | $C_{rss}$ Common-Source Reverse Transfer Capacitance |     | 0.8  | 1.5  |               | $V_{DS} = 0, V_{GS} = -7 \text{ V}$  |
| 14             | $t_{d(on)}$ Turn ON Delay Time                       |     | 3.0  | 20   | ns            | $V_{DD} = 1.5 \text{ V}$<br>$I_{D(on)} = 1.0 \text{ mA}$<br>$V_{GS(on)} = 0$<br>$V_{GS(off)} = -6 \text{ V}$<br>$R_L = 1.25\text{k} \Omega$<br>See Circuit Below |
| 15             | $t_r$ Rise Time                                      |     | 10.0 | 100  |               |  |
| 16             | $t_{off}$ Turn OFF Time                              |     | 30.0 | 100  |               |  |
| 17             | $t_{d(off)}$ Turn OFF Delay Time (Note 2)            |     | 10.0 |      |               |  |
| 18             | $t_f$ Fall Time (Note 2)                             |     | 20.0 |      |               |  |

\* JEDEC registered parameters unless otherwise noted (apply to min/max only).

**NOTES:**

- Pulse test duration  $\leq 2 \text{ ms}$ .
- Non-JEDEC registered parameters:  
 $t_{d(off)} + t_f = t_{off}$ .



**NH**

INPUT PULSE  
RISE TIME < 1 ns  
FALL TIME < 1 ns  
PULSE WIDTH 1 ns  
PULSE DUTY CYCLE 50%  
INPUT RESISTANCE 50  $\Omega$

SAMPLING SCOPE  
RISE TIME < 10 ns  
FALL TIME < 10 ns  
INPUT RESISTANCE > 5 M $\Omega$  @ < 10 pF

# n-channel JFETs designed for . . .



Performance Curves NC  
See Section 5

- Analog Switches
- Choppers
- Amplifiers

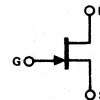
### BENEFITS

- Low Insertion Loss  
 $R_{DS(on)} < 30 \Omega$  (2N3970)
- Good Off-Isolation  
 $I_{D(off)} < 250 \text{ pA}$

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . -40 V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Case Temperature  
 (Note 1) . . . . . 1.8 W  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature  
 (1/16" from case for 60 seconds) . . . . . 300°C

TO-18  
See Section 7



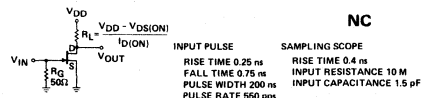
### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | 2N3970 |     | 2N3971 |     | 2N3972 |     | Unit | Test Conditions   |                        |
|--|--------|-----|--------|-----|--------|-----|------|---|------------------------|
|  | Min    | Max | Min    | Max | Min    | Max |      |   |                        |
| 1 BV <sub>GSS</sub> Gate Reverse Breakdown Voltage                               | -40    |     | -40    |     | -40    |     | V    | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0   |                        |
| 2 I <sub>DGO</sub> Drain Reverse Current   |        | 250 |        | 250 |        | 250 | pA   | V <sub>DG</sub> = 20 V, I <sub>S</sub> = 0  |                        |
| 3 I <sub>D(off)</sub> Drain Cutoff Current                                       |        | 500 |        | 500 |        | 500 | nA   |   |                        |
| 4 I <sub>D(off)</sub> Drain Cutoff Current                                       |        | 250 |        | 250 |        | 250 | pA   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = -12 V   |                        |
| 5 I <sub>D(off)</sub> Drain Cutoff Current                                       |        | 500 |        | 500 |        | 500 | nA   |   |                        |
| 6 V <sub>GS(off)</sub> Gate-Source Cutoff Voltage                                | -4     | -10 | -2     | -5  | -0.5   | -3  | V    | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA   |                        |
| 7 I <sub>DSS</sub> Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%) | 50     | 150 | 25     | 75  | 5      | 30  | mA   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0   |                        |
| 8 V <sub>DS(on)</sub> Drain-Source ON Voltage                                    |        |     |        | 1.5 |        |     | V    | V <sub>GS</sub> = 0   |                        |
| 9 V <sub>DS(on)</sub> Drain-Source ON Voltage                                    |        |     |        |     |        | 2   |      |   | I <sub>D</sub> = 5 mA  |
| 10 V <sub>DS(on)</sub> Drain-Source ON Voltage                                   |        | 1   |        |     |        |     |      |   | I <sub>D</sub> = 10 mA |
| 11 r <sub>DS(on)</sub> Static Drain-Source ON Resistance                         |        | 30  |        | 60  |        | 100 | Ω    | V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA  |                        |
| 12 r <sub>ds(on)</sub> Drain-Source ON Resistance                                |        | 30  |        | 60  |        | 100 | Ω    | V <sub>GS</sub> = 0, I <sub>D</sub> = 0   |                        |
| 13 C <sub>iss</sub> Common-Source Input Capacitance                              |        | 25  |        | 25  |        | 25  | pF   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0   |                        |
| 14 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance                   |        | 6   |        | 6   |        | 6   | pF   | V <sub>DS</sub> = 0, V <sub>GS</sub> = -12 V  |                        |
| 15 t <sub>d(on)</sub> Turn-On Delay Time   |        | 10  |        | 15  |        | 40  | ns   | V <sub>DD</sub> = 10 V, V <sub>GS(on)</sub> = 0<br>I <sub>D(on)</sub> R <sub>L</sub> V <sub>GS(off)</sub> |                        |
| 16 t <sub>r</sub> Rise Time  |        | 10  |        | 15  |        | 40  |      |   |                        |
| 17 t <sub>off</sub> Turn-Off Time  |        | 30  |        | 60  |        | 100 |      |   |                        |

\*JEDEC registered data.

**NOTE:**

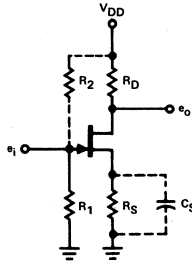
1. Derate linearly at the rate of 10 mW/°C.



2N3970 2N3971 2N3972

3

Siliconix



Amplifier Design Chart  
( $C_S$  for 3 dB Point at 50 Hz)

| V <sub>DD</sub><br>(V)                        | R <sub>S</sub><br>(Ω) | R <sub>1</sub><br>(MΩ) | R <sub>2</sub><br>(MΩ) | C <sub>S</sub><br>(μF) | I <sub>DD</sub><br>(mA) | R <sub>D</sub><br>(Ω) | e <sub>o</sub> Max<br>(V) | A <sub>V</sub> |
|---|-----------------------|------------------------|------------------------|------------------------|-------------------------|-----------------------|---------------------------|----------------|
| <b>2N3970</b>                                 |                       |                        |                        |                        |                         |                       |                           |                |
| 30  | 560                   | 1                      | ∞                      | 100                    | 11                      | 1K                    | 3                         | 9              |
|   | 2.7K                  | 3.3                    | 10                     | 100                    | 6                       | 1K                    | 2.5                       | 8              |
| V <sub>DD</sub> = 15<br>V <sub>SS</sub> = -15 | 3K                    | 1                      | Source<br>Follower     |                        | 7                       | 0                     | 8.5                       | 0.96           |
|   | 7.5K                  | 1                      |                        |                        | 6                       | 0                     | 8.5                       | 0.96           |
| V <sub>DD</sub> = 15<br>V <sub>SS</sub> = -15 | 7.5K                  | 1                      | Source<br>Follower     |                        | 6                       | 0                     | 15                        | 0.97           |
| <b>2N3971</b>                                 |                       |                        |                        |                        |                         |                       |                           |                |
| 20  | 2K                    | 4.7                    | 11                     | 100                    | 5                       | 1K                    | 1.5                       | 8-11           |
|   | 330                   | 1                      | ∞                      | 100                    | 8                       | 820                   | 1.5                       | 9              |
|   | 330                   | 1                      | ∞                      | 0                      | 8                       | 820                   | 3                         | 1.9            |
| 30  | 2K                    | 4.7                    | 11                     | 100                    | 6                       | 2.7K                  | 5                         | 18-24          |
|   | 330                   | 1                      | ∞                      | 100                    | 8                       | 1.5K                  | 2.5                       | 15             |
|   | 330                   | 1                      | ∞                      | 0                      | 8                       | 1.5K                  | 5.5                       | 3.3            |
| V <sub>DD</sub> = 15<br>V <sub>SS</sub> = -15 | 4.7K                  | 1                      | Source<br>Follower     |                        | 5                       | 0                     | 11                        | 0.97           |
| <b>2N3972</b>                                 |                       |                        |                        |                        |                         |                       |                           |                |
| 10  | 220                   | 1                      | ∞                      | 0                      | 5                       | 1.2K                  | 1.5                       | 3.5            |
| 20  | 220                   | 1                      | ∞                      | 0                      | 5                       | 2.2K                  | 3.5                       | 7              |
| 30  | 1K                    | 1                      | 12                     | 100                    | 4                       | 3.9K                  | 5                         | 38             |
|   | 1K                    | 1                      | 12                     | 100                    | 4                       | 5.6K                  | 3.5                       | 40-55          |
| V <sub>DD</sub> = 15<br>V <sub>SS</sub> = -15 | 4.7K                  | 1                      | Source<br>Follower     |                        | 2.5                     | 0                     | 13                        | 0.98           |
|   | 7.5K                  | 1                      |                        |                        | 1.5                     | 0                     | 13                        | 0.98           |

# n-channel JFETs designed for . . .



- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

## Performance Curves NC See Section 5

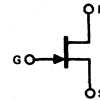
### BENEFITS

- Low Insertion Loss  
High Accuracy in Test Systems  
 $R_{ON} < 30 \Omega$  (2N4091)
- High Off-Isolation  
 $I_{D(off)} < 200 \text{ pA}$
- High Speed  
 $t_{rise} < 10 \text{ ns}$  (2N4091)
- Short Sample and Hold Aperture Time  
 $C_{rss} < 5 \text{ pF}$

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . -40 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at 25°C Case Temperature  
 (Derate 10 mW/°C) . . . . . 1.8 W  
 Storage Temperature Range . . . . . -55 to +200°C  
 Lead Temperature  
 (1/16" from case for 60 seconds) . . . . . 300°C

TO-18  
See Section 7



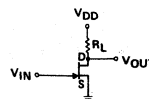
### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                                     | 2N4091                |     | 2N4092 |     | 2N4093 |     | Unit   | Test Conditions                                |                         |                |
|--|-----------------------|-----|--------|-----|--------|-----|--------|--|-------------------------|----------------|
|  | Min                   | Max | Min    | Max | Min    | Max |        |  |                         |                |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage  | -40                   |     | -40    |     | -40    |     | V      | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0    |                         |                |
| 2 IDGO Drain Reverse Current                       |                       | 200 |        | 200 |        | 200 | pA     | V <sub>GS</sub> = -20 V, I <sub>S</sub> = 0    |                         |                |
| 3  |                       | 400 |        | 400 |        | 400 | nA     | 150°C  |                         |                |
| 4 ID(off) Drain Cutoff Current                     |                       |     |        |     |        | 200 | pA     | V <sub>DS</sub> = 20 V                         | V <sub>GS</sub> = -6 V  | 150°C          |
|  |                       |     |        |     |        | 400 | nA     |  |                         |                |
|  |                       |     |        |     |        | 200 | pA     |  | V <sub>GS</sub> = -8 V  | 150°C          |
|  |                       |     |        |     |        | 400 | nA     |  |                         |                |
|  |                       |     | 200    |     |        |     | pA     |  | V <sub>GS</sub> = -12 V | 150°C          |
|  |                       | 400 |        |     |        | nA  |        |  |                         |                |
| 10 VGS(off) Gate-Source Cutoff Voltage             | -5                    | -10 | -2     | -7  | -1     | -5  | V      | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA  |                         |                |
| 11 IDSS Saturation Drain Current (Note 1)          | 30                    |     | 15     |     | 8      |     | mA     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0    |                         |                |
| 12 VDS(on) Drain-Source ON Voltage                 |                       |     |        | 0.2 |        | 0.2 | V      | V <sub>GS</sub> = 0                            | I <sub>D</sub> = 2.5 mA |                |
|  |                       |     |        |     |        |     |        |  | I <sub>D</sub> = 4 mA   |                |
|  |                       |     | 0.2    |     |        |     |        |  | I <sub>D</sub> = 6.6 mA |                |
| 15 rDS(on) Static Drain-Source ON Resistance       |                       | 30  |        | 50  |        | 80  | Ω      | V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA     |                         |                |
| 16 rds(on) Drain-Source ON Resistance              |                       | 30  |        | 50  |        | 80  | Ω      | V <sub>GS</sub> = 0, I <sub>D</sub> = 0        |                         |                |
| 17 Ciss Common-Source Input Capacitance            |                       | 16  |        | 16  |        | 16  | pF     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0    |                         |                |
| 18 Crss Common-Source Reverse Transfer Capacitance |                       | 5   |        | 5   |        | 5   |        | V <sub>DS</sub> = 0, V <sub>GS</sub> = -20 V   |                         |                |
| 19  td(on)  Turn-ON Delay Time                     |                       | 15  |        | 15  |        | 20  | ns     | V <sub>DD</sub> = 3 V, V <sub>GS(on)</sub> = 0 |                         |                |
|  | 20 tr Rise Time       |     | 10     |     | 20     |     |        | I <sub>D(on)</sub>                             | V <sub>GS(off)</sub>    | R <sub>L</sub> |
|  | 21 toff Turn-OFF Time |     | 40     |     | 60     |     |        | 2N4091   | -12 V                   | 425 Ω          |
|  |                       |     |        |     |        |     | 2N4092 | -8   | 700                     |                |
|  |                       |     |        |     |        |     | 2N4093 | -6   | 1120                    |                |

\*JEDEC registered data.

#### NOTE:

1. Pulewidth = 300 μs, duty cycle ≤ 3%.



#### INPUT PULSE

RISE TIME < 1 ns  
 FALL TIME < 1 ns  
 PULSE WIDTH 1 μs  
 PULSE DUTY CYCLE < 10%  
 PULSE GENERATOR IMPEDANCE 50Ω

#### SAMPLING SCOPE

RISE TIME 0.4 ns  
 INPUT RESISTANCE 10 MΩ  
 INPUT CAPACITANCE 1.7 pF

2N4091 2N4092 2N4093

3

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NT**  
See Section 5

■ **Ultra-High Input Impedance Amplifiers**

**Electrometers  
pH Meters  
Smoke Detectors**

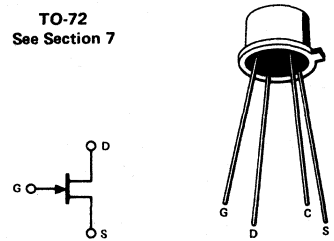
**BENEFITS**

- Low Power  
     $I_{DSS} < 90 \mu A$  (2N4117)
- Minimum Circuit Loading  
     $I_{GSS} < 1 pA$  (2N4117A Series)

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -40 V  
 Gate-Current . . . . . 50 mA  
 Total Device Dissipation  
 (Derate 2 mW/°C to 175°C) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +175°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 255°C

**TO-72**  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

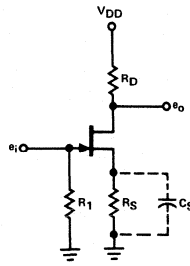
|                                 | Characteristic   | 2N4117<br>2N4117A |      | 2N4118<br>2N4118A |      | 2N4119<br>2N4119A |      | Unit | Test Conditions                               |           |
|---------------------------------|--|-------------------|------|-------------------|------|-------------------|------|------|---|-----------|
|                                 |  | Min               | Max  | Min               | Max  | Min               | Max  |      |   |           |
| S<br>T<br>A<br>T<br>I<br>C      | I <sub>GSS</sub> Gate Reverse Current<br>2N4117 Series Only        |                   | -10  |                   | -10  |                   | -10  | pA   | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0  |           |
|                                 |  |                   | -25  |                   | -25  |                   | -25  |      |   | 150°C     |
|                                 | I <sub>GSS</sub> Gate Reverse Current<br>2N4117A Series Only       |                   | -1   |                   | -1   |                   | -1   | pA   | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0  |           |
|                                 |  |                   | -2.5 |                   | -2.5 |                   | -2.5 |      |   | 150°C     |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | BV <sub>GSS</sub> Gate-Source Breakdown Voltage                    | -40               |      | -40               |      | -40               |      | V    | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0   |           |
|                                 | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage                    | -0.6              | -1.8 | -1                | -3   | -2                | -6   |      | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA |           |
| 7                               | I <sub>DSS</sub> Saturation Drain Current<br>(Note 2)              | 0.03              | 0.09 | 0.08              | 0.24 | 0.20              | 0.60 | mA   | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0   |           |
| 8                               | g <sub>fs</sub> Common-Source Forward<br>Transconductance (Note 2) | 70                | 210  | 80                | 250  | 100               | 330  | μmho | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0   |           |
| 9                               | g <sub>os</sub> Common-Source Output<br>Conductance                |                   | 3    |                   | 5    |                   | 10   |      |   | f = 1 kHz |
| 10                              | C <sub>iss</sub> Common-Source Input<br>Capacitance                |                   | 3    |                   | 3    |                   | 3    |      |   | pF        |
| 11                              | C <sub>rss</sub> Common-Source Reverse Transfer<br>Capacitance     |                   | 1.5  |                   | 1.5  |                   | 1.5  |      |   |           |

\*JEDEC registered data.

**NT**

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)



Amplifier Design Chart

| V <sub>DD</sub> (V)                            | R <sub>S</sub> (kΩ) | C <sub>S</sub>  | I <sub>DD</sub> (μA) | R <sub>D</sub> (kΩ) | e <sub>o</sub> Max (pK V) | A <sub>V</sub> |
|--|---------------------|-----------------|----------------------|---------------------|---------------------------|----------------|
| <b>2N4117</b>                                  |                     |                 |                      |                     |                           |                |
| 10   | 10                  |                 | 45                   | 120                 | 1                         | 5.7            |
| 20   | 10                  |                 | 45                   | 270                 | 1.5                       | 12             |
|  |                     |                 |                      | 360                 | 1                         | 15             |
| 30   | 10                  |                 | 45                   | 420                 | 4                         | 17             |
|  |                     |                 |                      | 620                 | 1                         | 22             |
| V <sub>DD</sub> = +15<br>V <sub>SS</sub> = -15 | 510                 | Source Follower | 35                   | 0                   | 8                         | 0.97           |
| <b>2N4118</b>                                  |                     |                 |                      |                     |                           |                |
| 10   | 8.2                 |                 | 120                  | 36                  | 0.6                       | 2.2            |
|  |                     |                 |                      | 50                  | 0.2                       | 3.5            |
| 20   | 8.2                 |                 | 120                  | 120                 | 1                         | 7.5            |
| 30   | 8.2                 |                 | 120                  | 180                 | 2                         | 10             |
| V <sub>DD</sub> = +15<br>V <sub>SS</sub> = -15 | 510                 | Source Follower | 35                   | 0                   | 8                         | 0.97           |
| <b>2N4119</b>                                  |                     |                 |                      |                     |                           |                |
| 20   | 56                  | 5 μF*<br>at 5 V | 70                   | 150                 | 1                         | 10             |
| 30   | 56                  |                 | 70                   | 240                 | 3                         | 17             |
|  |                     |                 | 330                  | 1                   | 17-23                     |                |
| 20   | 6.8                 |                 | 300                  | 27                  | 1                         | 1.8            |
| 30   | 6.8                 |                 | 300                  | 68                  | 2                         | 4.5            |
| V <sub>DD</sub> = +15<br>V <sub>SS</sub> = -15 | 510                 | Source Follower | 40                   | 0                   | 10                        | 0.97           |

\*AC Amplifier

2N4220 2N4220A 2N4221 2N4221A 2N4222 2N4222A

# n-channel JFETs designed for . . .



Performance Curves NRL  
See Section 5

- Small-Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers

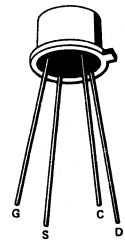
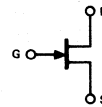
**BENEFITS**

- High Gain
- Low Receiver Noise Figure

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |               |
|--|---------------|
| Gate-Drain or Gate-Source Voltage (Note 1) . . . . .                                   | -30 V         |
| Gate Current . . . . .   | 10 mA         |
| Drain Current . . . . .  | 15 mA         |
| Total Device Dissipation at (or below) 25°C<br>Free-Air Temperature (Note 2) . . . . . | 300 mW        |
| Storage Temperature Range . . . . .  | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) . . . . .                         | 300°C         |

TO-72  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic  | 2N4220,<br>2N4220A              |          | 2N4221,<br>2N4221A                                 |     | 2N4222,<br>2N4222A |              | Units       | Test Conditions |   |             |      |                                     |             |
|---|---------------------------------|----------|--|-----|--------------------|--------------|-------------|-----------------|---|-------------|------|-------------------------------------|-------------|
|   | Min                             | Max      | Min  | Max | Min                | Max          |             |                 |   |             |      |                                     |             |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12 | S<br>T<br>A<br>T<br>I<br>C      | IGSS     | Gate Reverse Current                               |     | -0.1               | -0.1         | -0.1        | nA              | VGS = -15 V, VDS = 0<br>150°C                   |             |      |                                     |             |
|   |                                 |          |  |     |                    |              |             | μA              |   |             |      |                                     |             |
|   |                                 | BVGSS    | Gate-Source Breakdown Voltage                      |     | -30                | -30          | -30         | V               | IG = -10 μA, VDS = 0<br>VDS = 15 V, ID = 0.1 nA |             |      |                                     |             |
|   |                                 | VGS(off) | Gate-Source Cutoff Voltage                         |     | -4                 | -6           | -8          | V               |   |             |      |                                     |             |
|   |                                 | VGS      | Gate-Source Voltage                                |     | -0.5<br>(50)       | -2.5<br>(50) | -1<br>(200) | -5<br>(500)     | -2<br>(500)                                     | -6<br>(500) | V    | VDS = 15 V, ID = ( )                |             |
|   |                                 | IDSS     | Saturation Drain Current<br>(Note 3)               |     | 0.5                | 3            | 2           | 6               | 5   | 15          | mA   | VDS = 15 V, VGS = 0                 |             |
|   | D<br>Y<br>N<br>A<br>M<br>I<br>C | gfs      | Common-Source Forward<br>Transconductance (Note 3) |     | 1000               | 4000         | 2000        | 5000            | 2500  | 6000        | μmho | VDS = 15 V, VGS = 0                 | f = 1 kHz   |
|   |                                 | yfs      | Common-Source Forward<br>Transadmittance           |     | 750                |              | 750         |                 | 750   |             | μmho |                                     | f = 100 MHz |
|   |                                 | gos      | Common-Source Output<br>Conductance (Note 3)       |     |                    | 10           |             | 20              |   | 40          | μmho |                                     | f = 1 kHz   |
|   |                                 | Ciss     | Common-Source Input<br>Capacitance                 |     |                    | 6            |             | 6               |   | 6           | pF   |                                     | f = 1 MHz   |
|   |                                 | Crss     | Common-Source Reverse Transfer<br>Capacitance      |     |                    | 2            |             | 2               |   | 2           | pF   |                                     | f = 1 MHz   |
|   |                                 | NF       | Noise Figure, Only 2N4220A,<br>2N4221A, 2N4222A    |     |                    | 2.5          |             | 2.5             |   | 2.5         | dB   | VDS = 15 V, VGS = 0<br>Rgen = 1 meg | f = 100 Hz  |

\*JEDEC registered data.

NRL

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

Siliconix



# n-channel JFETs designed for . . .



Performance Curves NRL  
See Section 5

- VHF Amplifiers
- Mixers

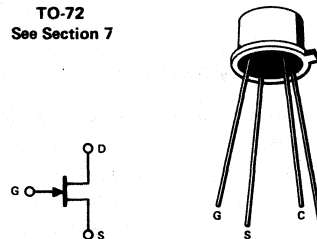
### BENEFITS

- Low Noise  
NF = 3 dB Typical @ 200 MHz
- Easy Tuning  
 $C_{rss} < 2$  pF

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -30 V  
 Gate Current . . . . . 10 mA  
 Drain Current . . . . . 20 mA  
 Total Device Dissipation at (or below) 25°C  
 Free-Air Temperature (Note 2) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-72  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic             |  | 2N4223         |               | 2N4224        |  | Unit      | Test Conditions                              |             |
|----------------------------|--|----------------|---------------|---------------|--|-----------|--|-------------|
|                            |  | Min            | Max           | Min           | Max  |           |  |             |
| S<br>T<br>A<br>T<br>I<br>C | 1   I <sub>GSS</sub>   Gate Reverse Current                              |                | -0.25         |               | -0.5   | nA        | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 | 150°C       |
|                            | 2   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage                    | -30            |               | -30           |  | V         |  |             |
|                            | 3   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage                    | -0.1<br>(0.25) | -8<br>(0.25)  | -0.1<br>(0.5) | -8<br>(0.5)  | V<br>(nA) | I <sub>G</sub> = -10 μA, V <sub>DS</sub> = 0 |             |
| D<br>Y<br>N                | 4   V <sub>GS</sub>   Gate-Source Voltage                                | -1.0<br>(0.3)  | -7.0<br>(0.3) | -1.0<br>(0.2) | -7.5<br>(0.2)  | V<br>(mA) | V <sub>DS</sub> = 15 V, I <sub>D</sub> = ( ) |             |
|                            | 5   I <sub>DSS</sub>   Saturation Drain Current (Note 3)                 | 3              | 18            | 2             | 20   | mA        |  |             |
| H<br>I<br>G<br>H           | 7   g <sub>fs</sub>   Common-Source Forward Transconductance (Note 3)    | 3000           | 7000          | 2000          | 7500   | μmho      | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0  | f = 1 kHz   |
|                            | 8   C <sub>iss</sub>   Common-Source Input Capacitance (Output Shorted)  |                | 6             |               | 6  | pF        |  | f = 1 MHz   |
|                            | 9   C <sub>rss</sub>   Common-Source Reverse Transfer Capacitance        |                | 2             |               | 2  |           |  |             |
| F<br>R<br>E<br>Q           | 10    y <sub>fs</sub>     Common-Source Forward Transadmittance          | 2700           |               | 1700          |  | μmho      | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0  | f = 200 MHz |
|                            | 11   g <sub>iss</sub>   Common-Source Input Conductance (Output Shorted) |                | 800           |               | 800  |           |  |             |
|                            | 12   g <sub>oss</sub>   Common-Source Output Conductance (Input Shorted) |                | 200           |               | 200  |           |  |             |
|                            | 13   G <sub>ps</sub>   Small Signal Power Gain                           | 10             |               |               |  |           |  |             |
| 14   NF   Noise Figure     |  | 5              |               |               | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0,<br>R <sub>gen</sub> = 1 K |           |  |             |

\*JEDEC registered data.

NRL

#### NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

2N4223 2N4224

3

Siliconix

# n-channel JFETs designed for . . .



- Small-Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

**Performance Curves NP**  
**See Section 5**

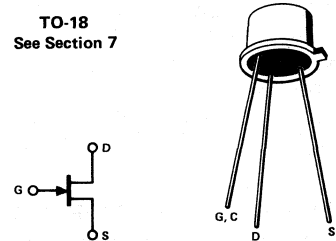
**BENEFITS**

- Low Noise  
NF < 1 dB at 1 kHz
- Operation from Low Power Supply Voltages  
V<sub>GS(off)</sub> < 1 V (2N4338)
- Simple Biasing Design with Tightly Specified Parameter Tolerances  
3:1 I<sub>DSS</sub>, V<sub>p</sub>, g<sub>fs</sub> Ranges
- High Off-Isolation as a Switch  
I<sub>D(off)</sub> < 50 pA

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -50 V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation (Note 2) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C  
 Maximum Operating Temperature . . . . . 175°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 300°C

**TO-18**  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)**

| Characteristic  | 2N4338              |   | 2N4339 |           | 2N4340    |           | 2N4341    |            | Unit   | Test Conditions  |      |      |   |
|---|---------------------|---|--------|-----------|-----------|-----------|-----------|------------|--------|--|------|------|---|
|   | Min                 | Max   | Min    | Max       | Min       | Max       | Min       | Max        |        |  |      |      |   |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12 | I <sub>GSS</sub>    | Gate Reverse Current                            |        | -0.1      | -0.1      | -0.1      | -0.1      | -0.1       | nA     | V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0<br>150°C  |      |      |   |
|   |                     |   |        | -0.1      | -0.1      | -0.1      | -0.1      | -0.1       | μA     |  |      |      |   |
| 3<br>4  | BV <sub>GSS</sub>   | Gate-Source Breakdown Voltage                   |        | -50       | -50       | -50       | -50       | -50        | V      | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0<br>V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.1 μA |      |      |   |
|   |                     | V <sub>GS(off)</sub>                            |        | -0.3      | -1        | -0.6      | -1.8      | -1         |        |  | -3   | -2   | -6  |
| 5   | I <sub>D(off)</sub> | Drain Cutoff Current                            |        | 0.05 (-5) | 0.05 (-5) | 0.05 (-5) | 0.05 (-5) | 0.07 (-10) | nA (V) | V <sub>DS</sub> = 15 V<br>V <sub>GS</sub> = ( )  |      |      |   |
| 6   | I <sub>DSS</sub>    | Saturation Drain Current (Note 3)               |        | 0.2       | 0.6       | 0.5       | 1.5       | 1.2        | 3.6    | 3  | 9    | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0   |
| 7   | g <sub>fs</sub>     | Common-Source Forward Transconductance (Note 3) |        | 600       | 1800      | 800       | 2400      | 1300       | 3000   | 2000   | 4000 | μmho | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0<br>f = 1 kHz  |
| 8   | g <sub>os</sub>     | Common-Source Output Conductance                |        |           | 5         |           | 15        |            | 30     |  | 60   |      |   |
| 9   | r <sub>ds(on)</sub> | Drain-Source ON Resistance                      |        |           | 2500      |           | 1700      |            | 1500   |  | 800  | ohm  | V <sub>DS</sub> = 0, V <sub>GS</sub> = 0  |
| 10  | C <sub>iss</sub>    | Common-Source Input Capacitance                 |        |           | 7         |           | 7         |            | 7      |  | 7    | pF   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0<br>f = 1 MHz  |
| 11  | C <sub>rss</sub>    | Common-Source Reverse Transfer Capacitance      |        |           | 3         |           | 3         |            | 3      |  | 3    |      |   |
| 12  | NF                  | Noise Figure                                    |        |           | 1         |           | 1         |            | 1      |  | 1    | dB   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0<br>R <sub>gen</sub> = 1 meg, BW = 200 Hz<br>f = 1 kHz |

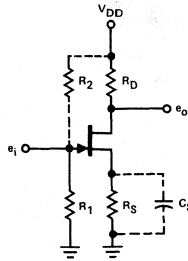
\*JEDEC registered data

NP

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 125 msec (I<sub>DSS</sub>) and 625 msec (g<sub>fs</sub>) after d-c power is applied. (Not a JEDEC condition.)

# APPLICATIONS



Amplifier Design Chart

| VDD (V)                | RS (Ω) | R1 (Ω)  | R2 (Ω) | CS (μF) | IDD (mA) | RD (KΩ) | e <sub>o</sub> Max (pk V) | AV      |
|------------------------|--------|---------|--------|---------|----------|---------|---------------------------|---------|
| <b>2N4338</b>          |        |         |        |         |          |         |                           |         |
| 15                     | 1500   | 1M      | ∞      | 0       | 0.25     | 36      | 2.5                       | 9-12    |
|                        |        |         |        | 30      |          | 36      | 1.5                       | 16-24   |
|                        | 5100   | 1M      | ∞      | 0       | 0.12     | 47      | 2.0                       | 20-30   |
|                        |        |         |        | 25      |          | 82      | 3.0                       | 10-10.5 |
| 30                     | 36K    | 1M      | 2M     | 30      | 0.15     | 27      | 1.0                       | 13-18.5 |
|                        |        |         |        | 0       |          | 82      | 4.0                       | 21.5-27 |
|                        | 1500   | 1M      | ∞      | 30      | 0.25     | 82      | 2.5                       | 32-49   |
|                        |        |         |        | 0       |          | 100     | 3.0                       | 43-64   |
| 45                     | 5100   | 1M      | ∞      | 0       | 0.12     | 150     | 4.5                       | 14.5-16 |
|                        |        |         |        | 25      |          | 150     | 2.5                       | 38-54   |
|                        | 36K    | 1M      | 5M     | 30      | 0.15     | 200     | 1.5                       | 40-50   |
|                        |        |         |        | 0       |          | 82      | 5.0                       | 37-52   |
| VDD = +15<br>VSS = -15 | 1500   | 1M      | ∞      | 0       | 0.25     | 120     | 6.5                       | 27-33   |
|                        |        |         |        | 30      |          | 120     | 4.0                       | 45-68   |
|                        | 5100   | 1M      | ∞      | 0       | 0.12     | 270     | 10                        | 28-31   |
|                        |        |         |        | 25      |          | 270     | 5.0                       | 76-105  |
| 36K                    | 1M     | 8.2M    | 0      | 0.15    | 120      | 14      | 2.8                       |         |
|                        |        |         | 30     |         | 120      | 7.0     | 54-76                     |         |
| <b>2N4339</b>          |        |         |        |         |          |         |                           |         |
| 15                     | 1800   | 1M      | ∞      | 0       | 0.42     | 20      | 3.0                       | 7-7.5   |
|                        |        |         |        | 40      |          | 20      | 2.0                       | 17-22   |
|                        | 9100   | 1M      | 6.8M   | 35      | 0.32     | 27      | 2.0                       | 23-27   |
|                        |        |         |        | 0       |          | 18      | 2.0                       | 17-19   |
| 30                     | 27K    | 1M      | 3M     | 25      | 0.2      | 30      | 2.5                       | 26-28   |
|                        |        |         |        | 0       |          | 22      | 1.0                       | 16-18   |
|                        | 1800   | 1M      | ∞      | 40      | 0.42     | 47      | 6.5                       | 15-17   |
|                        |        |         |        | 0       |          | 47      | 4.0                       | 38-47   |
| 45                     | 9100   | 1M      | 13M    | 35      | 0.32     | 51      | 4.5                       | 40-50   |
|                        |        |         |        | 0       |          | 43      | 8.0                       | 4.5     |
|                        | 27K    | 1M      | 7.5M   | 25      | 0.2      | 43      | 5.0                       | 40-43   |
|                        |        |         |        | 0       |          | 68      | 4.5                       | 53-60   |
| VDD = +15<br>VSS = -15 | 1800   | 1M      | ∞      | 40      | 0.42     | 68      | 4.0                       | 49-52   |
|                        |        |         |        | 0       |          | 100     | 7.0                       | 66-70   |
|                        | 9100   | 1M      | 22M    | 25      | 0.32     | 75      | 7.5                       | 23-25   |
|                        |        |         |        | 0       |          | 75      | 5.0                       | 58-70   |
| 27K                    | 1M     | 12M     | 25     | 0.2     | 100      | 7.0     | 73-77                     |         |
|                        |        |         | 0      |         | 68       | 7.0     | 7.0                       |         |
|                        | 0      | 0       | 0      | 25      | 0.32     | 68      | 6.5                       | 59-64   |
|                        |        |         |        | 0       |          | 120     | 7.0                       | 80-85   |
| 100                    | 12     | 3.3     | 0      | 0.2     | 100      | 12      | 3.3                       |         |
|                        |        |         | 0      |         | 100      | 5.0     | 65-68                     |         |
| 180                    | 8.0    | 100-115 | 0      | 0.22    | 180      | 8.0     | 100-115                   |         |
|                        |        |         | 0      |         | 0        | 10      | 0.98                      |         |

| VDD (V)                | RS (Ω) | R1 (Ω) | R2 (Ω) | CS (μF) | IDD (mA) | RD (KΩ) | e <sub>o</sub> Max (pk V) | AV      |       |
|------------------------|--------|--------|--------|---------|----------|---------|---------------------------|---------|-------|
| <b>2N4340</b>          |        |        |        |         |          |         |                           |         |       |
| 15                     | 680    | 1M     | ∞      | 0       | 1.5      | 5.1     | 3.0                       | 3.5-4   |       |
|                        |        |        |        | 65      |          | 5.1     | 1.5                       | 7-8.5   |       |
|                        | 1200   | 1M     | ∞      | 0       | 1.1      | 6.8     | 2.0                       | 9-10.5  |       |
|                        |        |        |        | 60      |          | 7.5     | 2.5                       | 3.5-4   |       |
| 30                     | 3900   | 1M     | ∞      | 0       | 0.4      | 7.5     | 2.0                       | 9-11    |       |
|                        |        |        |        | 40      |          | 10      | 2.0                       | 11-13   |       |
|                        | 680    | 1M     | ∞      | 0       | 1.5      | 18      | 4.0                       | 3.5-4   |       |
|                        |        |        |        | 65      |          | 18      | 1.5                       | 15-18   |       |
| 45                     | 1200   | 1M     | ∞      | 0       | 1.1      | 22      | 1.0                       | 19-22   |       |
|                        |        |        |        | 60      |          | 12      | 6.0                       | 9.5-10  |       |
|                        | 3900   | 1M     | ∞      | 0       | 0.4      | 18      | 3.0                       | 17-22   |       |
|                        |        |        |        | 40      |          | 18      | 1.0                       | 24-26   |       |
| VDD = +15<br>VSS = -15 | 20K    | 1M     | 6.8M   | 35      | 0.35     | 18      | 6.0                       | 9.5-9   |       |
|                        |        |        |        | 0       |          | 39      | 7.0                       | 7.5-8   |       |
|                        | 680    | 1M     | ∞      | 65      | 1.5      | 39      | 7.0                       | 30-36   |       |
|                        |        |        |        | 0       |          | 62      | 0.5                       | 34-45   |       |
| 2N4341                 | 20K    | 1M     | 3M     | 55      | 1.0      | 30      | 3.0                       | 25-27   |       |
|                        |        |        |        | 0       |          | 56      | 6.5                       | 40      |       |
|                        | 1200   | 1M     | ∞      | 0       | 1.1      | 20      | 10.5                      | 14-15.5 |       |
|                        |        |        |        | 60      |          | 20      | 8.0                       | 27-32   |       |
| VDD = +15<br>VSS = -15 | 22K    | 1M     | ∞      | 0       | 0.75     | 0       | 12                        | 0.96    |       |
|                        |        |        |        | 0       |          | 27      | 4.0                       | 35      |       |
|                        | 15     | 1000   | 1M     | ∞       | 70       | 2.7     | 2                         | 1.0     | 3-3.5 |
|                        |        |        |        |         | 80       |         | 2.7                       | 2.0     | 4-4.5 |
| 30                     | 1200   | 1.2M   | 7.5M   | 80      | 3.5      | 1.2     | 2.0                       | 2.5     |       |
|                        |        |        |        | 65      |          | 2.2     | 3.0                       | 3-4.5   |       |
|                        | 2000   | 1M     | ∞      | 0       | 1.8      | 3       | 2.0                       | 4-4.5   |       |
|                        |        |        |        | 70      |          | 4.7     | 1.5                       | 6-6.5   |       |
| 45                     | 1000   | 1M     | ∞      | 0       | 2.7      | 6.2     | 7.0                       | 4.0     |       |
|                        |        |        |        | 70      |          | 6.2     | 3.5                       | 10      |       |
|                        | 1200   | 1.1M   | 15M    | 80      | 3.5      | 9.1     | 1.5                       | 11-13   |       |
|                        |        |        |        | 0       |          | 3.9     | 4.0                       | 7.5-8   |       |
| VDD = +15<br>VSS = -15 | 2000   | 1M     | ∞      | 65      | 1.8      | 9.1     | 6.0                       | 3.0     |       |
|                        |        |        |        | 0       |          | 9.1     | 4.0                       | 12      |       |
|                        | 15K    | 1M     | 3.3M   | 50      | 0.7      | 15      | 1.0                       | 13-19   |       |
|                        |        |        |        | 0       |          | 18      | 3.0                       | 16-21   |       |
| 10K                    | 1M     | ∞      | 0      | 1.9     | 0        | 13.5    | 0.94                      |         |       |
|                        |        |        | 0      |         | 10       | 8.5     | 6.3                       |         |       |
|                        | 1200   | 1M     | 22M    | 80      | 3.5      | 10      | 6.0                       | 16      |       |
|                        |        |        |        | 0       |          | 6.8     | 7.0                       | 13      |       |
| 2000                   | 1M     | ∞      | 0      | 1.8     | 15       | 8.5     | 5.5                       |         |       |
|                        |        |        | 65     |         | 15       | 5.0     | 20-21                     |         |       |
| 15K                    | 1M     | 5.6M   | 50     | 0.7     | 30       | 9.0     | 28-35                     |         |       |
|                        |        |        | 0      |         | 0        | 30      | 9.0                       |         |       |

2N4338 2N4339 2N4340 2N4341

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NC**  
**See Section 5**

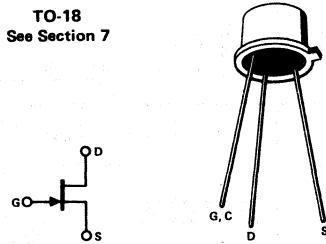
**BENEFITS**

- Low Insertion Loss, High Accuracy in Test Systems  $r_{ON} < 30 \Omega$  (2N4391)
- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive  
High Isolation Resistance from Driver
- High Off-Isolation  $I_{D(off)} < 100 \text{ pA}$
- High Speed  $t_{ON} < 20 \text{ ns}$

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . -40 V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Case Temperature  
 (Derate 10 mW/°C) . . . . . 1.8 W  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature  
 (1/16" from case for 60 seconds) . . . . . 300°C

TO-18  
See Section 7



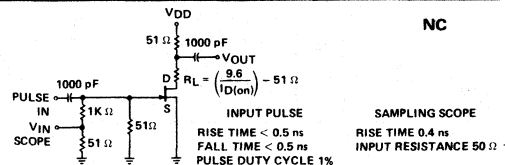
**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | 2N4391   |  | 2N4392 |     | 2N4393 |      | Unit | Test Conditions                             |                          |                          |
|--|--|--|--------|-----|--------|------|------|---|--------------------------|--------------------------|
|  | Min  | Max  | Min    | Max | Min    | Max  |      |   |                          |                          |
| 1   2   <b>S</b><br><b>T</b><br><b>A</b><br><b>T</b><br><b>I</b><br><b>C</b> | $I_{GSS}$   Gate Reverse Current   |  | -100   |     | -100   |      | -100 | $V_{GS} = -20 \text{ V}, V_{DS} = 0$        |                          |                          |
|  |  |  | -200   |     | -200   |      | -200 |   | 150°C                    |                          |
| 3  | $BV_{GSS}$   Gate-Source Breakdown Voltage   | -40  |        | -40 |        | -40  |      | $I_G = -1 \mu\text{A}, V_{DS} = 0$          |                          |                          |
| 4  | 5   6   7   8   9   <b>D</b><br><b>R</b><br><b>A</b><br><b>I</b><br><b>N</b><br><b>C</b> | $I_{D(off)}$   Drain Cutoff Current                    |        |     |        |      | 100  | $V_{DS} = 20 \text{ V}$                     | $V_{GS} = -5 \text{ V}$  |                          |
|  |  |  |        |     |        |      | 200  |   | 150°C                    |                          |
|  |  |  |        |     |        |      |      |   |                          | $V_{GS} = -7 \text{ V}$  |
|  |  |  |        |     |        |      |      |   |                          | 150°C                    |
|  |  |  |        |     |        |      |      |   |                          | $V_{GS} = -12 \text{ V}$ |
|  |  |  |        |     |        |      |      |   |                          | 150°C                    |
| 10   | $V_{GS(f)}$   Gate-Source Forward Voltage  |  | 1      |     | 1      |      | 1    | $I_G = 1 \text{ mA}, V_{DS} = 0$            |                          |                          |
| 11   | $V_{GS(off)}$   Gate-Source Cutoff Voltage   | -4   | -10    | -2  | -5     | -0.5 | -3   | $V_{DS} = 20 \text{ V}, I_D = 1 \text{ nA}$ |                          |                          |
| 12   | $I_{DSS}$   Saturation Drain Current (Note 1)  | 50   | 150    | 25  | 75     | 5    | 30   | $V_{DS} = 20 \text{ V}, V_{GS} = 0$         |                          |                          |
| 13   | 14   15   <b>V</b><br><b>D</b><br><b>S</b><br><b>(on)</b>                                | $V_{DS(on)}$   Drain Source ON Voltage                 |        |     |        |      |      | $V_{GS} = 0$                                | $I_D = 3 \text{ mA}$     |                          |
|  |  |  |        |     |        |      |      |   | $I_D = 6 \text{ mA}$     |                          |
|  |  |  |        |     |        |      |      |   | $I_D = 12 \text{ mA}$    |                          |
| 16   | $r_{DS(on)}$   Static Drain-Source ON Resistance   |  | 30     |     | 60     |      | 100  | $V_{GS} = 0, I_D = 1 \text{ mA}$            |                          |                          |
| 17   | $r_{ds(on)}$   Drain-Source ON Resistance  |  | 30     |     | 60     |      | 100  | $V_{GS} = 0, I_D = 0$                       | $f = 1 \text{ kHz}$      |                          |
| 18   | $C_{iss}$   Common-Source Input Capacitance  |  | 14     |     | 14     |      | 14   | $V_{DS} = 20 \text{ V}, V_{GS} = 0$         |                          |                          |
| 19   | 20   21   <b>C</b><br><b>R</b><br><b>S</b><br><b>S</b>                                   | $C_{rss}$   Common-Source Reverse Transfer Capacitance |        |     |        |      |      | $V_{DS} = 0$                                | $V_{GS} = -5 \text{ V}$  |                          |
|  |  |  |        |     |        |      |      |   | $V_{GS} = -7 \text{ V}$  |                          |
|  |  |  |        |     |        |      |      |   | $V_{GS} = -12 \text{ V}$ |                          |
| 22   | $t_d(on)$   Turn-ON Delay Time   |  | 15     |     | 15     |      | 15   | $V_{DD} = 10 \text{ V}, V_{GS(on)} = 0$     |                          |                          |
| 23   | $t_r$   Rise Time  |  | 5      |     | 5      |      | 5    | $I_{D(on)}$   $V_{GS(off)}$   $R_L$         |                          |                          |
| 24   | $t_d(off)$   Turn-OFF Delay Time   |  | 20     |     | 35     |      | 50   | 2N4391 12 mA -12 V 800 $\Omega$             |                          |                          |
| 25   | $t_f$   Fall Time  |  | 15     |     | 20     |      | 30   | 2N4392 6 -7 1.6K $\Omega$                   |                          |                          |
|  |  |  |        |     |        |      |      | 2N4393 3 -5 3.2K $\Omega$                   |                          |                          |

\*JEDEC registered data.

**NOTE:**

1. Pulse test required, pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 3\%$ .



# n-channel JFETs designed for . . .



2N4416 2N4416A

- VHF Amplifiers
- Mixers

## Performance Curves NH See Section 5

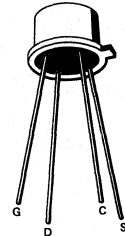
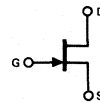
### BENEFITS

- Low Noise  
NF = 3 dB Typical at 400 MHz
- Wide Band  
High  $g_{fs}/C_{iss}$  Ratio

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|  |               |
|--|---------------|
| Gate-Drain or Gate-Source Voltage, 2N4416 . . . . .            | -30 V         |
| Gate-Drain or Gate-Source Voltage, 2N4416A . . . . .           | -35 V         |
| Gate Current . . . . .   | 10 mA         |
| Total Device Dissipation (Derate 1.7 mW/°C) . . . . .          | 300 mW        |
| Storage Temperature Range . . . . .                            | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 60 seconds) . . . . . | 300°C         |

TO-72  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                           |   | Min  | Max  | Unit  | Test Conditions                                |         |
|--|---|------|------|---|--|---------|
| S<br>T<br>A<br>T<br>I<br>C               | 1 IGSS Gate Reverse Current                                   |      | -0.1 | nA  | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V | 150°C   |
|  | 2   |      | -0.1 | μA  |  |         |
|  | 3 BVGSS Gate-Source Breakdown Voltage                         | -30  |      | V   | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V  | 2N4416  |
|  |   | -35  |      |   |  | 2N4416A |
| 4 VGS(off) Gate-Source Cutoff Voltage    |   | -6   | V    | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 nA | 2N4416   |         |
|  | -2.5  | -6   |      |   | 2N4416A  |         |
| 5 IDSS Saturation Drain Current (Note 1) | 5   | 15   | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V | f = 1 kHz                                      |         |
| 6 DYNAMI<br>C                            | 6 g <sub>fs</sub> Common-Source Forward Transconductance      | 4500 | 7500 |   |  | μmho    |
| 7  | 7 g <sub>os</sub> Common-Source Output Conductance            |      | 50   |   |  | μmho    |
| 8  | 8 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |      | 0.8  |   |  | pF      |
| 9  | 9 C <sub>iss</sub> Common-Source Input Capacitance            |      | 4    |   |  | pF      |
| 10                                       | 10 C <sub>oss</sub> Common-Source Output Capacitance          |      | 2    |   |  |         |

| Characteristic  |   | 100 MHz |      | 400 MHz |        | Unit | Test Conditions                               |  |
|---|---|---------|------|---------|--------|------|---|--|
|   |   | Min     | Max  | Min     | Max    |      |   |  |
| H<br>I<br>G<br>H<br>F<br>R<br>E<br>Q<br>U<br>E<br>N<br>C<br>Y | 11 g <sub>iss</sub> Common-Source Input Conductance       |         | 100  |         | 1000   | μmho | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V |  |
|   | 12 b <sub>iss</sub> Common-Source Input Susceptance       |         | 2500 |         | 10,000 | μmho |   |  |
|   | 13 g <sub>oss</sub> Common-Source Output Conductance      |         | 75   |         | 100    | μmho |   |  |
|   | 14 b <sub>oss</sub> Common-Source Output Susceptance      |         | 1000 |         | 4000   | μmho |   |  |
|   | 15 g <sub>fs</sub> Common-Source Forward Transconductance |         |      | 4000    |        | μmho |   |  |
|   | 16 G <sub>ps</sub> Common-Source Power Gain               | 18      |      | 10      |        | dB   |   | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA                        |
|   | 17 NF Noise Figure  |         | 2    |         | 4      | dB   |   | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA, R <sub>G</sub> = 1K Ω |

\*JEDEC Registered data

NH

#### NOTES:

1. Pulse test duration = 300 μs.

3

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NC**  
See Section 5

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

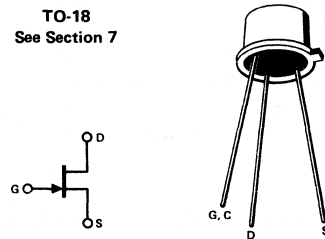
**BENEFITS**

- Low Insertion Loss and High Accuracy in Test Systems  
 $r_{DS(on)} < 25 \Omega$  (2N4856, 59)
- High Off-Isolation  
 $I_{D(off)} < 250 \text{ pA}$
- High Speed  
 $t_{ON} < 9 \text{ ns}$
- Fully Qualified  
JAN, JANTX and JANTXV Available

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |               |
|--|---------------|
| Reverse Gate-Drain or Gate-Source Voltage,<br>2N4856-58 . . . . .                | -40 V         |
| Reverse Gate-Drain or Gate-Source Voltage,<br>2N4859-61 . . . . .                | -30 V         |
| Gate Current . . . . .   | 50 mA         |
| Total Device Dissipation at 25°C Case Temperature<br>(Derate 10 mW/°C) . . . . . | 1.8 W         |
| Storage Temperature Range . . . . .  | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) . . . . .                   | 300°C         |

TO-18  
See Section 7



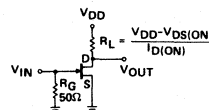
**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| 1   | 2  | Characteristic  | 2N4856<br>2N4859 |                     | 2N4857<br>2N4860 |                    | 2N4858<br>2N4861 |                    | Unit   | Test Conditions  |  |
|---|--|---|------------------|---------------------|------------------|--------------------|------------------|--------------------|--|--|--|
|   |  |   | Min              | Max                 | Min              | Max                | Min              | Max                |  |  |  |
| S<br>T<br>A<br>T<br>I<br>C                | 1  | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | 2N4856-58        | -40                 | -40              | -40                | -40              |                    | V  | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0  |  |
|   |  |   | 2N4859-61        | -30                 | -30              | -30                | -30              |                    |  |  |  |
|   | 4  | I <sub>GSS</sub> Gate Reverse Current                       | 2N4856-58        |                     | -250             | -250               | -250             | -250               | pA   | V <sub>GS</sub> = -20 V,<br>V <sub>DS</sub> = 0  | 150°C  |
|   |  |   |                  |                     | -500             | -500               | -500             | -500               | nA   |  |  |
|   |  |   | 2N4859-61        |                     | -250             | -250               | -250             | -250               | pA   |  |  |
|   |  |   |                  |                     | -500             | -500               | -500             | -500               | nA   |  |  |
|   | 7  | I <sub>D(off)</sub> Drain Cutoff Current                    |                  | 250                 | 250              | 250                | 250              | pA                 | V <sub>DS</sub> = 15 V,<br>V <sub>GS</sub> = -10 V | 150°C  |  |
|   |  |   |                  | 500                 | 500              | 500                | 500              | nA                 |  |  |  |
| 9   | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage    |   | -4               | -10                 | -2               | -6                 | -0.8             | -4                 | V  | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.5 nA  |  |
| 10  | I <sub>DSS</sub> Saturation Drain Current (Note 1) |   | 50               |                     | 20               | 100                | 8                | 80                 | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0  |  |
| 11  | V <sub>DS(on)</sub> Drain-Source ON Voltage        |   |                  | 0.75<br>(20)        |                  | 0.50<br>(10)       |                  | 0.50<br>(5)        | V<br>(mA)  | V <sub>GS</sub> = 0, I <sub>D</sub> = ( )  |  |
| D<br>Y<br>N                               | 12   | r <sub>ds(on)</sub> Drain-Source ON Resistance              |                  | 25                  |                  | 40                 |                  | 60                 | Ω  | V <sub>GS</sub> = 0,<br>I <sub>D</sub> = 0   | f = 1 kHz  |
|   | 13   | C <sub>iss</sub> Common-Source Input Capacitance            |                  | 18                  |                  | 18                 |                  | 18                 | pF   | V <sub>DS</sub> = 0,<br>V <sub>GS</sub> = -10 V  | f = 1 MHz  |
|   | 14   | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |                  | 8                   |                  | 8                  |                  | 8                  |  |  |  |
| S<br>W<br>I<br>T<br>C<br>H<br>I<br>N<br>G | 15   | t <sub>d(on)</sub> Turn-ON Delay Time                       |                  | 6<br>(20)<br>[-10]  |                  | 6<br>(10)<br>[-6]  |                  | 10<br>(5)<br>[-4]  | ns<br>(mA)<br>[V]                                  | V <sub>DD</sub> = 10 V,<br>V <sub>GS(on)</sub> = 0,<br>I <sub>D(on)</sub> = ( ),<br>V <sub>GS(off)</sub> = [ ] | R <sub>L</sub> = {<br>464 Ω, 2N4856, 59<br>953 Ω, 2N4857, 60<br>1910 Ω, 2N4858, 61 |
|   | 16   | t <sub>r</sub> Rise Time                                    |                  | 3<br>(20)<br>[-10]  |                  | 4<br>(10)<br>[-6]  |                  | 10<br>(5)<br>[-4]  | ns<br>(mA)<br>[V]                                  |  |  |
|   | 17   | t <sub>off</sub> Turn-OFF Time                              |                  | 25<br>(20)<br>[-10] |                  | 50<br>(10)<br>[-6] |                  | 100<br>(5)<br>[-4] | ns<br>(mA)<br>[V]                                  |  |  |

\*JEDEC registered data.

**NOTE:**

- Pulse test required, pulswidth = 100 μs, duty cycle ≤ 10%.



**NC**

INPUT PULSE  
RISE TIME 0.25 ns  
FALL TIME 0.75 ns  
PULSE WIDTH 100 ns  
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE  
RISE TIME 0.75 ns  
INPUT RESISTANCE 1 M  
INPUT CAPACITANCE 2.5 pF

# n-channel JFETs designed for . . .



**Performance Curves NC**  
See Section 5

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

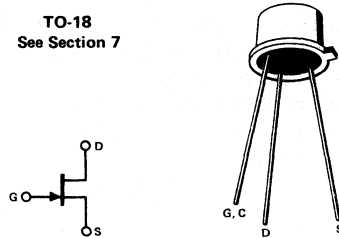
**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |               |
|---|---------------|
| Reverse Gate-Drain or Gate-Source Voltage,<br>2N4856A-58A. . . . .              | -40 V         |
| Reverse Gate-Drain or Gate-Source Voltage,<br>2N4859A-61A. . . . .              | -30 V         |
| Gate Current. . . . .   | 50 mA         |
| Total Device Dissipation at 25°C Case Temperature<br>(Derate 10 mW/°C). . . . . | 1.8 W         |
| Storage Temperature Range . . . . .   | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) . . . . .                  | 300°C         |

**BENEFITS**

- Low Insertion Loss and High Accuracy in Test Systems  
 $r_{DS(on)} < 25 \Omega$  (2N4856A, 59A)
- High Off-Isolation  
 $I_{D(off)} < 250 \text{ pA}$
- Short Sample and Hold Aperture Time  
 $C_{rss} < 4 \text{ pF}$
- High Speed  
 $t_{ON} < 8 \text{ ns}$

**TO-18**  
See Section 7



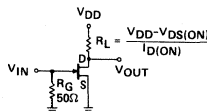
**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| 1   | 2  | 3                    | 4                                 | 5           | 6   | 7                   | 8   | 9                  | 10   | 11                | 12 | 13 | 14 | 15 | 16 | 17 | 2N4856A<br>2N4859A |     |                                      |  | 2N4857A<br>2N4860A |     |     |     | 2N4858A<br>2N4861A |     |     |     | Unit | Test Conditions |
|---|----|----------------------|-----------------------------------|-------------|-----|---------------------|-----|--------------------|------|-------------------|----|----|----|----|----|----|--------------------|-----|--------------------------------------|--|--------------------|-----|-----|-----|--------------------|-----|-----|-----|------|-----------------|
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    | Min                | Max | Min                                  | Max  | Min                | Max | Min | Max | Min                | Max | Min | Max |      |                 |
| S<br>T<br>A<br>T<br>I<br>C                | 1  | BV <sub>GSS</sub>    | Gate-Source Breakdown Voltage     | 2N4856A-58A | -40 |                     | -40 |                    | -40  |                   |    |    |    |    |    |    |                    | V   | $I_G = -1 \mu\text{A}, V_{DS} = 0$   |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A | -30 |                     | -30 |                    | -30  |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| S<br>T<br>A<br>T<br>I<br>C                | 4  | I <sub>GSS</sub>     | Gate Reverse Current              | 2N4856A-58A |     | -250                |     | -250               |      | -250              |    |    |    |    |    |    |                    | pA  | $V_{GS} = -20 \text{ V}, V_{DS} = 0$ |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     | -500                |     | -500               |      | -500              |    |    |    |    |    |    |                    |     |                                      | nA   |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| S<br>T<br>A<br>T<br>I<br>C                | 7  | I <sub>D(off)</sub>  | Drain Cutoff Current              | 2N4856A-58A |     | -250                |     | -250               |      | -250              |    |    |    |    |    |    |                    |     | pA                                   | $V_{DS} = 15 \text{ V}, V_{GS} = 0$  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     | -500                |     | -500               |      | -500              |    |    |    |    |    |    |                    |     | nA                                   |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| S<br>T<br>A<br>T<br>I<br>C                | 9  | V <sub>GS(off)</sub> | Gate-Source Cutoff Voltage        | 2N4856A-58A | -4  | -10                 | -2  | -6                 | -0.8 | -4                |    |    |    |    |    |    |                    |     | V                                    | $V_{DS} = 15 \text{ V}, I_D = 0.5 \text{ nA}$  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| D<br>Y<br>N                               | 10 | I <sub>DSS</sub>     | Saturation Drain Current (Note 1) | 2N4856A-58A | 50  |                     | 20  | 100                | 8    | 80                |    |    |    |    |    |    |                    |     | mA                                   | $V_{DS} = 15 \text{ V}, V_{GS} = 0$  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| D<br>Y<br>N                               | 11 | V <sub>DS(on)</sub>  | Drain-Source ON Voltage           | 2N4856A-58A |     | 0.75<br>(20)        |     | 0.50<br>(10)       |      | 0.50<br>(5)       |    |    |    |    |    |    |                    |     | V<br>(mA)                            | $V_{GS} = 0, I_D = ( )$  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| D<br>Y<br>N                               | 12 | r <sub>ds(on)</sub>  | Drain-Source ON Resistance        | 2N4856A-58A |     | 25                  |     | 40                 |      | 60                |    |    |    |    |    |    |                    |     | $\Omega$                             | $V_{GS} = 0, I_D = 0$<br>f = 1 kHz   |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| D<br>Y<br>N                               | 13 | C <sub>iss</sub>     | Common-Source Input Capacitance   | 2N4856A-58A |     | 10                  |     | 10                 |      | 10                |    |    |    |    |    |    |                    |     |                                      | $V_{DS} = 0, V_{GS} = -10 \text{ V}$<br>f = 1 MHz  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| S<br>W<br>I<br>T<br>C<br>H<br>I<br>N<br>G | 15 | t <sub>d(on)</sub>   | Turn-ON Delay Time                | 2N4856A-58A |     | 5<br>(20)<br>[-10]  |     | 6<br>(10)<br>[-6]  |      | 8<br>(5)<br>[-4]  |    |    |    |    |    |    |                    |     | ns<br>(mA)<br>[V]                    | $V_{DD} = 10 \text{ V}, V_{GS(on)} = 0, I_D(on) = ( ), V_{GS(off)} = ( )$<br>$R_L = \begin{cases} 464 \Omega, 2N4856A, 59A \\ 953 \Omega, 2N4857A, 60A \\ 1910 \Omega, 2N4858A, 61A \end{cases}$ |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| S<br>W<br>I<br>T<br>C<br>H<br>I<br>N<br>G | 16 | t <sub>r</sub>       | Rise Time                         | 2N4856A-58A |     | 3<br>(20)<br>[-10]  |     | 4<br>(10)<br>[-6]  |      | 8<br>(5)<br>[-4]  |    |    |    |    |    |    |                    |     | ns<br>(mA)<br>[V]                    |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
| S<br>W<br>I<br>T<br>C<br>H<br>I<br>N<br>G | 17 | t <sub>off</sub>     | Turn-OFF Time                     | 2N4856A-58A |     | 20<br>(20)<br>[-10] |     | 40<br>(10)<br>[-6] |      | 80<br>(5)<br>[-4] |    |    |    |    |    |    |                    |     | ns<br>(mA)<br>[V]                    |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   | 2N4859A-61A |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |
|   |    |                      |                                   |             |     |                     |     |                    |      |                   |    |    |    |    |    |    |                    |     |                                      |  |                    |     |     |     |                    |     |     |     |      |                 |

\*JEDEC registered data.

**NOTE:**

- Pulse test required, pulsewidth = 100  $\mu\text{s}$ , duty cycle  $\leq$  10%.



**INPUT PULSE**  
RISE TIME 0.25 ns  
FALL TIME 0.75 ns  
PULSE WIDTH 100 ns  
PULSE DUTY CYCLE < 10%

**SAMPLING SCOPE**  
RISE TIME 0.75 ns  
INPUT RESISTANCE 1 M  
INPUT CAPACITANCE 2.5 pF

NC

2N4856A 2N4857A 2N4858A  
2N4859A 2N4860A 2N4861A

3

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NS**  
See Section 5

## ■ Audio and Sub-Audio Amplifiers

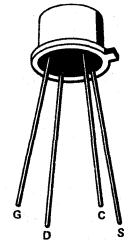
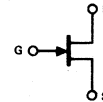
### BENEFITS

- Ultra Low Noise  
 $\bar{e}_n = 8 \text{ nV}/\sqrt{\text{Hz}}$  Typical at 10 Hz  
 $\bar{e}_n = 2 \text{ nV}/\sqrt{\text{Hz}}$  Typical at 1 kHz

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -40 V  
 Gate Current or Drain Current . . . . . 50 mA  
 Total Device Dissipation  
 (Derate 1.7 mW/°C) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature  
 (1/16" from case for 60 seconds) . . . . . 300°C

TO-72  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  |                            | 2N4867<br>2N4867A    |  | 2N4868<br>2N4868A |      | 2N4869<br>2N4869A |      | Unit  | Test Conditions  |  |   |   |                |           |
|---|----------------------------|----------------------|--|-------------------|------|-------------------|------|-------|--|--|---|---|----------------|-----------|
|   |                            | Min                  | Max  | Min               | Max  | Min               | Max  |       |  |  |   |   |                |           |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12<br>13<br>14 | S<br>T<br>A<br>T<br>I<br>C | I <sub>GSS</sub>     |  | -0.25             |      | -0.25             |      | -0.25 | nA   | V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 | 150°C   |   |                |           |
|   |                            | BV <sub>GSS</sub>    | -40  |                   | -40  |                   | -40  |       | V  | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0  |   |   |                |           |
|   |                            | V <sub>GS(off)</sub> | -0.7   | -2                | -1   | -3                | -1.8 | -5    |  | V  | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 μA |   |                |           |
|   |                            | I <sub>DSS</sub>     | 0.4  | 1.2               | 1    | 3                 | 2.5  | 7.5   | mA   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0  |   |   |                |           |
| D<br>Y<br>N<br>A<br>M<br>I<br>C   |                            | g <sub>fs</sub>      | 700  | 2000              | 1000 | 3000              | 1300 | 4000  | μmho   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0  | f = 1 kHz                                     |   |                |           |
|   |                            | g <sub>os</sub>      |  | 1.5               |      | 4                 |      | 10    |  |  |   |   |                |           |
|   |                            | C <sub>rss</sub>     |  | 5                 |      | 5                 |      | 5     |  |  | pF  | f = 1 MHz                                   |                |           |
|   |                            | C <sub>iss</sub>     |  | 25                |      | 25                |      | 25    |  |  |   |   |                |           |
|   |                            | e <sub>n</sub>       | Short Circuit Equivalent Input Noise Voltage |                   | 20   |                   | 20   |       | 20   |  | nV/√Hz  | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 | 2N4867 Series  | f = 10 Hz |
|   |                            |                      |  |                   | 10   |                   | 10   |       | 10   |  |   |   | 2N4867A Series |           |
|   |                            |                      |  |                   | 10   |                   | 10   |       | 10   |  |   |   | 2N4867 Series  | f = 1 kHz |
|   |                            | 5                    |  | 5                 |      | 5                 |      |       |  | 2N4867A Series                               |   |   |                |           |
| NF  | Spot Noise Figure          |                      | 1  |                   | 1    |                   | 1    | dB    | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0<br>R <sub>gen</sub> = 20 K, 2N4867 Series<br>5 K, 2N4867A Series | f = 1 kHz                                    |   |   |                |           |

\*JEDEC registered data.

NS

**NOTES:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms.



# p-channel JFETs designed for . . .



**Performance Curves PS**  
See Section 5

- Analog Switches
- Commutators
- Choppers

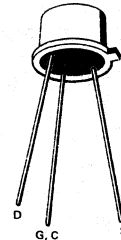
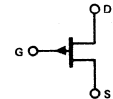
**BENEFITS**

- Low Insertion Loss  
 $R_{DS(on)} < 75 \Omega$  (2N5018)
- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |               |
|--|---------------|
| Reverse Gate-Drain or Gate-Source Voltage<br>(Note 1) . . . . .  | 30 V          |
| Gate Current . . . . .   | .50 mA        |
| Total Device Dissipation, Free-Air<br>(Derate 3 mW/°C) . . . . . | 500 mW        |
| Storage Temperature Range . . . . .                              | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 60 seconds) . . . . .   | 300°C         |

TO-18  
See Section 7



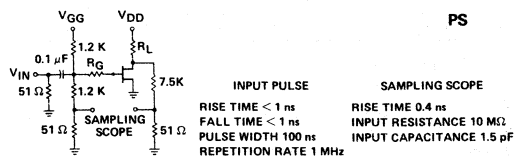
**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | 2N5018 |      | 2N5019 |      | Unit | Test Conditions   |
|--|--------|------|--------|------|------|---|
|  | Min    | Max  | Min    | Max  |      |   |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage              | 30     |      | 30     |      | V    | I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0  |
| 2 I <sub>GSS</sub> Gate Reverse Current                        |        | 2    |        | 2    | nA   | V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0   |
| 3 I <sub>D(off)</sub> Drain Cutoff Current                     |        | -10  |        | -10  | μA   | V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 12 V (2N5018)  |
| 4 I <sub>DGO</sub> Drain Reverse Current                       |        | -2   |        | -2   | nA   | V <sub>DS</sub> = 7 V (2N5019)  |
| 5 I <sub>DGO</sub> Drain Reverse Current                       |        | -3   |        | -3   | μA   | V <sub>DS</sub> = -15 V, I <sub>S</sub> = 0   |
| 6 V <sub>GS(off)</sub> Gate-Source Cutoff Voltage              |        | 10   |        | 5    | V    | V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1 μA   |
| 7 I <sub>DSS</sub> Saturation Drain Current                    | -10    |      | -5     |      | mA   | V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0  |
| 8 V <sub>DS(on)</sub> Drain-Source ON Voltage                  |        | -0.5 |        | -0.5 | V    | V <sub>GS</sub> = 0, I <sub>D</sub> = -6 mA (2N5018), I <sub>D</sub> = -3 mA (2N5019)   |
| 9 r <sub>DS(on)</sub> Static Drain-Source ON Resistance        |        | 75   |        | 150  | Ω    | I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0   |
| 10 r <sub>ds(on)</sub> Drain-Source ON Resistance              |        | 75   |        | 150  | Ω    | I <sub>D</sub> = 0, V <sub>GS</sub> = 0   |
| 11 C <sub>iss</sub> Common-Source Input Capacitance            |        | 45   |        | 45   | pF   | V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0  |
| 12 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |        | 10   |        | 10   | pF   | V <sub>DS</sub> = 0, V <sub>GS</sub> = 12 V (2N5018), V <sub>GS</sub> = 7 V (2N5019)  |
| 13 t <sub>d(on)</sub> Turn-ON Delay Time                       |        | 15   |        | 15   | ns   | V <sub>DD</sub> = -6 V, V <sub>GS(on)</sub> = 0<br>V <sub>GS(off)</sub> I <sub>D(on)</sub> R <sub>L</sub><br>2N5018 12 V -6 mA 910 Ω<br>2N5019 7 V -3 mA 1.8K Ω |
| 14 t <sub>r</sub> Rise Time                                    |        | 20   |        | 75   | ns   |   |
| 15 t <sub>d(off)</sub> Turn-OFF Delay Time                     |        | 15   |        | 25   | ns   |   |
| 16 t <sub>f</sub> Fall Time                                    |        | 50   |        | 100  | ns   |   |

\*JEDEC registered data.

**NOTE:**

- Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



2N5018 2N5019

3

Siliconix

# monolithic dual n-channel JFETs designed for . . .



## ■ High Gain Differential Amplifiers

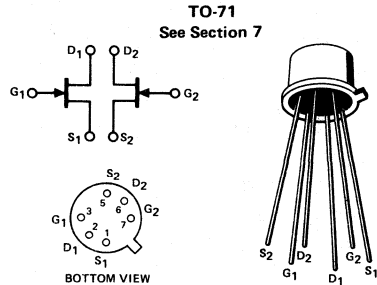
Performance Curves NNR  
See Section 5

### BENEFITS

- Minimum System Error and Calibration  
5 mV Offset Maximum (2N5045)
- Low Drift  
5 mV Drift Maximum (2N5045)

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|  |       |               |
|--|-------|---------------|
| Gate-Drain or Gate-Source Voltage                    | ..... | -50 V         |
| Forward Gate Current                                 | ..... | 30 mA         |
| Total Dissipation (25°C Free Air Temp.)              | ..... | 400 mW        |
| Power Derating (to 175°C)                            | ..... | 2.67 mW/°C    |
| Storage Temperature Range                            | ..... | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) | ..... | 300°C         |



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic (Note 1)   |                                      | 2N5045                                |  | 2N5046  |      | 2N5047 |      | Unit  | Test Conditions |   |   |   |  |
|---|--------------------------------------|---------------------------------------|--|---|------|--------|------|-------|-----------------|---|---|---|--|
|   |                                      | Min                                   | Max  | Min   | Max  | Min    | Max  |       |                 |   |   |   |  |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12<br>13<br>14<br>15<br>16<br>17<br>18<br>19<br>20 | S<br>T<br>A<br>T<br>I<br>C           | I <sub>GSS</sub>                      | Gate Reverse Current                       |   |      | -1     |      | -1    | μA              | V <sub>GS</sub> = -50 V, V <sub>DS</sub> = 0 V  |   |   |  |
|   |                                      |                                       |  |   |      | -0.25  |      | -0.25 | nA              |   |   |   |  |
|   |                                      |                                       |  |   |      | -250   |      | -250  |                 |   | -250  | T = 150°C   |  |
|   |                                      | V <sub>GS(off)</sub>                  | Gate-Source Cutoff Voltage                 |   | -0.5 | -4.5   | -0.5 | -4.5  | V               | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.5 nA |   |   |  |
|   |                                      | I <sub>DSS</sub>                      | Drain Saturation Current                   |   | 0.5  | 8.0    | 0.5  | 8.0   | 0.5             | 8.0   | mA  |   |  |
|   | D<br>Y<br>N<br>A<br>M<br>I<br>C      | g <sub>fs</sub>                       | Common-Source Forward Transconductance     |   | 1.5  | 6.0    | 1.5  | 6.0   | 1.5             | 6.0   | mmho  | f = 1 kHz   |  |
|   |                                      | y <sub>fs</sub>                       | Common-Source Forward Admittance           |   | 1.5  |        | 1.5  |       | 1.5             |   |   | f = 100 MHz   |  |
|   |                                      | g <sub>os</sub>                       | Common-Source Output Conductance           |   |      | 25     |      | 25    |                 | 25  | μmho  | f = 1 kHz   |  |
|   |                                      | C <sub>iss</sub>                      | Common-Source Input Capacitance            |   |      | 8.0    |      | 8.0   |                 | 8.0   | pF  | f = 1 MHz   |  |
|   |                                      | C <sub>rss</sub>                      | Common-Source Reverse Transfer Capacitance |   |      | 4.0    |      | 4.0   |                 | 4.0   | pF  | f = 10 Hz, R <sub>G</sub> = 1 MΩ  |  |
|   |                                      | NF                                    | Spot Noise Figure                          |   |      | 5.0    |      | 5.0   |                 |   | dB  | f = 10 Hz   |  |
|   | M<br>A<br>T<br>C<br>H<br>I<br>N<br>G | I <sub>GSS1</sub> - I <sub>GSS2</sub> |  | Differential Gate Current                       |      | 10     |      | 10    | 10              | nA  | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0 V  | T <sub>A</sub> = 100°C  |  |
|   |                                      | I <sub>DSS1</sub> /I <sub>DSS2</sub>  |  | Drain Current Ratio (Note 2)                    |      | 0.95   | 1.0  | 0.9   | 1.0             | 0.8   | 1.0   | —   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 15 V    |
|   |                                      | V <sub>GS1</sub> - V <sub>GS2</sub>   |  | Differential Gate-Source Voltage                |      |        | 5    |       | 10              | 15  | mV  | V <sub>DS</sub> = 15 V  | I <sub>D</sub> = 50 μA                           |
|   |                                      | ΔI <sub>VGS1</sub> - V <sub>GS2</sub> |  | Gate-Source Voltage Differential Drift (Note 3) |      |        | 5    |       | 10              | 15  |   | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 200 μA,<br>T <sub>A</sub> = 25°C | T <sub>B</sub> = -25°C<br>T <sub>B</sub> = 100°C |
|   |                                      | g <sub>fs1</sub> /g <sub>fs2</sub>    | Transconductance Ratio (Note 2)            |   | 0.95 | 1.0    | 0.9  | 1.0   | 0.8             | 1.0   | —   | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 200 μA                           | f = 1 kHz  |
|   |                                      | g <sub>os1</sub> - g <sub>os2</sub>   | Diff. Output Conductance                   |   |      | 1.0    |      | 2.0   | 3.0             | μmho  | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 200 μA | f = 1 kHz   |  |

\*JEDEC registered data.

#### NOTES:

- Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements.
- Assumes smaller value in numerator.
- Measured at end points, T<sub>A</sub> and T<sub>B</sub>.

NNR  
NRL-D

# p-channel JFETs designed for . . .



**Performance Curves PS**  
See Section 5

2N5114 2N5115 2N5116

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

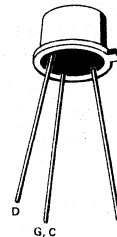
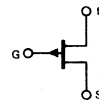
**BENEFITS**

- Simplifies Series-Shunt Switching when Combined with 2N4393, its N-Channel Complement
- Low Insertion Loss in Switching Systems  $R_{ON} < 75 \Omega$  (2N5114)
- Short Sample and Hold Aperture Time  $C_{RSS} < 7$  pF
- High Off-Isolation  $I_{D(off)} < 500$  pA

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |               |
|---|---------------|
| Reverse Gate-Drain or Gate-Source Voltage (Note 1)  | 30 V          |
| Gate Current  | .50 mA        |
| Total Device Dissipation, Free-Air (Derate 3 mW/°C) | 500 mW        |
| Storage Temperature Range                           | -65 to +200°C |
| Lead Temperature (1/16" from case for 10 seconds)   | 300°C         |

TO-18  
See Section 7



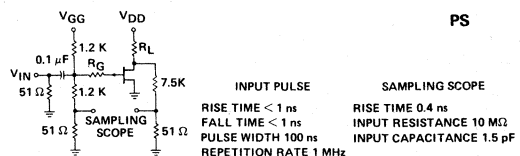
**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | 2N5114 |      | 2N5115 |      | 2N5116 |      | Unit | Test Conditions   |
|--|--------|------|--------|------|--------|------|------|---|
|  | Min    | Max  | Min    | Max  | Min    | Max  |      |   |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage              | 30     |      | 30     |      | 30     |      | V    | I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0  |
| 2 I <sub>GSS</sub> Gate Reverse Current                        |        | 500  |        | 500  |        | 500  | pA   | V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0   |
| 3  |        | 1.0  |        | 1.0  |        | 1.0  | μA   | 150°C   |
| 4 I <sub>D(off)</sub> Drain Cutoff Current                     |        | -500 |        | -500 |        | -500 | pA   | V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 12 V (2N5114)  |
| 5  |        | -1.0 |        | -1.0 |        | -1.0 | μA   | V <sub>GS</sub> = 7 V (2N5115), V <sub>GS</sub> = 5 V (2N5116)  |
| 6 V <sub>GS(off)</sub> Gate-Source Cutoff Voltage              | 5      | 10   | 3      | 6    | 1      | 4    | V    | V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1 nA   |
| 7 I <sub>DSS</sub> Saturation Drain Current (Note 2)           | -30    | -90  | -15    | -60  | -5     | -25  | mA   | V <sub>GS</sub> = 0, V <sub>DS</sub> = -18 V (2N5114)<br>V <sub>GS</sub> = -15 V (2N5115, 2N5116)                         |
| 8 V <sub>GS(f)</sub> Forward Gate-Source Voltage               |        | -1   |        | -1   |        | -1   | V    | I <sub>G</sub> = -1 mA, V <sub>DS</sub> = 0   |
| 9 V <sub>DS(on)</sub> Drain-Source ON Voltage                  |        | -1.3 |        | -0.8 |        | -0.6 | V    | V <sub>GS</sub> = 0, I <sub>D</sub> = -15 mA (2N5114)<br>I <sub>D</sub> = -7 mA (2N5115), I <sub>D</sub> = -3 mA (2N5116) |
| 10 r <sub>DS(on)</sub> Static Drain-Source ON Resistance       |        | 75   |        | 100  |        | 150  | Ω    | V <sub>GS</sub> = 0, I <sub>D</sub> = -1 mA   |
| 11 r <sub>ds(on)</sub> Drain-Source ON Resistance              |        | 75   |        | 100  |        | 150  | Ω    | V <sub>GS</sub> = 0, I <sub>D</sub> = 0   |
| 12 C <sub>iss</sub> Common-Source Input Capacitance            |        | 25   |        | 25   |        | 25   | pF   | V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0  |
| 13 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |        | 7    |        | 7    |        | 7    | pF   | V <sub>DS</sub> = 0, V <sub>GS</sub> = 12 V (2N5114)<br>V <sub>GS</sub> = 7 V (2N5115), V <sub>GS</sub> = 5 V (2N5116)    |
| 14 t <sub>d(on)</sub> Turn-ON Delay Time                       |        | 6    |        | 10   |        | 12   | ns   | 2N5114 -10 V<br>2N5115 -6 V<br>2N5116 -6 V  |
| 15 t <sub>r</sub> Rise Time                                    |        | 10   |        | 20   |        | 30   |      | V <sub>GS(off)</sub> 12 V<br>7 V<br>5 V   |
| 16 t <sub>d(off)</sub> Turn-OFF Delay Time                     |        | 6    |        | 8    |        | 10   |      | R <sub>L</sub> 580 Ω<br>743 Ω<br>1800 Ω   |
| 17 t <sub>f</sub> Fall Time                                    |        | 15   |        | 30   |        | 50   |      | V <sub>GS(on)</sub> 0<br>0<br>0   |
|  |        |      |        |      |        |      |      | I <sub>D(on)</sub> -15 mA<br>-7 mA<br>-3 mA   |

\*JEDEC registered data.

**NOTES:**

- Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
- Pulse Test PW 300 μs, duty cycle ≤ 3%.



3

Siliconix

# monolithic dual n-channel JFETs designed for . . .



**Performance Curves NNP**  
**See Section 5**

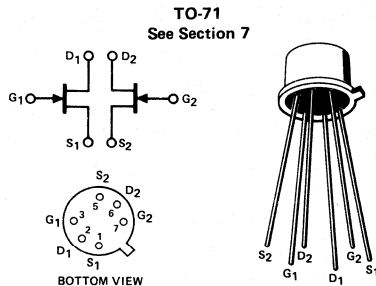
- **Differential Amplifiers**
- **FET Input Op Amps**

**BENEFITS**

- **Minimum System Error and Calibration**  
5 mV Maximum Offset (2N5196, 97)
- **Low Drift**  
5  $\mu\text{V}/^\circ\text{C}$  Maximum (2N5196)
- **Simplifies Amplifier Design**  
Low Output Conductance

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |       |               |
|---|-------|---------------|
| Gate-Drain or Gate-Source Voltage   | ..... | -50 V         |
| Gate Current  | ..... | 50 mA         |
| Device Dissipation (Each Side), $T_A = 85^\circ\text{C}$<br>(Derate 2.56 mW/ $^\circ\text{C}$ ) | ..... | 250 mW        |
| Total Device Dissipation, $T_A = 85^\circ\text{C}$<br>(Derate 4.3 mW/ $^\circ\text{C}$ )        | ..... | 500 mW        |
| Storage Temperature Range   | ..... | -65 to +200°C |



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                                       |   | Min  | Max  | Unit                                 | Test Conditions  |
|--|---|------|------|--------------------------------------|--|
| S<br>T<br>A<br>T<br>I<br>C                           | 1  G <sub>SS</sub> Gate Reverse Current                         |      | -25  | pA                                   | V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0<br>150°C  |
|  | 2   |      | -50  | nA                                   |  |
|  | 3  BV <sub>GS</sub> Gate-Source Breakdown Voltage               | -50  |      |                                      | I <sub>G</sub> = -1 $\mu\text{A}$ , V <sub>DS</sub> = 0<br>V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA   |
|  | 4  V <sub>GS(off)</sub> Gate-Source Cutoff Voltage              | -0.7 | -4   | V                                    |  |
|  | 5  V <sub>GS</sub> Gate-Source Voltage                          | -0.2 | -3.8 |                                      |  |
| D<br>Y<br>N<br>A<br>M<br>I<br>C                      | 6  I <sub>G</sub> Gate Operating Current                        |      | -15  | pA                                   | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$<br>125°C  |
|  | 7  I <sub>DSS</sub> Saturation Drain Current                    | 0.7  | 7    | mA                                   |  |
|  | 8  g <sub>fs</sub> Common-Source Forward Transconductance       | 1000 | 4000 | $\mu\text{mho}$                      | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0<br>V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$<br>V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0<br>V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$ |
|  | 9  g <sub>fs</sub> Common-Source Forward Transconductance       | 700  | 1600 |                                      |  |
|  | 10  g <sub>os</sub> Common-Source Output Conductance            |      | 50   |                                      |  |
| 11  g <sub>os</sub> Common-Source Output Conductance |   | 4    |      |                                      |  |
| 12  C <sub>iss</sub> Common-Source Input Capacitance |   | 6    |      |                                      |  |
| M<br>A<br>T<br>C<br>H<br>I<br>N<br>G                 | 13  C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |      | 2    | pF                                   | f = 1 MHz  |
|  | 14  NF Spot Noise Figure  |      | 0.5  | dB                                   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0<br>f = 100 Hz, R <sub>G</sub> = 10 M $\Omega$  |
|  | 15   $\bar{e}_n$ Equivalent Short-Circuit Input Noise Voltage   |      | 20   | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ | f = 1 kHz  |

| Characteristic  | 2N5196 |     | 2N5197 |     | 2N5198 |     | 2N5199 |     | Unit                         | Test Conditions  |
|---|--------|-----|--------|-----|--------|-----|--------|-----|------------------------------|--|
|   | Min    | Max | Min    | Max | Min    | Max | Min    | Max |                              |  |
| 16  I <sub>G1</sub> -I <sub>G2</sub>   Differential Gate Current  |        | 5   |        | 5   |        | 5   |        | 5   | nA                           | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$<br>125°C  |
| 17  I <sub>DSS1</sub> /I <sub>DSS2</sub> Saturation Drain Current Ratio (Note 1)                                | 0.95   | 1   | 0.95   | 1   | 0.95   | 1   | 0.95   | 1   | -                            | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 18  g <sub>fs1</sub> /g <sub>fs2</sub> Transconductance Ratio (Note 1)  | 0.97   | 1   | 0.97   | 1   | 0.95   | 1   | 0.95   | 1   | -                            | f = 1 kHz  |
| 19  V <sub>GS1</sub> -V <sub>GS2</sub>   Differential Gate-Source Voltage                                       |        | 5   |        | 5   |        | 10  |        | 15  | mV                           | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$<br>T <sub>A</sub> = 25°C<br>T <sub>B</sub> = 125°C<br>T <sub>A</sub> = -55°C<br>T <sub>B</sub> = 25°C |
| 20 $\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$ Gate-Source Differential Voltage Change with Temperature (Note 2) |        | 5   |        | 10  |        | 20  |        | 40  | $\mu\text{V}/^\circ\text{C}$ |  |
| 22  g <sub>os1</sub> -g <sub>os2</sub>   Differential Output Conductance  |        | 1   |        | 1   |        | 1   |        | 1   | $\mu\text{mho}$              |  |

\*JEDEC registered data.

**NOTES:**

1. Assumes smaller value in numerator.
2. Measured at end points, T<sub>A</sub> and T<sub>B</sub>.

NNP  
NP-D

# n-channel JFETs designed for . . .



**Performance Curves NIP**  
See Section 5

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

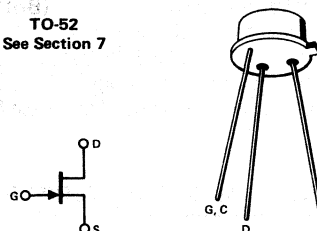
**BENEFITS**

- Low Insertion Loss  
 $R_{DS(on)} < 5 \Omega$  (2N5432)
- Small Error in Measurement Systems  
 $V_{DS(on)} < 50 \text{ mV}$  (2N5432)
- High Off-Isolation  
 $I_{D(off)} < 200 \text{ pA}$
- High Speed  
 $t_{d(on)} < 4 \text{ ns}$
- Low Noise Audio-Frequency Amplification  
 $e_n < 2 \text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz Typical

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . -25 V  
 Gate Current . . . . . 100 mA  
 Drain Current . . . . . 400 mA  
 Total Device Dissipation at 25°C  
 Free-Air Temperature (Note 1) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +150°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-52  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

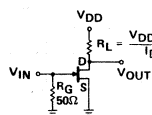
| Characteristic  | 2N5432 |      | 2N5433 |      | 2N5434 |      | Unit | Test Conditions  |
|---|--------|------|--------|------|--------|------|------|--|
|   | Min    | Max  | Min    | Max  | Min    | Max  |      |  |
| 1   $I_{GSS}$   Gate Reverse Current                        |        | -200 |        | -200 |        | -200 | pA   | $V_{GS} = -15 \text{ V}, V_{DS} = 0$<br>150°C  |
| 2   $BV_{GSS}$   Gate Source Breakdown Voltage              | -25    |      | -25    |      | 25     |      | V    | $I_G = -1 \mu\text{A}, V_{DS} = 0$   |
| 3   $I_{D(off)}$   Drain Cutoff Current                     |        | 200  |        | 200  |        | 200  | pA   | $V_{DS} = 5 \text{ V}, V_{GS} = -10 \text{ V}$<br>150°C  |
| 4   $I_{D(off)}$   Drain Cutoff Current                     |        | 200  |        | 200  |        | 200  | nA   |  |
| 5   $V_{GS(off)}$   Gate-Source Cutoff Voltage              | -4     | -10  | -3     | -9   | -1     | -4   | V    | $V_{DS} = 5 \text{ V}, I_D = 3 \text{ nA}$   |
| 6   $I_{DSS}$   Saturation Drain Current (Note 2)           | 150    |      | 100    |      | 30     |      | mA   | $V_{DS} = 15 \text{ V}, V_{GS} = 0$  |
| 7   $r_{DS(on)}$   Static Drain-Source ON Resistance        | 2      | 5    |        | 7    |        | 10   | ohm  | $V_{GS} = 0, I_D = 10 \text{ mA}$  |
| 8   $V_{DS(on)}$   Drain-Source ON Voltage                  |        | 50   |        | 70   |        | 100  | mV   |  |
| 9   $r_{ds(on)}$   Drain-Source ON Resistance               |        | 5    |        | 7    |        | 10   | ohm  | $V_{GS} = 0, I_D = 0$<br>f = 1 kHz   |
| 10   $C_{iss}$   Common-Source Input Capacitance            |        | 30   |        | 30   |        | 30   | pF   | $V_{DS} = 0, V_{GS} = -10 \text{ V}$<br>f = 1 MHz  |
| 11   $C_{rss}$   Common-Source Reverse Transfer Capacitance |        | 15   |        | 15   |        | 15   |      |  |
| 12   $t_{d(on)}$   Turn-ON Delay Time                       |        | 4    |        | 4    |        | 4    | ns   | $V_{DD} = 1.5 \text{ V},$<br>$V_{GS(on)} = 0,$<br>$V_{GS(off)} = -12 \text{ V},$<br>$I_{D(on)} = 10 \text{ mA}$<br>$R_L = 143 \Omega$ (2N5433)<br>$145 \Omega$ (2N5432)<br>$140 \Omega$ (2N5434) |
| 13   $t_r$   Rise Time                                      |        | 1    |        | 1    |        | 1    |      |  |
| 14   $t_{d(off)}$   Turn-OFF Delay Time                     |        | 6    |        | 6    |        | 6    |      |  |
| 15   $t_f$   Fall Time                                      |        | 30   |        | 30   |        | 30   |      |  |

\*JEDEC registered data.

NIP

**NOTES:**

1. Derate linearly at the rate of 2.3 mW/°C.
2. Pulse test required pulsewidth 300  $\mu\text{s}$ , duty cycle  $\leq$  3%.



**INPUT PULSE**  
 RISE TIME 0.25 ns  
 FALL TIME 0.75 ns  
 PULSE WIDTH 200 ns  
 PULSE RATE 550 pps

**SAMPLING SCOPE**  
 RISE TIME 0.4 ns  
 INPUT RESISTANCE 10 M  
 INPUT CAPACITANCE 1.5 pF

2N5432 2N5433 2N5434

3

Siliconix

# matched dual n-channel JFETs designed for . . .



Performance Curves NFA  
See Section 5

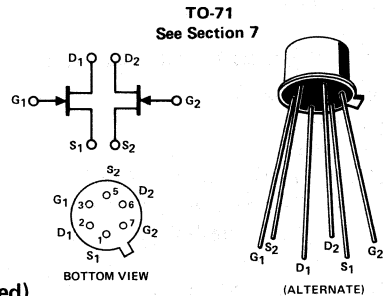
## Low and Medium Frequency Differential Amplifiers

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|   |               |
|---|---------------|
| Any Lead-To-Case Voltage . . . . .                          | ±100 V        |
| Gate-Drain or Gate-Source Voltage . . . . .                 | -50 V         |
| Gate-To-Gate Voltage . . . . .                              | ±100 V        |
| Gate Current . . . . .                                      | 50 mA         |
| Total Device Dissipation 85°C (Each Side) . . . . .         | 250 mW        |
| Case Temperature (Both Sides) . . . . .                     | 500 mW        |
| Power Derating (Each Side) . . . . .                        | 2.86 mW/°C    |
| (Both Sides) . . . . .                                      | 4.3 mW/°C     |
| Storage Temperature Range . . . . .                         | -65 to +250°C |
| Lead Temperature (1/16" from case for 10 seconds) . . . . . | 300°C         |

### BENEFITS

- Minimum System Error and Calibration  
5 mV Offset Maximum (2N5452)
- Simplifies Amplifier Design  
Output Conductance Less than  
1 μmho



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | 2N5452 |      | 2N5453 |      | 2N5454 |      | Unit   | Test Conditions  |
|--|--------|------|--------|------|--------|------|--------|--|
|  | Min    | Max  | Min    | Max  | Min    | Max  |        |  |
| 1   I <sub>GSS</sub>   Gate Reverse Current  |        | -100 |        | -100 |        | -100 | pA     | V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V<br>T <sub>A</sub> = 150°C                   |
|  | 2      | -200 | -200   | -200 |        |      | nA     |  |
| 3   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage  | -50    |      | -50    |      | -50    |      | V      | V <sub>DS</sub> = 0 V, I <sub>G</sub> = -1 μA  |
| 4   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage  | -1     | -4.5 | -1     | -4.5 | -1     | -4.5 |        | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA  |
| 5   V <sub>GS</sub>   Gate-Source Voltage  | -0.2   | -4.2 | -0.2   | -4.2 | -0.2   | -4.2 |        | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 50 μA   |
| 6   V <sub>GS(f)</sub>   Gate-Source Forward Voltage   |        | 2    |        | 2    |        | 2    |        | V <sub>DS</sub> = 0 V, I <sub>G</sub> = 1 mA   |
| 7   I <sub>DSS</sub>   Drain Saturation Current  | 0.5    | 5.0  | 0.5    | 5.0  | 0.5    | 5.0  | mA     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 8   g <sub>fs</sub>   Common-Source Forward Transconductance   | 1000   | 3000 | 1000   | 3000 | 1000   | 3000 | μmho   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V<br>f = 1 kHz                                 |
|  | 9      | 1000 | 1000   | 1000 |        |      |        | f = 100 MHz  |
| 10   g <sub>os</sub>   Common-Source Output Conductance  |        | 3.0  |        | 3.0  |        | 3.0  | pF     | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA<br>f = 1 kHz                               |
| 11   C <sub>iss</sub>   Common-Source Input Capacitance  |        | 4.0  |        | 4.0  |        | 4.0  |        | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V<br>f = 1 MHz                                 |
| 12   C <sub>rss</sub>   Common-Source Reverse Transfer Capacitance                                   |        | 1.2  |        | 1.2  |        | 1.2  | pF     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V<br>f = 1 MHz                                 |
| 13   C <sub>dgo</sub>   Drain-Gate Capacitance   |        | 1.5  |        | 1.5  |        | 1.5  |        | V <sub>DG</sub> = 10 V, I <sub>S</sub> = 0 V   |
| 14   ē <sub>n</sub>   Equivalent Short Circuit Input Noise Voltage                                   |        | 20   |        | 20   |        | 20   | nV/√Hz | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V<br>f = 1 kHz                                 |
| 15   NF   Common-Source Spot Noise Figure  |        | 0.5  |        | 0.5  |        | 0.5  | dB     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, R <sub>G</sub> = 10 MΩ<br>f = 100 Hz        |
| 16   I <sub>DSS1</sub> /I <sub>DSS2</sub>   Drain Saturation Current Ratio (Note 1)                  | 0.95   | 1.0  | 0.95   | 1.0  | 0.95   | 1.0  | -      | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 17    V <sub>GS1</sub> -V <sub>GS2</sub>     Differential Gate-Source Voltage                        |        | 5.0  |        | 10.0 |        | 15.0 | mV     | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA<br>T = 25°C to -55°C<br>T = 25°C to +125°C |
| 18   ΔI <sub>VGS1</sub> -V <sub>GS2</sub>   Gate-Source Voltage Differential Change with Temperature |        | 0.4  |        | 0.8  |        | 2.0  |        |  |
| 19   |        | 0.5  |        | 1.0  |        | 2.5  |        |  |
| 20   g <sub>fs1</sub> /g <sub>fs2</sub>   Transconductance Ratio (Note 1)                            | 0.97   | 1.0  | 0.97   | 1.0  | 0.95   | 1.0  |        |  |
| 21    g <sub>os1</sub> -g <sub>os2</sub>     Differential Output Conductance                         |        | 0.25 |        | 0.25 |        | 0.25 | μmhos  | f = 1 kHz  |

\*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NFA

# matched dual n-channel JFETs designed for . . .

## ■ Differential Amplifiers

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|  |               |
|--|---------------|
| Gate-Drain or Gate-Source Voltage  | -40 V         |
| Gate Current   | 50 mA         |
| Device Dissipation (Each Side), $T_A = 85^\circ\text{C}$<br>(Derate 2.0 mW/°C) | 250 mW        |
| Total Device Dissipation, $T_A = 85^\circ\text{C}$<br>(Derate 3.0 mW/°C)       | 375 mW        |
| Storage Temperature Range  | -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 30 seconds)                           | 300°C         |

### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| 1                          | Characteristic   | Min  | Max       | Unit            | Test Conditions                                |                                      |  |
|----------------------------|--|--|-----------|-----------------|--|--------------------------------------|--|
|                            |  |  |           |                 |  |                                      |  |
| S<br>T<br>A<br>T<br>I<br>C | $I_{GSS}$ Gate Reverse Current                           |  | -250      | pA              | $V_{GS} = -30\text{ V}, V_{DS} = 0$            |                                      |  |
|                            | $BV_{GSS}$ Gate-Source Breakdown Voltage                 | -40  | -250      | nA              | 150°C  |                                      |  |
|                            | $V_{GS(off)}$ Gate-Source Cutoff Voltage                 | -0.7   | -4        | V               | $I_G = -1\ \mu\text{A}, V_{DS} = 0$            |                                      |  |
|                            | $V_{GS}$ Gate Source Voltage                             | -0.2   | -3.8      |                 | $V_{DS} = 20\text{ V}, I_D = 1\ \text{nA}$     |                                      |  |
|                            | $I_G$ Gate Operating Current                             |  | -100      | pA              | $V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$ |                                      |  |
| D<br>V<br>N<br>A<br>I<br>C | $I_{DSS}$ Saturation Drain Current (Note 1)              | 0.5  | 7.5       | mA              | $V_{DS} = 20\text{ V}, V_{GS} = 0$             |                                      |  |
|                            | $g_{fs}$ Common-Source Forward Transconductance (Note 1) | 1000   | 4000      | $\mu\text{mho}$ | $V_{DS} = 20\text{ V}, V_{GS} = 0$             |                                      |  |
|                            | $g_{fs}$ Common-Source Forward Transconductance (Note 1) | 500  | 1000      |                 | $V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$ |                                      |  |
|                            | $g_{os}$ Common-Source Output Conductance                |  | 10        |                 | $V_{DS} = 20\text{ V}, V_{GS} = 0$             |                                      |  |
|                            | $g_{os}$ Common-Source Output Conductance                |  | 1         |                 | $V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$ |                                      |  |
|                            | $C_{iss}$ Common-Source Input Capacitance                |  | 25        | pF              | $V_{DS} = 20\text{ V}, V_{GS} = 0$             |                                      |  |
|                            | $C_{rss}$ Common-Source Reverse Transfer Capacitance     |  | 5         |                 | f = 1 MHz                                      |                                      |  |
|                            | $\bar{e}_n$  | Equivalent Short Circuit Input Noise Voltage | 2N5515-19 |                 | 30   | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ | $V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$ |
|                            |  |  | 2N5520-24 |                 | 15   |                                      |  |
|                            |  |  | 2N5515-24 |                 | 10   |                                      |  |

| Characteristic   | 2N5515,20 |     | 2N5516,21 |     | 2N5517,22 |     | 2N5518,23 |     | 2N5519,24 |     | Unit                         | Test Conditions   |       |   |
|--|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------------------------------|---|-------|---|
|  | Min       | Max | Min       | Max | Min       | Max | Min       | Max | Min       | Max |                              |   |       |   |
| $ I_{G1} - I_{G2} $ Differential Gate Current                                |           | 10  |           | 10  |           | 10  |           | 10  |           | 10  | nA                           | $V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$              | 125°C |   |
| $I_{DSS1}$<br>$I_{DSS2}$ Saturation Drain Current Ratio (Notes 1 and 2)      | 0.95      | 1   | 0.95      | 1   | 0.95      | 1   | 0.95      | 1   | 0.90      | 1   | -                            | $V_{DS} = 20\text{ V}, V_{GS} = 0$                          |       |   |
| $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage                       |           | 5   |           | 5   |           | 10  |           | 15  |           | 15  | mV                           | $V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$              |       |   |
| $ \Delta V_{GS1} - V_{GS2} $ Gate-Source Voltage Differential Drift (Note 3) |           | 5   |           | 10  |           | 20  |           | 40  |           | 80  | $\mu\text{V}/^\circ\text{C}$ |   |       | $T_A = 25^\circ\text{C}$<br>$T_B = 125^\circ\text{C}$ |
| $\Delta T$   |           | 5   |           | 10  |           | 20  |           | 40  |           | 80  | $\mu\text{V}/^\circ\text{C}$ |   |       | $T_A = -55^\circ\text{C}$<br>$T_B = 25^\circ\text{C}$ |
| $ g_{os1} - g_{os2} $ Differential Output Conductance                        |           | 0.1 |           | 0.1 |           | 0.1 |           | 0.1 |           | 0.1 | $\mu\text{mho}$              | f = 1 kHz   |       |   |
| $\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Notes 1 and 2)             | 0.97      | 1   | 0.97      | 1   | 0.95      | 1   | 0.95      | 1   | 0.90      | 1   | -                            |   |       |   |
| CMRR Common Mode Rejection Ratio (Note 4)                                    | 100       |     | 100       |     | 90        |     |           |     |           |     | dB                           | $V_{DD} = 10\text{ to }20\text{ V}, I_D = 200\ \mu\text{A}$ |       |   |

\*JEDEC registered data.

NOTES:

- Pulse test required, pulsewidth = 300  $\mu\text{s}$ , duty cycle  $\leq 3\%$ .
- Assumes smaller value in numerator.

3. Measured at end points,  $T_A$  and  $T_B$ .

4.  $CMRR = 20 \log_{10} \left( \frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right), \Delta V_{DD} = 10\text{ V}.$

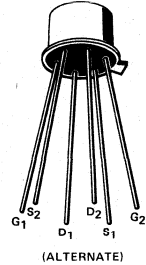
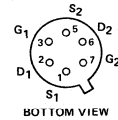
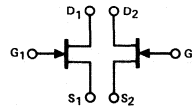
NS

### Performance Curves NS See Section 5

#### BENEFITS

- Ultra-Low Noise  
 $\bar{e}_n = 8\text{ nV}/\sqrt{\text{Hz}}$  at 10 Hz (Typical)  
 $\bar{e}_n = 2\text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz (Typical)
- Minimum System Error and Calibration  
 5 mV Offset Maximum  
 CMRR > 100 dB

TO-71  
See Section 7



2N5515 2N5516 2N5517 2N5518 2N5519  
2N5520 2N5521 2N5522 2N5523 2N5524

3

Siliconix

# monolithic dual n-channel JFETs designed for . . .



## Performance Curves NNP See Section 5

### BENEFITS

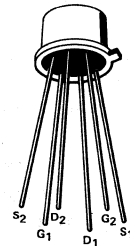
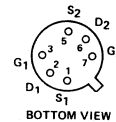
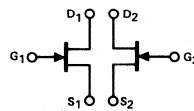
- High Input Impedance  
 $I_G < 50 \text{ pA}$
- Minimum System Error and Calibration  
5 mV Offset Maximum (2N5545)

## ■ General Purpose Differential Amplifiers

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|   |       |               |
|---|-------|---------------|
| Gate-Drain or Gate-Source Voltage   | ..... | -50 V         |
| Gate Current  | ..... | 30 mA         |
| Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$<br>(Derate 1.67 mW/°C) | ..... | 250 mW        |
| Total Device Dissipation, $T_A = 25^\circ\text{C}$<br>(Derate 2.67 mW/°C)       | ..... | 400 mW        |
| Storage Temperature Range   | ..... | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 30 seconds)                            | ..... | 300°C         |

TO-71  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                  |   | Min  | Max  | Unit                          | Test Conditions                                |                                  |
|---------------------------------|---|------|------|-------------------------------|--|----------------------------------|
| S<br>T<br>A<br>T<br>I<br>C      | 1 $I_{GSS}$ Gate Reverse Current                            |      | -100 | pA                            | $V_{GS} = -30 \text{ V}, V_{DS} = 0$           | $T_A = 150^\circ\text{C}$        |
|                                 | 2   |      | -150 | nA                            |  |                                  |
|                                 | 3 $BV_{GSS}$ Gate-Source Breakdown Voltage                  | -50  |      | V                             | $I_G = -1 \mu\text{A}, V_{DS} = 0$             |                                  |
|                                 | 4 $V_{GS(off)}$ Gate-Source Cutoff Voltage                  | -0.5 | -4.5 |                               | $V_{DS} = 15 \text{ V}, I_D = 0.5 \text{ nA}$  |                                  |
|                                 | 5 $I_G$ Gate Operating Current                              |      | -50  | pA                            | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$ |                                  |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | 6 $I_{DSS}$ Saturation Drain Current                        | 0.5  | 8    | mA                            | $V_{DS} = 15 \text{ V}, V_{GS} = 0$            |                                  |
|                                 | 7 $g_{fs}$ Common-Source Forward Transconductance           | 1500 | 6000 | $\mu\text{mho}$               | $V_{DS} = 15 \text{ V}, V_{GS} = 0$            | $f = 1 \text{ kHz}$              |
|                                 | 8 $g_{os}$ Common-Source Output Conductance                 |      | 25   |                               |  | $f = 1 \text{ MHz}$              |
|                                 | 9 $C_{iss}$ Common-Source Input Capacitance                 |      | 6    | pF                            |  |                                  |
|                                 | 10 $C_{rss}$ Common-Source Reverse Transfer Capacitance     |      | 2    |                               |  |                                  |
|                                 | 11 NF Spot Noise Figure                                     |      | 3.5  | dB                            | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$ | 2N5545 $f = 10 \text{ Hz}$       |
|                                 |   |      | 5    |                               |  | 2N5546 $R_G = 1 \text{ M}\Omega$ |
|                                 | 12 $\bar{e}_n$ Equivalent Short Circuit Input Noise Voltage |      | 180  | $\frac{nV}{\sqrt{\text{Hz}}}$ | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$ | 2N5545 $f = 10 \text{ Hz}$       |
|                                 |   | 200  |      | 2N5546                        |  |                                  |

| Characteristic   | 2N5545 |     | 2N5546 |     | 2N5547 |     | Unit                         | Test Conditions   |
|--|--------|-----|--------|-----|--------|-----|------------------------------|---|
|  | Min    | Max | Min    | Max | Min    | Max |                              |   |
| 13 $ I_{G1} - I_{G2} $ Differential Gate Current   |        | 5   |        | 5   |        | 5   | nA                           | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}, T_A = 125^\circ\text{C}$ |
| 14 $\frac{I_{DSS1}}{I_{DSS2}}$ Saturation Drain Current Ratio (Note 1)                           | 0.95   | 1   | 0.90   | 1   | 0.90   | 1   | -                            | $V_{DS} = 15 \text{ V}, V_{GS} = 0$                                     |
| 15 $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage  |        | 5   |        | 10  |        | 15  | mV                           | $V_{DG} = 15 \text{ V}$   |
|  |        | 5   |        | 10  |        | 15  |                              | $I_D = 50 \mu\text{A}$<br>$I_D = 200 \mu\text{A}$                       |
| 16 $\frac{\Delta  V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 2) |        | 10  |        | 20  |        | 40  | $\mu\text{V}/^\circ\text{C}$ | $T_A = 25^\circ\text{C}$<br>$T_B = 125^\circ\text{C}$                   |
|  |        | 10  |        | 20  |        | 40  |                              | $T_A = -55^\circ\text{C}$<br>$T_B = 25^\circ\text{C}$                   |
| 17 $\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Note 1)                                     | 0.97   | 1   | 0.95   | 1   | 0.90   | 1   | -                            | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$                          |
| 18 $ g_{os1} - g_{os2} $ Differential Output Conductance   |        | 1   |        | 2   |        | 3   | $\mu\text{mho}$              | $f = 1 \text{ kHz}$   |

\*JEDEC registered data.

#### NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points,  $T_A$  and  $T_B$ .

NNP  
NP-D



# n-channel JFETs designed for . . .



Performance Curves NRL  
See Section 5

## ■ General Purpose Amplifiers

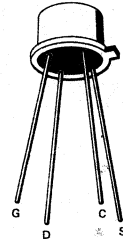
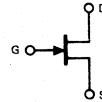
### BENEFITS

- Low Noise
- Low Output Conductance

### \*ABSOLUTE MAXIMUM RATINGS (at 25°C)

|   |               |
|---|---------------|
| Gate-Drain or Gate-Source Voltage (Note 1)              | -30 V         |
| Gate Current  | 10 mA         |
| Total Device Dissipation<br>(25°C Free Air Temperature) | 300 mW        |
| Power Derating (to +175°C)                              | 2.0 mW/°C     |
| Storage Temperature Range                               | -65 to +200°C |
| Operating Temperature Range                             | -65 to +175°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)    | 240°C         |

TO-72  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic | 2N5556 |                                   | 2N5557                                 |                               | 2N5558   |      | Unit | Test Conditions        |           |      |                       |                       |           |                       |            |
|----------------|--------|-----------------------------------|--|-------------------------------|--|------|------|------------------------|-----------|------|-----------------------|-----------------------|-----------|-----------------------|------------|
|                | Min    | Max                               | Min                                    | Max                           | Min  | Max  |      |                        |           |      |                       |                       |           |                       |            |
| STATIC         | IGSS   | Gate Reverse Current              |  | -0.1                          | -0.1   | -0.1 | nA   | VGS = -15 V, VDS = 0 V | T = 150°C |      |                       |                       |           |                       |            |
|                |        | VGS(off)                          | Gate-Source Cutoff Voltage             |                               | -0.2   | -4.0 |      |                        |           | -0.8 | 5.0                   | -1.5                  | -6.0      | VDS = 15 V, ID = 1 nA |            |
|                |        |                                   | BVGSS                                  | Gate-Source Breakdown Voltage |  | -30  |      |                        |           |      | -30                   |                       | -30       |                       |            |
| 5              | IDSS   | Saturation Drain Current (Note 2) |  | 0.5                           | 2.5  | 2.0  | 5.0  | 4.0                    | 10.0      | mA   | VDG = 15 V, VGS = 0 V |                       |           |                       |            |
| DYNAMIC        | 6      | gfs                               | Common-Source Forward Transconductance |                               | 1500   | 6500 | 1500 | 6500                   | 1500      | 6500 | μmho                  | VDS = 15 V, VGS = 0 V | f = 1 kHz |                       |            |
|                |        |                                   | 7                                      | gos                           | Common-Source Output Conductance                           |      |      | 20                     |           | 20   |                       |                       |           |                       | 20         |
|                | 8      | Crss                              |  |                               | Common-Source Reverse Transfer Capacitance                 |      |      | 3                      |           | 3    |                       |                       |           |                       | 3          |
|                |        |                                   | 9                                      | Ciss                          | Common-Source Input Capacitance                            |      |      | 6                      |           | 6    |                       |                       |           |                       | 6          |
|                | 10     | ēn                                |  |                               | Common-Source Equivalent Short Circuit Input Noise Voltage |      |      | 35                     |           | 35   |                       |                       |           |                       | 35         |
|                |        |                                   | 11                                     | NF                            | Noise Figure   |      |      | 20                     |           | 20   |                       |                       |           |                       | 20         |
| 12             | NF     | Noise Figure                      |  |                               |  | 1    |      | 1                      |           | 1    | dB                    | f = 10 Hz             |           |                       |            |
|                |        | 13                                | NF                                     | Noise Figure                  |  |      | 1    |                        | 1         |      |                       |                       | 1         | dB                    | f = 100 Hz |

\*JEDEC registered data

#### NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Pulse test duration ≤ 2 ms.

NRL

2N5556 2N5557 2N5558

3

Siliconix

# matched dual n-channel JFETs designed for . . .



**Performance Curves NC**  
See Section 5

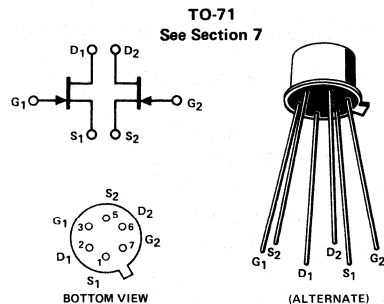
- **Wideband Differential Amplifiers**
- **Commutators**

**BENEFITS**

- High Gain  
7500  $\mu\text{mho}$  Minimum  $g_{fs}$
- Specified Matching Characteristics

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |               |
|--|---------------|
| Gate-Gate Voltage  | ±80 V         |
| Gate-Drain or Gate-Source Voltage  | -40 V         |
| Gate Current   | 50 mA         |
| Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$<br>(Derate 2.2 mW/°C) | 325 mW        |
| Total Device Dissipation, $T_A = 25^\circ\text{C}$<br>(Derate 3.3 mW/°C)       | 650 mW        |
| Storage Temperature Range  | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)                           | 300°C         |



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                  |  | Min  | Max    | Unit                   | Test Conditions                              |                                      |
|---------------------------------|--|------|--------|------------------------|--|--------------------------------------|
| S<br>T<br>A<br>T<br>I<br>C      | $I_{GSS}$ Gate-Reverse Current                           |      | -100   | pA                     | $V_{GS} = -20\text{ V}, V_{DS} = 0$<br>150°C |                                      |
|                                 | $BV_{GSS}$ Gate-Source Breakdown Voltage                 | -40  | -200   | nA                     |  |                                      |
|                                 | $V_{GS(off)}$ Gate-Source Cutoff Voltage                 | -0.5 | -3     | V                      | $I_G = -1\ \mu\text{A}, V_{DS} = 0$          |                                      |
|                                 | $V_{GS(f)}$ Gate-Source Voltage                          | 1.0  |        |                        | $V_{DS} = 15\text{ V}, I_D = 1\text{ nA}$    |                                      |
|                                 | $I_{DSS}$ Saturation Drain Current (Note 1)              | 5    | 30     | mA                     | $V_{DS} = 0\text{ V}, I_G = 2\text{ mA}$     |                                      |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | $r_{DS(on)}$ Static Drain Source ON Resistance           |      | 100    | $\Omega$               | $I_D = 1\text{ mA}, V_{GS} = 0$              |                                      |
|                                 | $g_{fs}$ Common-Source Forward Transconductance (Note 1) | 7500 | 12,500 | $\mu\text{mho}$        | $V_{DG} = 15\text{ V}, I_D = 2\text{ mA}$    | $f = 1\text{ kHz}$                   |
|                                 |  | 7000 |        |                        |  | $f = 100\text{ MHz}$                 |
|                                 | $g_{os}$ Common-Source Output Conductance                |      | 45     |                        |  | $f = 1\text{ kHz}$                   |
|                                 | $C_{rss}$ Common-Source Reverse Transfer Capacitance     |      | 3      | pF                     |  | $f = 1\text{ MHz}$                   |
|                                 | $C_{iss}$ Common-Source Input Capacitance                |      | 12     |                        |  | $f = 10\text{ Hz}, R_g = 1\text{ M}$ |
|                                 | NF Spot Noise Figure                                     |      | 1.0    | dB                     |  | $f = 10\text{ Hz}$                   |
|                                 | $\bar{e}_n$ Equivalent Short Circuit Input Noise Voltage |      | 50     | $\frac{nV}{\sqrt{Hz}}$ |  | $f = 10\text{ Hz}$                   |

| Characteristics  | 2N5564 |     | 2N5565 |     | 2N5566 |     | Unit                         | Test Conditions                                       |
|--|--------|-----|--------|-----|--------|-----|------------------------------|---|
|  | Min    | Max | Min    | Max | Min    | Max |                              |   |
| $I_{DSS1}$<br>$I_{DSS2}$ Saturation Drain Current Ratio (Notes 1 and 2)                      | 0.95   | 1   | 0.95   | 1   | 0.95   | 1   | -                            | $V_{DS} = 15\text{ V}, V_{GS} = 0$                    |
|  |        |     |        |     |        |     |                              |   |
| $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage                                       |        | 5   |        | 10  |        | 20  | mV                           | $V_{DS} = 15\text{ V}, I_D = 2\text{ mA}$             |
| $\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 3) |        | 10  |        | 25  |        | 50  | $\mu\text{V}/^\circ\text{C}$ |   |
|  |        | 10  |        | 25  |        | 50  |                              |   |
| $\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Notes 1 and 2)                             | 0.95   | 1   | 0.90   | 1   | 0.90   | 1   | -                            | $T_A = 25^\circ\text{C}$<br>$T_B = 125^\circ\text{C}$ |
|  |        |     |        |     |        |     |                              | $T_A = -55^\circ\text{C}$<br>$T_B = 25^\circ\text{C}$ |
|  |        |     |        |     |        |     |                              | $f = 1\text{ kHz}$                                    |

\*JEDEC registered data.

**NOTES:**

1. Pulse test required, pulse width 300  $\mu\text{s}$ , duty cycle  $\leq 3\%$ .
2. Assumes smaller value in numerator.
3. Measured at ends points,  $T_A$  and  $T_B$ .

NC

# matched dual n-channel JFETs designed for . . .



**Performance Curves NT**  
See Section 5

- Differential Amplifiers
- High Input Impedance Amplifiers

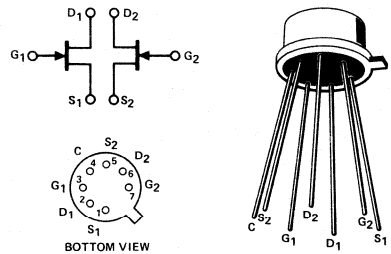
**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |               |
|--|---------------|
| Gate-to-Gate Voltage   | ±80 V         |
| Gate-Drain or Gate-Source Voltage  | -40 V         |
| Gate Current   | 10 mA         |
| Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$<br>(Derate 3 mW/°C) | 367 mW        |
| Total Device Dissipation, $T_A = 25^\circ\text{C}$<br>(Derate 4 mW/°C)       | 500 mW        |
| Storage Temperature Range  | -65 to +150°C |

**BENEFITS**

- Matching Characteristics Specified
- High Input Impedance  
 $I_G = 1 \text{ pA Max (2N5906-9)}$

**TO-78**  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                                     | 2N5902-5 |      | 2N5906-9 |      | Unit   | Test Conditions   |
|--|----------|------|----------|------|--------|---|
|  | Min      | Max  | Min      | Max  |        |   |
| 1  GSS  Gate Reverse Current                       |          | -5   |          | -2   | pA     | $V_{GS} = -20 \text{ V}, V_{DS} = 0$<br>125°C                                     |
|  |          | -10  |          | -5   |        |   |
| 3 BVGSS Gate-Source Breakdown Voltage              | -40      |      | -40      |      | V      | $I_G = -1 \mu\text{A}, V_{DS} = 0$<br>$V_{DS} = 10 \text{ V}, I_D = 1 \text{ nA}$ |
| 4  VGS(off)  Gate-Source Cutoff Voltage            | -0.6     | -4.5 | -0.6     | -4.5 |        |   |
| 5 VGS Gate Source Voltage                          |          | -4   |          | -4   | pA     | $V_{DG} = 10 \text{ V}, I_D = 30 \mu\text{A}$<br>125°C                            |
| 6 IG Gate Operating Current                        |          | -3   |          | -1   |        |   |
| 8 IDSS Saturation Drain Current                    | 30       | 500  | 30       | 500  | μA     | $V_{DS} = 10 \text{ V}, V_{GS} = 0$<br>f = 1 kHz                                  |
| 9 gfs Common-Source Forward Transconductance       | 70       | 250  | 70       | 250  |        |   |
| 10 gos Common-Source Output Conductance            |          | 5    |          | 5    | pF     | f = 1 MHz   |
| 11 Ciss Common-Source Input Capacitance            |          | 3    |          | 3    |        |   |
| 12 Crss Common-Source Reverse Transfer Capacitance |          | 1.5  |          | 1.5  | μmho   | $V_{DG} = 10 \text{ V}, I_D = 30 \mu\text{A}$<br>f = 1 kHz                        |
| 13 gfs Common-Source Forward Transconductance      | 50       | 150  | 50       | 150  |        |   |
| 14 gos Common-Source Output Conductance            |          | 1    |          | 1    | μV/√Hz | $V_{DS} = 10 \text{ V}, V_{GS} = 0$<br>f = 100 Hz,<br>RG = 10 M                   |
| 15 ēn Equivalent Short Circuit Input Noise Voltage |          | 0.2  |          | 0.1  |        |   |
| 16 NF Spot Noise Figure                            |          | 3    |          | 1    | dB     |   |

| Characteristic  | 2N5902, 6 |     | 2N5903, 7 |     | 2N5904, 8 |     | 2N5905, 9 |     | Unit  | Test Conditions  |
|---|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-------|--|
|   | Min       | Max | Min       | Max | Min       | Max | Min       | Max |       |  |
| 17  IG1-IG2  Differential Gate Current                          |           | 2.0 |           | 2.0 |           | 2.0 |           | 2.0 | nA    | $V_{DG} = 10 \text{ V}, I_D = 30 \mu\text{A}, T_A = 125^\circ\text{C}$ |
|   |           | 0.2 |           | 0.2 |           | 0.2 |           | 0.2 |       |  |
| 19 IDSS1 / IDSS2 Saturation Drain Current Ratio (Note 1)        | 0.95      | 1   | 0.95      | 1   | 0.95      | 1   | 0.95      | 1   | -     | $V_{DS} = 10 \text{ V}, V_{GS} = 0$                                    |
|   |           |     |           |     |           |     |           |     |       |  |
| 20 gfs1 / gfs2 Transconductance Ratio (Note 1)                  | 0.97      | 1   | 0.97      | 1   | 0.95      | 1   | 0.95      | 1   | -     | f = 1 kHz  |
|   |           |     |           |     |           |     |           |     |       |  |
| 21  VGS1-VGS2  Differential Gate-Source Voltage                 |           | 5   |           | 5   |           | 10  |           | 15  | mV    | $V_{DG} = 10 \text{ V}, I_D = 30 \mu\text{A}$                          |
| 22 Δ VGS1-VGS2  Gate-Source Voltage Differential Drift (Note 2) |           | 5   |           | 10  |           | 20  |           | 40  |       |  |
| 23 ΔT Gate-Source Voltage Differential Drift (Note 2)           |           | 5   |           | 10  |           | 20  |           | 40  | μV/°C | $T_A = 25^\circ\text{C}$<br>$T_B = 125^\circ\text{C}$                  |
|   |           |     |           |     |           |     |           |     |       | $T_A = -55^\circ\text{C}$<br>$T_B = 25^\circ\text{C}$                  |
| 24  gos1-gos2  Differential Output Conductance                  |           | 0.2 |           | 0.2 |           | 0.2 |           | 0.2 | μmho  | f = 1 kHz  |

\*JEDEC registered data.

**NOTES:**

1. Assumes smaller value in numerator.
2. Measured at end points,  $T_A$  and  $T_B$ .

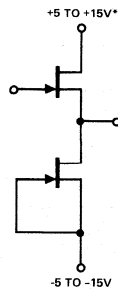
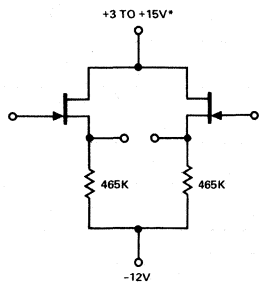
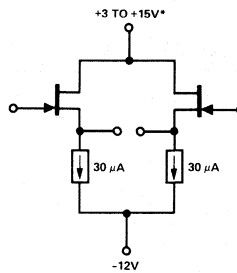
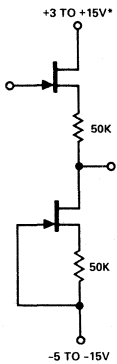
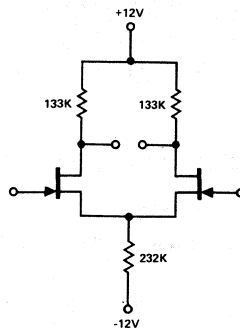
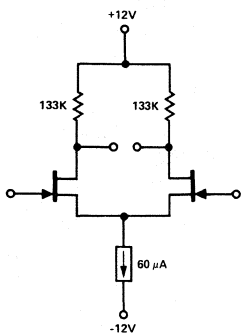
NT

2N5902 2N5903 2N5904 2N5905  
 2N5906 2N5907 2N5908 2N5909

3

Siliconix

APPLICATIONS



\*Use lower voltages for minimum  $I_G$

# matched dual n-channel JFETs designed for . . .



**Performance Curves NZF**  
See Section 5

**BENEFITS**

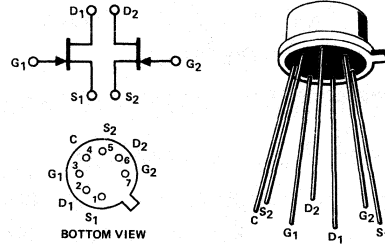
- High Gain through 100 MHz  
 $g_{fs} > 5000 \mu\text{mho}$
- Matching Characteristics Specified

■ **Wideband Differential Amplifiers**

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |               |
|--|---------------|
| Gate-to-Gate Voltage                                 | ±80 V         |
| Gate-Drain or Gate-Source Voltage                    | -25 V         |
| Gate Current   | 50 mA         |
| Device Dissipation (Each Side), (Derate 3 mW/°C)     | 367 mW        |
| Total Device Dissipation, (Derate 4 mW/°C)           | 500 mW        |
| Storage Temperature Range                            | -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) | 300°C         |

TO-78  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)**

| Characteristic                         |   | Min  | Max    | Unit                    | Test Conditions       |             |
|--|---|------|--------|-------------------------|-----------------------|-------------|
| S<br>T<br>A<br>T<br>I<br>C             | IGSS Gate Reverse Current                       |      | -100   | pA                      | VGS = -15 V, VDS = 0  | TA = 150°C  |
|  | BVGSS Gate-Source Breakdown Voltage             | -25  |        | nA                      |                       |             |
|  | VGS(off) Gate-Source Cutoff Voltage             | -1   | -5     | V                       | IG = -1 μA, VDS = 0   |             |
|  | VGS Gate-Source Voltage                         | -0.3 | -4     |                         | VDS = 10 V, ID = 1 nA |             |
|  | IG Gate Operating Current                       |      | -100   | pA                      | VDG = 10 V, ID = 5 mA | TA = 125°C  |
| IDSS Saturation Drain Current (Note 1) | 7   | 40   | nA     |                         |                       |             |
| D<br>Y<br>N<br>A<br>M<br>I<br>C        | gfs Common-Source Forward Transconductance      | 5000 | 10,000 | μmho                    | VDG = 10 V, ID = 5 mA | f = 1 kHz   |
|  | gfs Common-Source Forward Transconductance      | 5000 | 10,000 |                         |                       | f = 100 MHz |
|  | gos Common-Source Output Conductance            |      | 100    |                         |                       | f = 1 kHz   |
|  | gos Common-Source Output Conductance            |      | 150    |                         |                       | f = 100 MHz |
|  | Ciss Common-Source Input Capacitance            |      | 5      | pF                      |                       | f = 1 MHz   |
|  | Crss Common-Source Reverse Transfer Capacitance |      | 1.2    |                         |                       |             |
|  | en Equivalent Short Circuit Input Noise Voltage |      | 20     | nV/√Hz                  |                       | f = 10 kHz  |
| NF Spot Noise Figure                   |   | 1    | dB     | f = 10 kHz<br>RG = 100K |                       |             |

| Characteristic   | 2N5911 |     | 2N5912 |     | Unit  | Test Conditions                     |                         |
|--|--------|-----|--------|-----|-------|-------------------------------------|-------------------------|
|  | Min    | Max | Min    | Max |       |                                     |                         |
| 16  IG1-IG2  Differential Gate Current                               |        | 20  | 20     |     | nA    | VDG = 10 V, ID = 5 mA<br>TA = 125°C |                         |
| 17 IDSS1 / IDSS2 Saturation Drain Current Ratio (Notes 1 and 2)      | 0.95   | 1   | 0.95   | 1   | -     | VDG = 10 V, VGS = 0                 |                         |
| 18  VGS1-VGS2  Differential Gate-Source Voltage                      |        | 10  | 15     |     | mV    | VDG = 10 V, ID = 5 mA               |                         |
| 19 Δ VGS1-VGS2  / ΔT Gate-Source Voltage Differential Drift (Note 3) |        | 20  | 40     |     | μV/°C |                                     | TA = 25°C<br>TB = 125°C |
| 20   |        | 20  | 40     |     |       |                                     | TA = -55°C<br>TB = 25°C |
| 21 gfs1 / gfs2 Transconductance Ratio (Note 2)                       | 0.95   | 1   | 0.95   | 1   | -     | f = 1 kHz                           |                         |

\*JEDEC registered data.

**NOTES:**

1. Pulswidth ≤ 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, TA and TB.

NZF

2N5911 2N5912

3

Siliconix

# enhancement-type p-channel MOSFETs designed for . . .



**Performance Curves MRA**  
**See Section 5**

■ **Ultra-High Input Impedance Amplifiers**

**Electrometers**  
**Smoke Detectors**  
**pH Meters**

■ **Digital Switching Interfaces**

■ **Analog Switching**

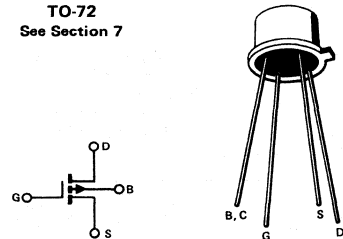
\*ABSOLUTE MAXIMUM RATINGS (25°C)

|   |               |
|---|---------------|
| Drain-Source or Gate-Source Voltage 3N163 . . . . .               | -40 V         |
| Drain-Source or Gate-Source Voltage 3N164 . . . . .               | -30 V         |
| Transient Gate-Source Voltage (Note 1) . . . . .                  | ±150 V        |
| Drain Current . . . . .   | -50 mA        |
| Storage Temperature . . . . .                                     | -65 to +200°C |
| Operating Junction Temperature . . . . .                          | -55 to +150°C |
| Total Device Dissipation<br>(Derate 3.0 mW/°C to 150°C) . . . . . | 375 mW        |
| Lead Temperature 1/16" From Case For 10 Seconds . . . . .         | 265°C         |

**BENEFITS**

- Rugged MOS Gate Minimizes Handling Problems  
±150 V Transient Capability
- Low Gate-Leakage  
Typically 0.02 pA
- High Off-Isolation as a Switch  
 $I_{DSS} < 200 \text{ pA}$

TO-72  
See Section 7



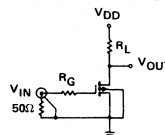
\*ELECTRICAL CHARACTERISTICS (25°C and  $V_{BS} = 0$  unless otherwise noted)

| Characteristic  | 3N163 |       | 3N164 |       | Unit            | Test Conditions   |                            |
|---|-------|-------|-------|-------|-----------------|---|----------------------------|
|   | Min   | Max   | Min   | Max   |                 |   |                            |
| 1 $I_{GSS}$ Gate-Body Leakage Current                   |       | -10   |       |       | pA              | $V_{GS} = -40 \text{ V}, V_{DS} = 0$  | $T_A = 125^\circ \text{C}$ |
| 2   |       | -25   |       |       |                 | $V_{GS} = -30 \text{ V}, V_{DS} = 0$  | $T_A = 125^\circ \text{C}$ |
| 3   |       |       |       | -10   |                 |   |                            |
| 4   |       |       |       | -25   |                 |   |                            |
| 5 $BV_{DSS}$ Drain-Source Breakdown Voltage             | -40   |       | -30   |       | V               | $I_D = -10 \mu\text{A}, V_{GS} = 0$   |                            |
| 6 $BV_{SDS}$ Source-Drain Breakdown Voltage             | -40   |       | -30   |       |                 | $I_S = -10 \mu\text{A}, V_{GD} = V_{BD} = 0$  |                            |
| 7 $V_{GS}$ Gate Source Voltage                          | -3    | -6.5  | -2.5  | -6.5  | V               | $V_{DS} = -15 \text{ V}, I_D = -0.5 \text{ mA}$   |                            |
| 8 $V_{GS(th)}$ Gate-Source Threshold Voltage            | -2    | -5    | -2    | -5    |                 | $V_{DS} = V_{GS}, I_D = -10 \mu\text{A}$  |                            |
| 9 $I_{DSS}$ Drain Cutoff Current                        |       | -200  |       | -400  | pA              | $V_{DS} = -15 \text{ V}, V_{GS} = 0$  |                            |
| 10 $I_{SDS}$ Source Cutoff Current                      |       | -400  |       | -800  |                 | $V_{SD} = -20 \text{ V}, V_{GD} = 0, V_{DB} = 0$  |                            |
| 11 $I_{D(on)}$ ON Drain Current                         | -5    | -30   | -3    | -30   | mA              | $V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}$  |                            |
| 12 $r_{DS(on)}$ Drain-Source ON Resistance              |       | 250   |       | 300   |                 | $V_{GS} = -20 \text{ V}, I_D = -100 \mu\text{A}$  |                            |
| 13 $g_{fs}$ Common-Source Forward Transconductance      | 2,000 | 4,000 | 1,000 | 4,000 | $\mu\text{mho}$ | $V_{DS} = -15 \text{ V}, I_D = -10 \text{ mA}$  | $f = 1 \text{ kHz}$        |
| 14 $g_{os}$ Common-Source Output Conductance            |       | 250   |       | 250   |                 |   |                            |
| 15 $C_{iss}$ Common-Source Input Capacitance            |       | 2.5   |       | 2.5   | pF              | $V_{DS} = -15 \text{ V}, I_D = -10 \text{ mA}$  | $f = 1 \text{ MHz}$        |
| 16 $C_{rss}$ Common-Source Reverse Transfer Capacitance |       | 0.7   |       | 0.7   |                 |   |                            |
| 17 $C_{oss}$ Common-Source Output Capacitance           |       | 3     |       | 3     |                 |   |                            |
| 18 $t_{d(on)}$ Turn-ON Delay Time                       |       | 12    |       | 12    |                 |   |                            |
| 19 $t_r$ Rise Time                                      |       | 24    |       | 24    | ns              | $V_{DD} = -15 \text{ V}$<br>$I_{D(on)} = -10 \text{ mA}$<br>$R_G = R_L = 1.5 \text{ k}\Omega$ |                            |
| 20 $t_{off}$ Turn-OFF Time                              |       | 50    |       | 50    |                 |   |                            |

\*JEDEC registered data

**NOTE:**

1. Transient gate-source voltage JEDEC registered as ±125 V.



|                                   |                                  |
|-----------------------------------|----------------------------------|
| <b>INPUT PULSE</b>                | <b>SAMPLING SCOPE</b>            |
| RISE TIME $\leq 2 \text{ ns}$     | $t_r \leq 0.2 \text{ ns}$        |
| PULSE WIDTH $\geq 200 \text{ ns}$ | $C_{IN} \leq 2 \text{ pF}$       |
|                                   | $R_{IN} \geq 10 \text{ M}\Omega$ |

MRA



# current regulator diodes designed for . . .

Performance Curves  
NKL NKM NKO See Section 5

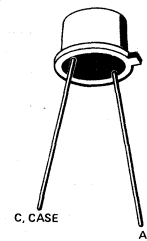
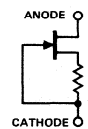
- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

- BENEFITS**
- Simple Two Lead Current Source
  - Current Insensitive to Temperature Changes  
Temperature Coefficient Better Than 1500 ppm/°C On All Devices
  - TO-18 Package for Improved Current Control
  - Simplifies Floating Current Sources  
No Power Supplies Required

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |               |
|---|---------------|
| Peak Operating Voltage                        | 100 V         |
| Forward Current                               | 20 mA         |
| Reverse Current                               | 50 mA         |
| Thermal Resistance $\theta_{JC}$              | 100°C/W       |
| Power Dissipation at $T_C = 25^\circ\text{C}$ | 1.25 W        |
| Operating Junction Temperature                | -55 to +150°C |
| Storage Temperature                           | -55 to +200°C |

TO-18  
See Section 7



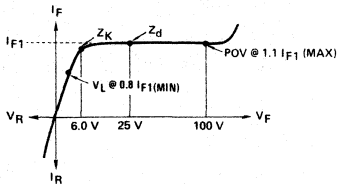
**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Symbol<br>Parameter | $I_{F1}$                        |       |       | $Z_d$                           |      | $Z_k$              |      | $V_L$   |      | POV   | $\theta_1$  |   |   | G<br>E<br>O<br>M |
|---------------------|---------------------------------|-------|-------|---------------------------------|------|--------------------|------|---|------|---|---|---|---|------------------|
|                     | Regulator Current               |       |       | Dynamic Impedance               |      | Knee Impedance     |      | Limiting Voltage                                  |      | Peak Operating Voltage                            | Temperature Coefficient   |   |   |                  |
|                     | $V_F = 25\text{ V}$<br>(Note 1) |       |       | $V_F = 25\text{ V}$<br>(Note 2) |      | $V_F = 6\text{ V}$ |      | $I_F = 0.8\text{ I}_{F1}(\text{Min})$<br>(Note 3) |      | $I_F = 1.1\text{ I}_{F1}(\text{Max})$<br>(Note 4) | $V_F = 25\text{ V}$<br>$-55^\circ\text{C} < T_A < 25^\circ\text{C}$ | $V_F = 25\text{ V}$<br>$0^\circ\text{C} < T_A < 50^\circ\text{C}$ | $V_F = 25\text{ V}$<br>$25^\circ\text{C} < T_A < 125^\circ\text{C}$ |                  |
| Test Conditions     | mA                              |       |       | M $\Omega$                      |      | M $\Omega$         |      | Volts   |      | Min Volts   | Typ ppm/°C  | Typ ppm/°C  | Typ ppm/°C  | N<br>K<br>L      |
| Units               | Nom                             | Min   | Max   | Min                             | Typ  | Min                | Typ  | Max   | Typ  |   |   |   |   |                  |
| CR022               | 0.22                            | 0.198 | 0.242 | 13.0                            | 16.0 | 2.75               | 3.5  | 1.0   | 0.40 | 100   | +1350   | +1050   | +750  |                  |
| CR024               | 0.24                            | 0.216 | 0.264 | 10.0                            | 14.0 | 2.35               | 3.0  | 1.0   | 0.45 | 100   | +1200   | +900  | +600  |                  |
| CR027               | 0.27                            | 0.243 | 0.297 | 9.0                             | 13.0 | 1.95               | 2.8  | 1.0   | 0.50 | 100   | +1000   | +700  | +400  |                  |
| CR030               | 0.30                            | 0.270 | 0.330 | 8.0                             | 12.0 | 1.60               | 2.5  | 1.0   | 0.55 | 100   | +800  | +500  | +200  |                  |
| CR033               | 0.33                            | 0.297 | 0.363 | 6.6                             | 11.0 | 1.35               | 2.2  | 1.0   | 0.60 | 100   | +600  | +300  | -50   |                  |
| CR039               | 0.39                            | 0.351 | 0.429 | 4.10                            | 9.5  | 1.00               | 1.90 | 1.05  | 0.70 | 100   | +300  | +50   | -300  |                  |
| CR043               | 0.43                            | 0.387 | 0.473 | 3.30                            | 8.6  | 0.87               | 1.65 | 1.05  | 0.78 | 100   | +150  | -150  | -450  |                  |
| CR047               | 0.47                            | 0.423 | 0.517 | 2.70                            | 8.0  | 0.75               | 1.50 | 1.10  | 0.85 | 100   | -50   | -300  | -600  |                  |
| CR056               | 0.56                            | 0.504 | 0.616 | 1.90                            | 6.5  | 0.56               | 1.25 | 1.20  | 0.98 | 100   | -300  | -600  | -900  |                  |
| CR062               | 0.62                            | 0.558 | 0.682 | 1.55                            | 6.2  | 0.47               | 1.15 | 1.30  | 1.10 | 100   | -500  | -800  | -1100   |                  |
| CR068               | 0.68                            | 0.612 | 0.748 | 1.35                            | 8.5  | 0.400              | 1.70 | 1.15  | 0.70 | 100   | +850  | +400  | -50   | N<br>K<br>M      |
| CR075               | 0.75                            | 0.675 | 0.825 | 1.15                            | 7.2  | 0.335              | 1.50 | 1.20  | 0.75 | 100   | +650  | +200  | -250  |                  |
| CR082               | 0.82                            | 0.738 | 0.902 | 1.00                            | 6.0  | 0.290              | 1.30 | 1.25  | 0.80 | 100   | +450  | +50   | -450  |                  |
| CR091               | 0.91                            | 0.819 | 1.001 | 0.88                            | 5.2  | 0.240              | 1.10 | 1.29  | 0.85 | 100   | +300  | -150  | -600  |                  |
| CR100               | 1.00                            | 0.900 | 1.100 | 0.80                            | 4.4  | 0.205              | 0.95 | 1.35  | 0.85 | 100   | +150  | -300  | -750  |                  |
| CR110               | 1.10                            | 0.990 | 1.210 | 0.70                            | 3.8  | 0.180              | 0.80 | 1.40  | 1.05 | 100   | +50   | -450  | -900  |                  |
| CR120               | 1.20                            | 1.08  | 1.32  | 0.64                            | 3.3  | 0.155              | 0.71 | 1.45  | 1.15 | 100   | -150  | -600  | -1050   |                  |
| CR130               | 1.30                            | 1.17  | 1.43  | 0.58                            | 3.2  | 0.135              | 0.60 | 1.50  | 1.25 | 100   | -300  | -750  | -1200   |                  |
| CR140               | 1.40                            | 1.26  | 1.54  | 0.54                            | 2.5  | 0.115              | 0.52 | 1.55  | 1.30 | 100   | -400  | -850  | -1300   |                  |
| CR150               | 1.50                            | 1.35  | 1.65  | 0.51                            | 2.2  | 0.105              | 0.46 | 1.60  | 1.35 | 100   | -500  | -950  | -1400   |                  |
| CR160               | 1.60                            | 1.44  | 1.76  | 0.475                           | 1.00 | 0.092              | 0.35 | 1.65  | 0.50 | 100   | +650  | +350  | +50   | N<br>K<br>O      |
| CR180               | 1.80                            | 1.62  | 1.98  | 0.420                           | 0.95 | 0.074              | 0.30 | 1.75  | 0.55 | 100   | +500  | +200  | -100  |                  |
| CR200               | 2.00                            | 1.80  | 2.20  | 0.395                           | 0.88 | 0.061              | 0.25 | 1.85  | 0.60 | 100   | +350  | +50   | -250  |                  |
| CR220               | 2.20                            | 1.98  | 2.42  | 0.370                           | 0.80 | 0.052              | 0.22 | 1.95  | 0.65 | 100   | +200  | -100  | -350  |                  |
| CR240               | 2.40                            | 2.16  | 2.64  | 0.345                           | 0.75 | 0.044              | 0.20 | 2.00  | 0.70 | 100   | +50   | -200  | -450  |                  |
| CR270               | 2.70                            | 2.43  | 2.97  | 0.320                           | 0.68 | 0.035              | 0.18 | 2.15  | 0.75 | 100   | -100  | -300  | -550  |                  |
| CR300               | 3.00                            | 2.70  | 3.30  | 0.300                           | 0.60 | 0.029              | 0.14 | 2.25  | 0.85 | 100   | -250  | -450  | -700  |                  |
| CR330               | 3.30                            | 2.97  | 3.63  | 0.280                           | 0.56 | 0.024              | 0.13 | 2.35  | 0.90 | 100   | -400  | -600  | -800  |                  |
| CR360               | 3.60                            | 3.24  | 3.96  | 0.265                           | 0.52 | 0.020              | 0.11 | 2.50  | 0.95 | 100   | -550  | -750  | -900  |                  |
| CR390               | 3.90                            | 3.51  | 4.29  | 0.255                           | 0.48 | 0.017              | 0.10 | 2.60  | 1.00 | 100   | -700  | -850  | -1000   |                  |
| CR430               | 4.30                            | 3.87  | 4.73  | 0.245                           | 0.45 | 0.014              | 0.09 | 2.75  | 1.10 | 100   | -850  | -950  | -1100   |                  |
| CR470               | 4.70                            | 4.23  | 5.17  | 0.235                           | 0.40 | 0.012              | 0.08 | 2.90  | 1.40 | 100   | -1000   | -1100   | -1200   |                  |

- NOTES:**
1. Pulse test - steady state currents may vary.
  2. Pulse test - steady state impedances may vary.
  3. Min  $V_F$  required to insure  $I_F > 0.8\text{ I}_{F1}(\text{min})$ .
  4. Max  $V_F$  where  $I_F < 1.1\text{ I}_{F1}(\text{max})$  is guaranteed.

NKL, NKM, NKO

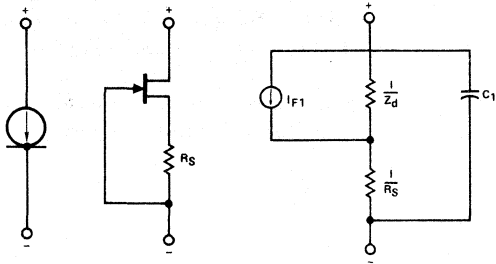
Current-Limiter Diode V-I Characteristic



SYMBOLS AND DEFINITIONS

- A Anode (Drain)
- C Cathode (Source and Gate Shorted)
- $I_F$  Forward Current (Anode Positive)
- $I_{F1}$  Current at a specified Test Voltage,  $V_F$
- POV Peak Operating Voltage
- $\theta_I$  Current Temperature Coefficient
- $\theta_{JC}$  Thermal Resistance Junction to Case
- $\theta_{JA}$  Thermal Resistance Junction to Ambient
- $Z_K$  Knee AC Impedance at specified  $V_F$ .  $Z_K$  should be as high as possible and is specified as a minimum.
- $Z_d$  Dynamic Impedance at specified  $V_F$ .  $Z_d$  is specified as a minimum.

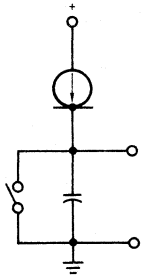
EQUIVALENT CIRCUIT



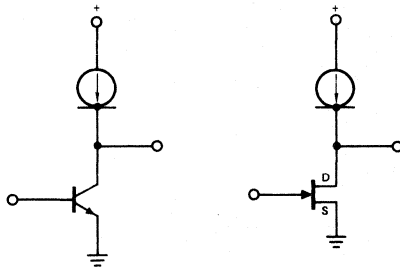
APPLICATIONS

The current-limiter diode is the electrical dual of the Zener diode.

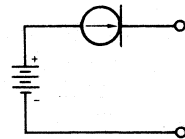
Constant-Current Timing Circuits



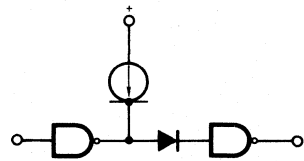
Collector or Drain Hi-Z Load Resistors



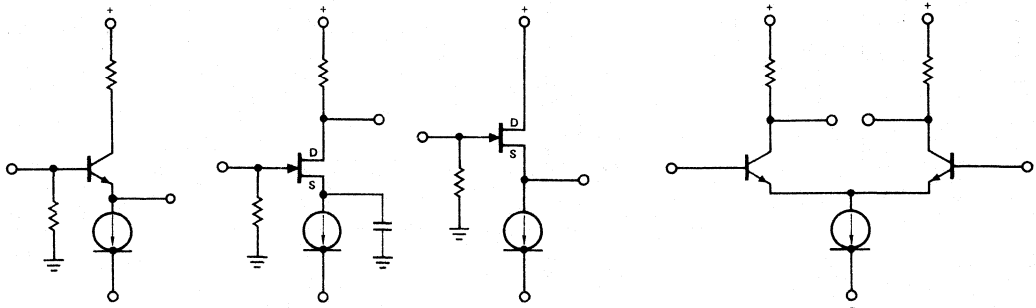
Constant-Current Supply or Current-Limiting Element



Logic Circuit Pull-Up Current Source



Emitter or Source Biasing





# enhancement-type p-channel MOSFET designed for . . .



MFE823

**Performance Curves MRA**  
**See Section 5**

## ■ High-Input Impedance Amplifiers

**Smoke Detectors**  
**Electrometers**  
**pH Meters**

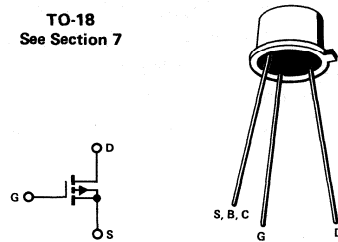
### BENEFITS

- High Input Impedance  
 $I_{GSS} = 30$  Femto Amp Typical
- High Gain  
 $g_{fs} = 1000$   $\mu$ mho Minimum

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |                                     |
|---|-------------------------------------|
| Drain-Source Voltage  | .....25 V                           |
| Gate-Source Voltage   | ..... $\pm 10$ V                    |
| Drain Current   | .....30 mA                          |
| Total Device Dissipation at (Or Below) $T_A = 25^\circ\text{C}$<br>(Derate 3 mW/ $^\circ\text{C}$ to $+150^\circ\text{C}$ ) | .....375 mW                         |
| Operating Junction Temperature  | ..... $-55$ to $+150^\circ\text{C}$ |
| Storage Temperature   | ..... $-65$ to $+200^\circ\text{C}$ |
| Lead Temperature<br>(1/16" from case for 10 seconds)  | ..... $265^\circ\text{C}$           |

**TO-18**  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C)

|   |                                 | Characteristic                                       | Min  | Max  | Unit       | Test Conditions                                 |
|---|---------------------------------|--|------|------|------------|---|
| 1 | S<br>T<br>A<br>T<br>I<br>C      | $I_{GSS}$ Gate-Source Leakage Current                |      | -1.0 | pA         | $V_{GS} = -10$ V, $V_{DS} = 0$                  |
| 2 |                                 | $BV_{DSS}$ Drain-Source Breakdown Voltage            | -25  |      | V          | $I_D = -10$ $\mu$ A, $V_{GS} = 0$               |
| 3 |                                 | $V_{GS}$ Gate-Source Voltage                         | -2.0 | -6.0 | V          | $V_{DS} = -10$ V, $I_D = -10$ $\mu$ A           |
| 4 |                                 | $I_{DSS}$ Drain Cutoff Current                       |      | -20  | nA         | $V_{DS} = -10$ V, $V_{GS} = 0$                  |
| 5 |                                 | $I_{D(on)}$ ON Drain Current                         | -3.0 |      | mA         | $V_{DS} = -10$ V, $V_{GS} = -10$ V              |
| 6 | D<br>Y<br>N<br>A<br>M<br>I<br>C | $g_{fs}$ Common-Source Forward Transconductance      | 1000 |      | $\mu$ mhos | $V_{DS} = -10$ V, $I_D = -2$ mA, $f = 1$ kHz    |
| 7 |                                 | $C_{iss}$ Common-Source Input Capacitance            |      | 6.0  | pF         | $V_{DS} = -10$ V, $V_{GS} = -10$ V, $f = 1$ MHz |
| 8 |                                 | $C_{rss}$ Common-Source Reverse Transfer Capacitance |      | 1.5  |            |   |

MRA

3

Siliconix

# dual pico ampere diodes designed for . . .



- Clipping Circuits
- Diode Switching
- High Impedance Protection Circuits

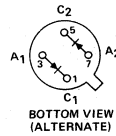
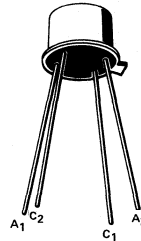
### BENEFITS

- Very High Off-Isolation  
1 pA Max (DPAD1)
- High Isolation Between Diodes  
20 Femto Amp Typical (DPAD1)
- Matched Capacitances
- Compact Packaging

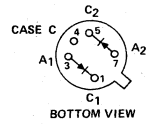
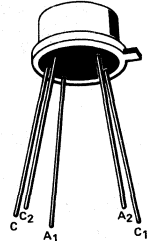
### ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Gate Current, Each Side. . . . . 50 mA  
 Total Device Dissipation @  $T_A = 25^\circ\text{C}$   
 Derate 4.0 mW/°C to 125°C. . . . . 400 mW  
 Storage Temperature Range. . . . .  $-55$  to  $+125^\circ\text{C}$   
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . .  $300^\circ\text{C}$

TO-71  
 (Pins 2 and 6 Removed)  
 See Section 7



TO-78  
 (DPAD1 Only)  
 See Section 7



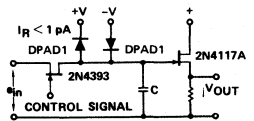
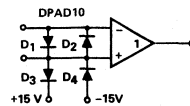
### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| CHARACTERISTIC |   | MIN | TYP | MAX  | UNIT | TEST CONDITION                        |                              |
|----------------|---|-----|-----|------|------|---------------------------------------|------------------------------|
| 1              | S<br>T<br>A<br>T<br>I<br>C<br><br>$I_R$ Reverse Current         |     |     | -1   | pA   | $V_R = -20$ V                         | DPAD1                        |
| 2              |   |     |     | -2   |      |                                       | DPAD2                        |
| 3              |   |     |     | -5   |      |                                       | DPAD5                        |
| 4              |   |     |     | -10  |      |                                       | DPAD10                       |
| 5              |   |     |     | -20  |      |                                       | DPAD20                       |
| 6              |   |     |     | -50  |      |                                       | DPAD50                       |
| 7              |   |     |     | -100 |      |                                       | DPAD100                      |
| 8              | B<br>V<br>R<br><br>$B_{VR}$ Reverse Breakdown Voltage           | -45 |     | -120 | V    | $I_R = -1$ $\mu$ A                    | DPAD1, 2, 5                  |
| 9              |   | -35 |     |      |      |                                       | DPAD10, 20, 50, 100          |
| 10             | $V_F$ Forward Voltage Drop                                      |     | 0.8 | 1.5  |      | $I_F = 1$ mA                          | DPAD1, 2, 5, 10, 20, 50, 100 |
| 11             | D<br>Y<br>N<br><br>$C_R$ Capacitance                            |     |     | 0.8  | pF   | $V_R = -5$ V, $f = 1$ MHz             | DPAD1, 2, 5                  |
| 12             |   |     |     | 2.0  |      |                                       | DPAD10, 20, 50, 100          |
| 13             | M<br>A<br>T<br><br>$ C_{R1} - C_{R2} $ Differential Capacitance |     | 0.1 | 0.2  | pF   | $V_{R1} = V_{R2} = -5$ V, $f = 1$ MHz | DPAD1, 2, 5, 10, 20, 50, 100 |

### APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by DPADS  $D_1$  and  $D_2$  Common mode input voltage limited by DPADS  $D_3$  and  $D_4$  to  $\pm 15$  V.

Typical sample and hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the FET switch gate.



# low-leakage pico-amp diodes designed for . . .



PAD1 PAD2 PAD5 PAD10 PAD20 PAD50 PAD100

- Clipping Circuits
- Diode Switching
- High Impedance Protection Circuits

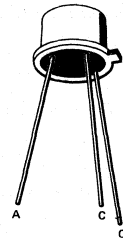
## BENEFITS

- Very High Off-Isolation  
1 pA Max (PAD1)

## ABSOLUTE MAXIMUM RATINGS (25°C)

|  |                 |
|--|-----------------|
| Forward Current                                      | 50 mA           |
| Total Device Dissipation                             | 300 mW          |
| Storage Temperature Range                            | -55°C to +125°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) | 300°C           |

TO-18  
See Section 7

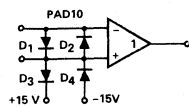


CASE LEAD FOR PAD1, 2, 5 ONLY

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

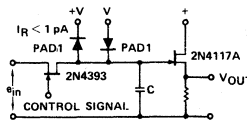
| Characteristic             |                                    | Min | Typ | Max  | Unit | Test Conditions                             |
|----------------------------|------------------------------------|-----|-----|------|------|---|
| S<br>T<br>A<br>T<br>I<br>C | $I_R$ Reverse Current              |     |     | -1   | pA   | PAD1  |
|                            |                                    |     |     | -2   |      | 2   |
|                            |                                    |     |     | -5   |      | 5   |
|                            |                                    |     |     | -10  |      | PAD10                                       |
|                            |                                    |     |     | -20  |      | 20  |
|                            |                                    |     |     | -50  |      | 50  |
|                            |                                    |     |     | -100 |      | PAD100                                      |
| 8                          | $BV_R$ Breakdown Voltage (Reverse) | -45 |     | -120 | V    | PAD1, 2, 5                                  |
|                            |                                    | -35 |     |      |      | PAD10, 20, 50, 100                          |
| 10                         | $V_F$ Forward Voltage Drop         |     | 0.8 | 1.5  |      | $I_F = 5$ mA<br>PAD1, 2, 5, 10, 20, 50, 100 |
| D<br>Y<br>N                | $C_{Ri}$ Capacitance               |     |     | 0.8  | pF   | PAD1, 2, 5                                  |
|                            |                                    |     |     | 2    |      | PAD10, 20, 50, 100                          |

3



## APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by PADS D1 and D2. Common mode input voltage limited by PADS D3 and D4 to  $\pm 15$  V.



Typical sample and hold circuit with clipping. PAD diodes reduce offset voltages fed capacitively from the FET switch gate.

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NC**  
See Section 5

- Analog Switches
- Commutators
- Choppers

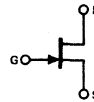
**BENEFITS**

- Low Insertion Loss  
 $R_{DS(on)} < 50 \Omega$  (U202)
- Good Off-Isolation  
 $I_{D(off)} < 1 \text{ nA}$

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |       |               |
|--|-------|---------------|
| Gate-Drain or Gate-Source Voltage                                      | ..... | -30 V         |
| Gate Current   | ..... | 50 mA         |
| Total Device Dissipation at 25°C Case Temperature<br>(Derate 10 mW/°C) | ..... | 1.8 W         |
| Storage Temperature Range  | ..... | -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)                   | ..... | 300°C         |

**TO-18**  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| 1                          | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | Characteristic  | U200 |     | U201 |     | U202 |     | Unit | Test Conditions                                 |           |
|----------------------------|---|---|---|---|---|---|---|---|---|------|-----|------|-----|------|-----|------|---|-----------|
|                            |   |   |   |   |   |   |   |   |   | Min  | Max | Min  | Max | Min  | Max |      | Min   | Max       |
|                            |   |   |   |   |   |   |   |   | I <sub>GSS</sub> Gate Reverse Current                       |      | -1  |      | -1  |      | -1  | nA   | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0    | 150°C     |
| S<br>T<br>A<br>T<br>I<br>C |   |   |   |   |   |   |   |   | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | -30  |     | -30  |     | -30  |     | V    | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0     |           |
|                            |   |   |   |   |   |   |   |   | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage             | -0.5 | -3  | -1.5 | -5  | -3.5 | -10 |      | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 10 nA  |           |
|                            |   |   |   |   |   |   |   |   | I <sub>D(off)</sub> Drain Cutoff Current                    |      | 1   |      | 1   |      | 1   | nA   | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = -12 V | 150°C     |
|                            |   |   |   |   |   |   |   |   | I <sub>DSS</sub> Saturation Drain Current (Note 1)          | 3    | 25  | 15   | 75  | 30   | 150 | mA   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0     |           |
|                            |   |   |   |   |   |   |   |   | r <sub>ds(on)</sub> Drain-Source ON Resistance              |      | 150 |      | 75  |      | 50  | ohm  | V <sub>GS</sub> = 0, I <sub>D</sub> = 0         | f = 1 kHz |
| D<br>Y<br>N                |   |   |   |   |   |   |   |   | C <sub>iss</sub> Common-Source Input Capacitance (Note 1)   |      | 30  |      | 30  |      | 30  | pF   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0     | f = 1 MHz |
|                            |   |   |   |   |   |   |   |   | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |      | 8   |      | 8   |      | 8   |      | V <sub>DS</sub> = 0, V <sub>GS</sub> = -12 V    |           |

**NOTE:**

1. Pulse test required, pulsewidth = 300 μsec, duty cycle ≤ 3%.

**NC**



# monolithic dual n-channel JFETs designed for . . .

## ■ Differential Amplifiers

**Performance Curves NNP**  
See Section 5

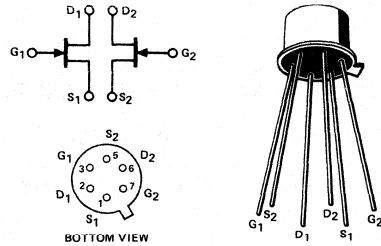
**BENEFITS**

- Good Matching Characteristics

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |                     |
|---|---------------------|
| Gate-Drain or Gate-Source Voltage                               | ..... -50 V         |
| Gate Current  | ..... 50 mA         |
| Total Device Dissipation at 25°C<br>(Derate 1.7 mW/°C to 200°C) | ..... 300 mW        |
| Storage Temperature Range                                       | ..... -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)            | ..... 300°C         |

TO-71  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   |   | Min  | Max  | Unit   | Test Conditions         |       |                         |                         |            |            |
|--|---|------|------|--------|-------------------------|-------|-------------------------|-------------------------|------------|------------|
| S<br>T<br>A<br>T<br>I<br>C   | 1  IGSS  Gate Reverse Current                         |      | -100 | pA     | VGS = -30 V, VDS = 0    |       |                         |                         |            |            |
|  | 2  IGSS  Gate Reverse Current                         |      | -500 | nA     | 150°C                   |       |                         |                         |            |            |
|  | 3 BVGSS Gate-Source Breakdown Voltage                 | -50  |      |        | IG = -1 μA, VDS = 0     |       |                         |                         |            |            |
|  | 4 VGS(off) Gate-Source Cutoff Voltage                 | -0.5 | -4.5 | V      | VDS = 20 V, ID = 1 nA   |       |                         |                         |            |            |
|  | 5 VGS Gate-Source Voltage                             | -0.3 | -4.0 |        |                         |       |                         |                         |            |            |
| D<br>Y<br>N<br>A<br>M<br>I<br>C                                    | 6 IG Gate Operating Current                           |      | -50  | pA     | VDG = 20 V, ID = 200 μA |       |                         |                         |            |            |
|  | 7 IDSS Saturation Drain Current (Note 1)              | 0.5  | 5.0  | mA     | VDS = 20 V, VGS = 0     |       |                         |                         |            |            |
|  | 8 gfs Common-Source Forward Transconductance (Note 1) | 1000 | 3000 |        | VDS = 20 V, VGS = 0     |       |                         |                         |            |            |
| M<br>A<br>T<br>C<br>H<br>I<br>N<br>G                               | 9 gfs Common-Source Forward Transconductance (Note 1) | 600  | 1600 | μmho   | VDG = 20 V, ID = 200 μA |       |                         |                         |            |            |
|  | 10 gos Common-Source Output Conductance               |      | 35   |        | VDS = 20 V, VGS = 0     |       |                         |                         |            |            |
|  | 11 gos Common-Source Output Conductance               |      | 10   |        | VDG = 20 V, ID = 200 μA |       |                         |                         |            |            |
|  | 12 Ciss Common-Source Input Capacitance               |      | 6    | pF     | f = 1 MHz               |       |                         |                         |            |            |
|  | 13 Crss Common-Source Reverse Transfer Capacitance    |      | 2    | pF     | VDS = 20 V, VGS = 0     |       |                         |                         |            |            |
|  | 14 en Equivalent Short Circuit Input Noise Voltage    |      | 80   | nV/√Hz | f = 100 Hz              |       |                         |                         |            |            |
|  | 15  IG1-IG2  Differential Gate Current                | 10   | 10   | 10     | 10                      | 10    | nA                      | VDG = 20 V, ID = 200 μA | 125°C      |            |
| 16 ((IDSS1-IDSS2)/IDSS1) Match (Note 1)                            | 5   | 5    | 5    | 10     | 15                      | %     | VDS = 20 V, VGS = 0     |                         |            |            |
| 17  VGS1-VGS2  Differential Gate-Source Voltage                    | 5   | 10   | 15   | 20     | 25                      | mV    | VDG = 20 V, ID = 200 μA |                         |            |            |
| 18 Δ VGS1-VGS2 /ΔT Gate-Source Voltage Differential Drift (Note 2) | 10  | 25   | 50   | 75     | 100                     | μV/°C |                         |                         | TA = 25°C  | TB = 125°C |
| 19 Δ VGS1-VGS2 /ΔT Gate-Source Voltage Differential Drift (Note 2) | 10  | 25   | 50   | 75     | 100                     | μV/°C |                         |                         | TA = -55°C | TB = 25°C  |
| 20 ((gfs1-gfs2)/gfs1) Transconductance Match (Note 1)              | 3   | 5    | 5    | 10     | 15                      | %     |                         |                         | f = 1 kHz  |            |
| 21  gos1-gos2  Differential Output Conductance                     | 5   | 5    | 5    | 5      | 5                       | μmho  |                         |                         |            |            |

| Characteristic |   | U231 Max | U232 Max | U233 Max | U234 Max | U235 Max | Unit  | Test Conditions         |       |            |            |
|----------------|---|----------|----------|----------|----------|----------|-------|-------------------------|-------|------------|------------|
| 15             | IG1-IG2  Differential Gate Current                              | 10       | 10       | 10       | 10       | 10       | nA    | VDG = 20 V, ID = 200 μA | 125°C |            |            |
| 16             | ((IDSS1-IDSS2)/IDSS1) Match (Note 1)                            | 5        | 5        | 5        | 10       | 15       | %     | VDS = 20 V, VGS = 0     |       |            |            |
| 17             | VGS1-VGS2  Differential Gate-Source Voltage                     | 5        | 10       | 15       | 20       | 25       | mV    | VDG = 20 V, ID = 200 μA |       |            |            |
| 18             | Δ VGS1-VGS2 /ΔT Gate-Source Voltage Differential Drift (Note 2) | 10       | 25       | 50       | 75       | 100      | μV/°C |                         |       | TA = 25°C  | TB = 125°C |
| 19             | Δ VGS1-VGS2 /ΔT Gate-Source Voltage Differential Drift (Note 2) | 10       | 25       | 50       | 75       | 100      | μV/°C |                         |       | TA = -55°C | TB = 25°C  |
| 20             | ((gfs1-gfs2)/gfs1) Transconductance Match (Note 1)              | 3        | 5        | 5        | 10       | 15       | %     |                         |       | f = 1 kHz  |            |
| 21             | gos1-gos2  Differential Output Conductance                      | 5        | 5        | 5        | 5        | 5        | μmho  |                         |       |            |            |

**NOTES:**

1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Measured at end points, TA and TB.

NNP  
NP-D

3

# matched dual n-channel JFET designed for . . .



## Wideband Differential Amplifiers

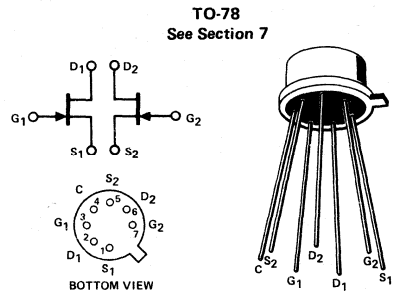
### Performance Curves NZF See Section 5

#### BENEFITS

- High Gain through 100 MHz  
     $g_{fs} = 5000 \mu\text{mho}$  Minimum
- Matching Characteristics Specified

#### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |               |
|---|---------------|
| Gate-Drain or Gate-Source Voltage   | -25 V         |
| Gate Current  | 50 mA         |
| Device Dissipation (Each Side), $T_A = 85^\circ\text{C}$<br>(Derate 3.85 mW/°C) | 250 mW        |
| Total Device Dissipation, $T_A = 85^\circ\text{C}$<br>(Derate 7.7 mW/°C)        | 500 mW        |
| Storage Temperature Range   | -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)                            | 300°C         |



#### ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

|   |  | Characteristic   | Min  | Max  | Unit            | Test Conditions                             |             |        |   |   |
|---|--|--|------|--|-----------------|---|-------------|--------|---|---|
| 1<br>2<br>3<br>4<br>5<br>S<br>T<br>A<br>T<br>I<br>C             | 1  | $I_{GSS}$ Gate Reverse Current   |      | -100   | pA              | $V_{GS} = -15 \text{ V}, V_{DS} = 0$        | 150°C       |        |   |   |
|   |  |  |      | -250   | nA              |   |             |        |   |   |
|   | 3  | $BV_{GSS}$ Gate-Source Breakdown Voltage                                   | -25  |  | V               | $I_G = -1 \mu\text{A}, V_{DS} = 0$          |             |        |   |   |
|   |  |  | 4    | $V_{GS(\text{off})}$ Gate-Source Cutoff Voltage        |                 |   |             | -1     | -5  | $V_{DS} = 10 \text{ V}, I_D = 1 \text{ nA}$ |
|   |  |  |      |  |                 |   |             | 5      | $I_{DSS}$ Saturation Drain Current (Note 1) |   |
| 6<br>7<br>8<br>9<br>10<br>11<br>D<br>Y<br>N<br>A<br>M<br>I<br>C | 6  | $g_{fs}$ Common-Source Forward Transconductance                            | 5000 | 10,000   | $\mu\text{mho}$ | $V_{DS} = 10 \text{ V}, I_D = 5 \text{ mA}$ | f = 1 kHz   |        |   |   |
|   |  |  | 7    | $g_{fs}$ Common-Source Forward Transconductance        |                 |   | 5000        | 10,000 | $V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$ | f = 100 MHz                                 |
|   | 8  | $g_{os}$ Common-Source Output Conductance                                  |      | 150  | $\mu\text{mho}$ | $V_{DS} = 10 \text{ V}, I_D = 5 \text{ mA}$ | f = 1 kHz   |        |   |   |
|   | 9  | $g_{os}$ Common-Source Output Conductance                                  |      | 150  |                 |   | f = 100 MHz |        |   |   |
|   | 10   | $C_{iss}$ Common-Source Input Capacitance                                  |      | 5  | pF              | $V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$ | f = 1 MHz   |        |   |   |
|   | 11   | $C_{rss}$ Common-Source Reverse Transfer Capacitance                       |      | 1.2  |                 |   | f = 10 kHz  |        |   |   |
| 12  | $\bar{e}_n$ Equivalent Short Circuit Input Noise Voltage |  | 30   | $\frac{nV}{\sqrt{Hz}}$                                 |                 | f = 10 kHz                                  |             |        |   |   |
| 13<br>14<br>15<br>16<br>M<br>A<br>T<br>C<br>H<br>I<br>N<br>G    | 13   | $\frac{I_{DSS1}}{I_{DSS2}}$ Saturation Drain Current Ratio (Notes 1 and 2) | 0.85 | 1  |                 | $V_{DS} = 10 \text{ V}, V_{GS} = 0$         |             |        |   |   |
|   |  |  | 14   | $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage |                 |   | 100         | mV     |   |   |
|   | 15   | $\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Note 2)                  | 0.85 | 1  |                 | $V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$ | f = 1 kHz   |        |   |   |
|   |  |  | 16   | $ g_{os1} - g_{os2} $ Differential Output Conductance  |                 |   |             | 20     | $\mu\text{mho}$                             |   |

#### NOTES:

1. Pulse test required, pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 30\%$ .
2. Assumes smaller value in numerator.

NZF

# n-channel JFETs designed for . . .



U290 U291

- Analog Switches
- Commutators
- Choppers

**Performance Curves NVA**  
See Section 5

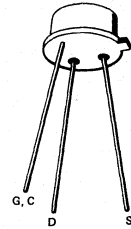
**BENEFITS**

- Ultra-Low Insertion Loss  
 $R_{DS(on)} < 2.5 \Omega$  (U290)
- High Off-Isolation  
 $I_{D(off)} < 1 \text{ nA}$

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . -30 V  
 Gate Current . . . . . 100 mA  
 Drain Current . . . . . 1.5 A  
 Total Device Dissipation at 25°C  
 Free-Air Temperature (Note 1) . . . . . 500 mW  
 Storage Temperature Range . . . . . -65 to +150°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-52  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                  |    | U290                             |  | U291                              |     | Unit | Test Conditions |                      |  |  |           |
|---------------------------------|----|----------------------------------|--|-----------------------------------|-----|------|-----------------|----------------------|--|--|-----------|
|                                 |    | Min                              | Max  | Min                               | Max |      |                 |                      |  |  |           |
| S<br>T<br>A<br>T<br>I<br>C      | 1  | IGSS                             | Gate Reverse Current                       |                                   | -1  | -1   | nA              | VGS = -15 V, VDS = 0 |  |  |           |
|                                 |    |                                  |  |                                   | -1  | -1   | μA              |                      | 150°C  |  |           |
|                                 | 3  | BVGSS                            | Gate-Source Breakdown Voltage              | -30                               |     | -30  |                 | V                    | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0    |  |           |
|                                 | 4  | VGS(off)                         | Gate-Source Cutoff Voltage                 | -4                                | -10 | -1.5 | -4.5            |                      | V  | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3 nA  |           |
|                                 | 5  | ID(off)                          | Drain Cutoff Current                       |                                   | 1   | 1    | 1               | nA                   | V <sub>DS</sub> = 5 V, V <sub>GS</sub> = -10 V |  |           |
|                                 |    |                                  |  |                                   | 1   | 1    | 1               | μA                   |  | 150°C  |           |
|                                 | 7  | VDS(on)                          | Drain-Source ON Voltage                    |                                   | 25  |      | 70              | mV                   | VGS = 0, ID = 10 mA                            |  |           |
|                                 |    | 8                                | IDSS                                       | Saturation Drain Current (Note 2) | 500 |      | 200             |                      | mA   | VDS = 10 V, VGS = 0  |           |
|                                 |    | 9                                | rDS(on)                                    | Static Drain-Source ON Resistance | 1.0 | 2.5  | 2               | 7                    | Ω  | VGS = 0 V, ID = 10 mA  |           |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | 10 | ids(on)                          | Drain-Source ON Resistance                 | 1.0                               | 2.5 | 2    | 7               | Ω                    | VGS = 0, ID = 0                                | f = 1 kHz  |           |
|                                 | 11 | CSGO                             | Source-Gate OFF Capacitance                |                                   | 30  |      | 30              |                      | pF   | VSG = 15 V, ID = 0   | f = 1 MHz |
|                                 | 12 | CDGO                             | Drain-Gate OFF Capacitance                 |                                   | 30  |      | 30              |                      | pF   | V <sub>DG</sub> = 15 V, I <sub>S</sub> = 0   |           |
|                                 | 13 | C <sub>SG</sub> +C <sub>DG</sub> | Source Gate Plus Drain Gate On Capacitance |                                   | 160 |      | 160             |                      | pF   | V <sub>DS</sub> = 0, V <sub>GS</sub> = 0   |           |
| S<br>W<br>I<br>T<br>C<br>H      | 14 | td(on)                           | Turn-ON Delay Time                         |                                   | 15  |      | 15              |                      | ns   | VDD = 1.5 V, ID(on) = 30 mA, RL = 50 Ω,<br>VGS(on) = 0 V,<br>VGS(off) = -12 V (U290)<br>VGS(off) = -7 V (U291) |           |
|                                 | 15 | tr                               | Rise Time                                  |                                   | 20  |      | 20              |                      |  |  |           |
|                                 | 16 | td(off)                          | Turn-OFF Delay Time                        |                                   | 15  |      | 15              |                      |  |  |           |
|                                 | 17 | tf                               | Fall Time                                  |                                   | 20  |      | 20              |                      |  |  |           |

**NOTES:**

1. Derate linearly at the rate of 4.0 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

NVA

3

Siliconix

# p-channel JFETs designed for . . .



- Analog Switches
- Commutators
- Choppers

## Performance Curves PS See Section 5

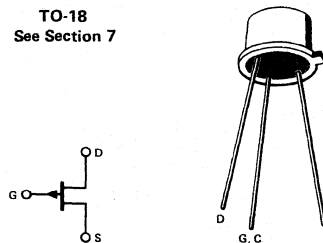
### BENEFITS

- Low Insertion Loss  
 $R_{DS(on)} < 85 \Omega$  (U304)
- High Off-Isolation  
 $I_{D(off)} < 500 \text{ pA}$

### ABSOLUTE MAXIMUM RATINGS (25°C)

|  |               |
|--|---------------|
| Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . .           | 30 V          |
| Gate Current . . . . .   | 50 mA         |
| Total Device Dissipation, Free-Air<br>(Derate 2.8 mW/°C) . . . . . | 350 mW        |
| Storage Temperature Range . . . . .                                | -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 60 seconds) . . . . .     | 300°C         |

TO-18  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | U304                                       |                      | U305                          |      | U306 |     | Unit | Test Conditions         |       |  |
|--|--|----------------------|-------------------------------|------|------|-----|------|-------------------------|-------|--|
|  | Min  | Max                  | Min                           | Max  | Min  | Max |      |                         |       |  |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12<br>13<br>14<br>15<br>16<br>S<br>T<br>A<br>T<br>I<br>C<br><br>D<br>Y<br>N<br><br>S<br>W<br>I<br>T<br>C<br>H | IGSS                                       | Gate Reverse Current |                               | 500  | 500  | 500 | pA   | VGS = 20 V, VDS = 0     |       |  |
|  |  | BVGSS                | Gate-Source Breakdown Voltage |      | 30   | 30  | 30   | μA                      | 150°C |  |
|  |  | VGS(off)             | Gate-Source Cutoff Voltage    |      | 5    | 10  | 3    | 6                       | 1     | 4  |
| VDS(on)  | Drain-Source ON Voltage                    |                      | -1.3                          | -0.8 | -0.6 |     |      | VDS = -15 V, ID = -1 μA |       |  |
| IDSS   | Saturation Drain Current (Note 2)          |                      | -30                           | -90  | -15  | -60 | -5   | -25                     | mA    | VDS = -15 V, VGS = 0   |
| ID(off)  | Drain Cutoff Current                       |                      | -500                          | -500 | -500 |     |      |                         | pA    | VDS = -15 V, VGS = 12 V (U304),<br>VGS = 7 V (U305),<br>VGS = 5 V (U306) |
| ID(off)  | Drain Cutoff Current                       |                      | -1.0                          | -1.0 | -1.0 |     |      |                         | μA    | 150°C  |
| rDS(on)  | Static Drain-Source ON Resistance          |                      | 85                            | 110  | 175  |     |      |                         | Ω     | VGS = 0 V, ID = -1 mA  |
| rds(on)  | Drain-Source ON Resistance                 |                      | 85                            | 110  | 175  |     |      |                         | Ω     | VGS = 0 V, ID = 0  |
| Ciss   | Common-Source Input Capacitance            |                      | 27                            | 27   | 27   |     |      |                         | pF    | VDS = -15 V, VGS = 0   |
| Crss   | Common-Source Reverse Transfer Capacitance |                      | 7                             | 7    | 7    |     |      |                         | pF    | VDS = 0, VGS = 12 V (U304),<br>VGS = 7 V (U305),<br>VGS = 5 V (U306)     |
| td(on)   | Turn-ON Delay Time                         |                      | 20                            | 25   | 25   |     |      |                         | ns    | U304 U305 U306   |
| tr   | Rise Time                                  |                      | 15                            | 25   | 35   |     |      |                         | ns    | VDD -10 V -6 V -6 V  |
| td(off)  | Turn-OFF Delay Time                        |                      | 10                            | 15   | 20   |     |      |                         | ns    | VGS(off) 12 V 7 V 5 V  |
| tf   | Fall Time                                  |                      | 25                            | 40   | 60   |     |      |                         | ns    | RL 580 Ω 743 Ω 1800 Ω  |
|  |  |                      |                               |      |      |     |      |                         | ns    | VGS(on) 0 0 0  |
|  |  |                      |                               |      |      |     |      |                         | ns    | ID(on) -15 mA -7 mA -3 mA  |

- NOTES:
- Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
  - Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

PS



# n-channel JFETs designed for . . .



U308 U309 U310

**Performance Curves NZA**  
See Section 5

- VHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

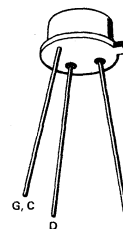
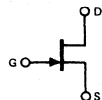
**BENEFITS**

- Industry Standard
- High Power Gain  
16 dB at 105 MHz, Common-Gate  
11 dB at 450 MHz, Common-Gate
- Low Noise  
2.7 dB Noise Figure at 450 MHz
- Wide Dynamic Range  
Greater than 100 dB
- 75 Ω Input Match Common Gate

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |       |               |
|--|-------|---------------|
| Gate-Drain or Gate-Source Voltage                    | ..... | -25 V         |
| Gate Current   | ..... | 20 mA         |
| Total Power Dissipation at T <sub>A</sub> = 25°C     | ..... | 500 mW        |
| Power Derating to 150°C                              | ..... | 4.0 mW/°C     |
| Storage Temperature Range                            | ..... | -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) | ..... | 300°C         |

TO-52  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | U308                 |   |      | U309 |      |      | U310 |      |      | Unit | Test Conditions |        |   |  |
|--|----------------------|---|------|------|------|------|------|------|------|------|-----------------|--------|---|--|
|  | Min                  | Typ   | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |                 |        |   |  |
| 1<br>2<br>S<br>T<br>A<br>T<br>I<br>C                                       | I <sub>GSS</sub>     | Gate Reverse Current                          |      |      | -150 |      |      | -150 |      |      | -150            | pA     | V <sub>GS</sub> = -15 V,<br>V <sub>GS</sub> = 0<br>T <sub>A</sub> = 125°C   |  |
|  |                      |   |      |      | -150 |      |      | -150 |      |      | -150            | nA     |   |  |
| 3  | BV <sub>GSS</sub>    | Gate-Source Breakdown Voltage                 | -25  |      | -25  |      |      | -25  |      |      |                 | V      | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0   |  |
| 4  | V <sub>GS(off)</sub> | Gate-Source Cutoff Voltage                    | -1.0 |      | -6.0 | -1.0 |      | -4.0 | -2.5 |      | -6.0            |        | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA   |  |
| 5  | I <sub>DSS</sub>     | Saturation Drain Current (Note 1)             | 12   |      | 60   | 12   |      | 30   | 24   |      | 60              | mA     | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0   |  |
| 6  | V <sub>GS(f)</sub>   | Gate-Source Forward Voltage                   |      |      | 1.0  |      |      | 1.0  |      |      | 1.0             | V      | I <sub>G</sub> = 10 mA, V <sub>DS</sub> = 0   |  |
| 7<br>8<br>9<br>10<br>D<br>Y<br>N<br>A<br>M<br>I<br>C                       | g <sub>fg</sub>      | Common-Gate Forward Transconductance (Note 1) | 10   |      | 20   | 10   |      | 20   | 10   |      | 18              | mmho   | V <sub>DS</sub> = 10 V,<br>I <sub>D</sub> = 10 mA<br>f = 1 kHz  |  |
|  | g <sub>og</sub>      | Common-Gate Output Conductance                |      |      | 200  |      |      | 200  |      |      | 200             | μmho   |   |  |
|  | C <sub>gd</sub>      | Drain-Gate Capacitance                        |      |      | 2.5  |      |      | 2.5  |      |      | 2.5             | pF     | V <sub>GS</sub> = -10 V,<br>V <sub>DS</sub> = 10 V<br>f = 1 MHz   |  |
|  | C <sub>gs</sub>      | Gate-Source Capacitance                       |      |      | 5.0  |      |      | 5.0  |      |      | 5.0             |        |   |  |
| 11   | ē <sub>n</sub>       | Equivalent Short Circuit Input Noise Voltage  |      |      | 10   |      |      | 10   |      |      | 10              | nV/√Hz | V <sub>DS</sub> = 10 V,<br>I <sub>D</sub> = 10 mA<br>f = 100 Hz   |  |
| 12<br>13<br>14<br>15<br>16<br>17<br>18<br>19<br>H<br>I<br>F<br>R<br>E<br>Q | g <sub>fg</sub>      | Common-Gate Forward Transconductance          |      |      | 15   |      |      | 15   |      |      | 15              |        | V <sub>DS</sub> = 10 V,<br>I <sub>D</sub> = 10 mA<br>f = 105 MHz<br>f = 450 MHz<br>f = 105 MHz<br>f = 450 MHz<br>f = 105 MHz<br>f = 450 MHz<br>f = 105 MHz<br>f = 450 MHz |  |
|  |                      |   |      |      | 14   |      |      | 14   |      |      | 14              |        |   |  |
|  | g <sub>og</sub>      | Common-Gate Output Conductance                |      |      | 0.18 |      |      | 0.18 |      |      | 0.18            |        |   |  |
|  |                      |   |      |      | 0.32 |      |      | 0.32 |      |      | 0.32            |        |   |  |
|  | G <sub>pg</sub>      | Common-Gate Power Gain (Note 2)               |      |      | 14   | 16   |      | 14   | 16   |      | 14              | 16     |   |  |
|  |                      |   |      |      | 10   | 11   |      | 10   | 11   |      | 10              | 11     |   |  |
| NF   | Noise Figure         |   |      | 1.5  | 2.0  |      | 1.5  | 2.0  |      | 1.5  | 2.0             | dB     |   |  |
|  |                      |   |      | 2.7  | 3.5  |      | 2.7  | 3.5  |      | 2.7  | 3.5             |        |   |  |

**NOTES:**

1. Pulse test duration = 2 ms.
2. Gain (G<sub>pg</sub>) measured at optimum input noise match.

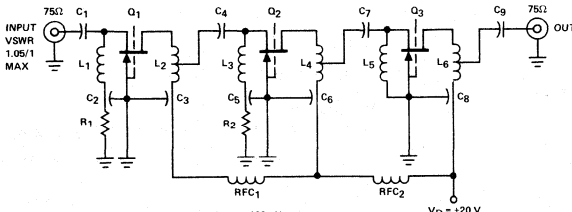
NZA

3

Siliconix

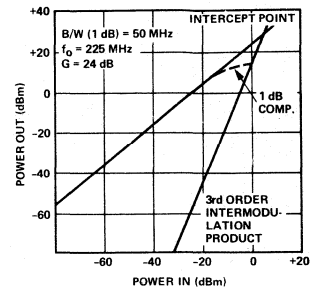
APPLICATIONS

200-250 MHz Wideband Amplifier (1 dB Ripple)  
3-Stage Amplifier Circuit

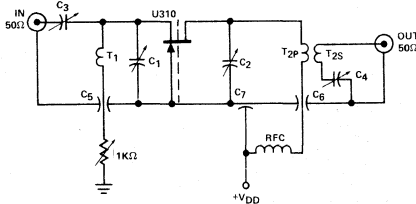


- C<sub>1</sub>, C<sub>4</sub>, C<sub>7</sub>, C<sub>8</sub> = 68 pF
- C<sub>2</sub>, C<sub>5</sub> = 500 pF
- C<sub>3</sub>, C<sub>6</sub>, C<sub>8</sub> = 1,000 pF
- Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub> = Siliconix U310
- L<sub>1</sub>, L<sub>3</sub>, L<sub>5</sub> = 120 nHy
- L<sub>2</sub>, L<sub>4</sub>, L<sub>6</sub> = 222 nHy
- RFC<sub>1</sub>, RFC<sub>2</sub> = 2.2 μHy
- R<sub>1</sub>, R<sub>2</sub> = 51 Ω

2 Tone Intercept & Compression  
Point Measurement

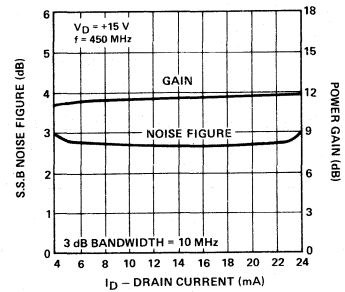


450 MHz Common Gate Amplifier

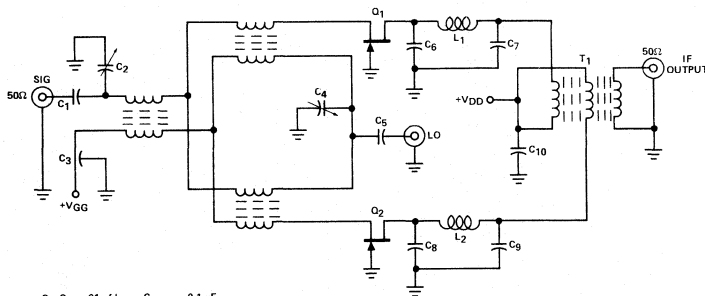


- C<sub>1</sub>, C<sub>2</sub> - 0.8-10 pF JFD model MVM 010W
- C<sub>3</sub>, C<sub>4</sub> - 8-35 pF Erie series 539-002D
- C<sub>5</sub>, C<sub>6</sub> - 5000 pF Erie (2443-000)
- C<sub>7</sub> - 1000 pF ALLEN-BRADLEY type FASC
- RFC - .33 μH MILLER type (9230-30)
- T<sub>1</sub> - one turn, #16 copper wire, 1/4" I.D. (Air Core)
- T<sub>2P</sub> - one turn, #16 copper wire, 1/4" I.D. (Air Core)
- T<sub>2S</sub> - one turn, #16 copper wire, 1/4" I.D. (Air Core)

Noise Figure vs. Power Gain

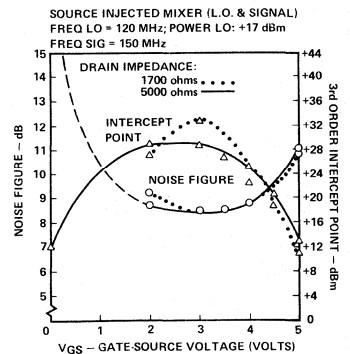


Prototype Active Balanced Mixer\*



- C<sub>1</sub>, C<sub>5</sub> - .01 μfd
- C<sub>2</sub>, C<sub>4</sub> - 1-10 pF
- C<sub>3</sub> - 1000 pF
- C<sub>6</sub>, C<sub>8</sub> - 30 pF
- C<sub>7</sub>, C<sub>9</sub> - 68 pF
- C<sub>10</sub> - 0.1 μF
- L<sub>1</sub>, L<sub>2</sub> - 1.3 μHy
- Q<sub>1</sub>, Q<sub>2</sub> - U310
- T<sub>1</sub> - RELCOM BT-9

Comparison of Mixer IM  
Characteristics



\*Reference Siliconix Application Note AN71-2.

# n-channel JFET designed for . . .

- VHF Amplifiers
- Oscillators
- Mixers

**Performance Curves NZA**  
See Section 5

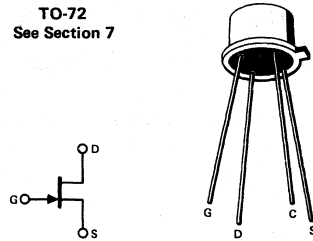
**BENEFITS**

- High Power Gain  
16 dB Typ @ 105 MHz, Common-Gate  
11 dB Typ @ 450 MHz, Common-Gate
- Low Noise Figure  
1.5 dB Typ @ 105 MHz  
2.7 dB Typ @ 450 MHz
- Wide Dynamic Range—Greater than 100 dB

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -25 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW  
 Storage Temperature Range . . . . . -65 to +200°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-72  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

|                            |                                    | Characteristic                                    | Min    | Max    | Unit               | Test Conditions        |           |
|----------------------------|------------------------------------|---|--------|--------|--------------------|------------------------|-----------|
| S<br>T<br>A<br>T<br>I<br>C | 1                                  | IGSS Gate Reverse Current                         |        | -150   | pA                 | VGS = -15 V, VDS = 0   | 150°C     |
|                            | 2                                  |   |        | -150   | nA                 |                        |           |
|                            | 3                                  | BVGSS Gate-Source Breakdown Voltage               | -25    |        | V                  | IG = -1 μA, VDS = 0    |           |
|                            | 4                                  | VGS(off) Gate-Source Cutoff Voltage               | -1     | -6     |                    | VDS = 10 V, ID = 1 nA  |           |
|                            | 5                                  | IDSS Saturation Drain Current (Note 1)            | 20     | 60     | mA                 | VDS = 10 V, VGS = 0    |           |
| 6                          | VGS(f) Gate-Source Forward Voltage |   | 1      | V      | IG = 1 mA, VDS = 0 |                        |           |
| D<br>Y<br>N                | 7                                  | 9fg Common-Gate Forward Transconductance (Note 1) | 10,000 | 20,000 | μmho               | VDS = 10 V, ID = 10 mA | f = 1 kHz |
|                            | 8                                  | 9og Common-Gate Output Conductance                |        | 200    |                    |                        |           |
|                            | 9                                  | Cgd Gate-Drain Capacitance                        |        | 2.5    | pF                 | VDG = 10 V, ID = 5 mA  | f = 1 MHz |
|                            | 10                                 | Cgs Gate-Source Capacitance                       |        | 5.0    |                    |                        |           |

**NOTE:**  
1. Pulse test duration = 2 ms.

NZA

# n-channel JFET designed for . . .



- VHF/UHF Common-Gate Amplifiers
- Mixers

**Performance Curves NZF**  
See Section 5

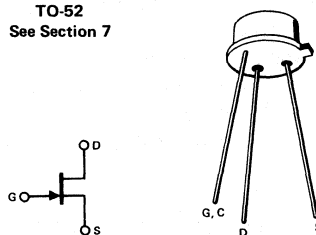
**BENEFITS**

- High Power Gain  
10 dB Typical at 450 MHz,  
Common Gate
- Low Noise  
NF = 3.5 dB Typical at 450 MHz

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |                     |
|--|---------------------|
| Gate-Drain or Gate-Source Voltage        | ..... -25 V         |
| Gate Current                             | ..... 10 mA         |
| Total Power Dissipation at or below 25°C |                     |
| Free-Air Temperature                     | ..... 500 mW        |
| Power Derating                           | ..... 4.0 mW/°C     |
| Operating Temperature Range              | ..... -65 to +150°C |
| Storage Temperature Range                | ..... -65 to +150°C |
| Lead Temperature                         |                     |
| (1/16" from case for 10 seconds)         | ..... 300°C         |

TO-52  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

|  |          | Characteristic                                | Min                            | Max    | Unit | Test Conditions        |           |
|--|----------|---|--------------------------------|--------|------|------------------------|-----------|
| 1<br>2<br>3<br>4<br>5<br>T<br>A<br>T<br>I<br>C | 1gSS     | Gate Reverse Current                          |                                | -0.1   | nA   | VGS = -15 V, VDS = 0   | 150°C     |
|  |          |   |                                | -0.1   | µA   |                        |           |
|  | BVGSS    | Gate-Source Breakdown Voltage                 | -25                            |        | V    | IG = -1 µA, VDS = 0    |           |
|  | VGS(off) | Gate-Source Cutoff Voltage                    | -1                             | -6     | V    | VDS = 10 V, ID = 1 nA  |           |
| 5  | IDSS     | Saturation Drain Current (Note 1)             | 10                             | 30     | mA   | VDS = 10 V, VGS = 0    |           |
| 6<br>7<br>8<br>9<br>D<br>Y<br>N                | 9fg      | Common-Gate Forward Transconductance (Note 1) | 6000                           | 10,000 | µmho | VDS = 10 V, ID = 10 mA | f = 1 kHz |
|  |          | 9og   | Common-Gate Output Conductance |        | 200  |                        |           |
|  | Cgd      | Gate-Drain Capacitance                        |                                | 1.2    | pF   | VDG = 10 V, ID = 10 mA | f = 1 MHz |
|  | Cgs      | Gate-Source Capacitance                       |                                | 3.8    | pF   |                        |           |

**NOTE:**

1. Pulse test duration = 2 ms.

NZF

# n-channel JFETs designed for . . .

- VHF Buffer Amplifiers
- IF Amplifiers

**Performance Curves NIP**  
See Section 5

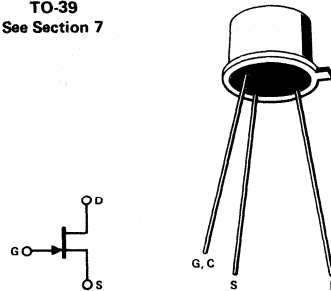
**BENEFITS**

- High Gain  
 $g_{fs} = 120,000 \mu\text{mho Typical}$
- Wide Dynamic Range
- Low Intermodulation Distortion

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -25 V  
 Gate Current . . . . . 100 mA  
 Total Device Dissipation (25°C Case Temperature) . . . . . 3 W  
 Power Derating (to 150°C) . . . . . 24 mW/°C  
 Storage Temperature Range . . . . . -55 to +150°C  
 Operating Temperature Range . . . . . -55 to +150°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-39  
See Section 7



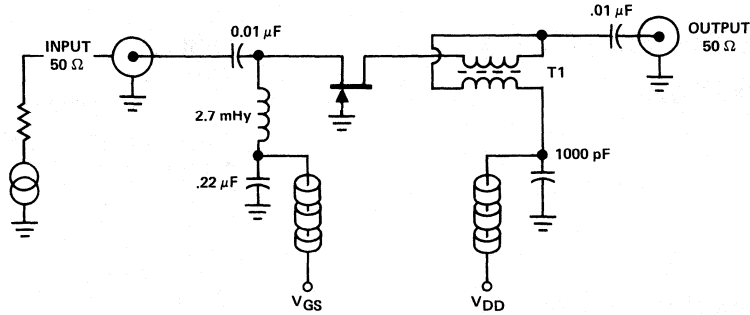
**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                  | U320 |               |   | U321 |     |     | U322 |     |     | Unit | Test Conditions |   |
|---------------------------------|------|---------------|---|------|-----|-----|------|-----|-----|------|-----------------|---|
|                                 | Min  | Typ           | Max   | Min  | Typ | Max | Min  | Typ | Max |      |                 |   |
| S<br>T<br>A<br>T<br>I<br>C      | 1    | $I_{GSS}$     | Gate Reverse Current (Note 1)                   |      |     | -3  |      | -3  |     | -3   | nA              | $V_{GS} = -15 \text{ V}, V_{DS} = 0 \text{ V}$<br>$T = 100^\circ\text{C}$   |
|                                 | 2    | $V_{GS(off)}$ | Gate-Source Cutoff Voltage                      |      | -2  | -10 | -1   | -4  | -3  | -10  | $\mu\text{A}$   |   |
|                                 | 3    | $BV_{GSS}$    | Gate-Source Breakdown Voltage                   |      | -25 |     | -25  |     | -25 |      | V               | $V_{DS} = 5 \text{ V}, I_D = 1 \text{ mA}$<br>$I_G = -1 \mu\text{A}, V_{GS} = 0 \text{ V}$  |
|                                 | 4    | $I_{DSS}$     | Saturation Drain Current (Note 2)               |      | 100 | 500 | 80   | 250 | 200 | 700  | mA              |   |
|                                 | 5    | $V_{GS(f)}$   | Gate-Source Forward Voltage                     |      |     | 1   |      | 1   |     | 1    | V               | $I_G = 1 \text{ mA}, V_{DS} = 0 \text{ V}$  |
|                                 | 6    | $r_{DS(on)}$  | Drain-Source ON Resistance                      |      |     | 10  |      | 11  |     | 8    | $\Omega$        | $V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}$   |
|                                 | 7    | $g_{fs}$      | Common-Source Forward Transconductance (Note 2) |      | 75  | 120 | 200  | 75  | 130 | 200  | mmhos           | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$<br>$f = 1 \text{ kHz}$  |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | 8    | $C_{iss}$     | Common-Source Input Capacitance                 |      |     | 30  |      | 30  |     | 30   | $\mu\text{F}$   | $V_{GS} = -10 \text{ V}, V_{DS} = 0 \text{ V}$<br>$V_{GS} = -10 \text{ V}, I_D = 0$<br>$V_{GD} = -10 \text{ V}, I_S = 0$<br>$f = 1 \text{ MHz}$ |
|                                 | 9    | $C_{rss}$     | Common-Source Reverse Transfer Capacitance      |      |     | 15  |      | 15  |     | 15   |                 |   |
|                                 | 10   | $C_{gs}$      | Gate-Source Capacitance                         |      |     | 12  |      | 12  |     | 12   |                 |   |
|                                 | 11   | $C_{gd}$      | Gate-Drain Capacitance                          |      |     | 12  |      | 12  |     | 12   |                 |   |
|                                 | 12   | $e_n$         | Equivalent Short Circuit Input Noise Voltage    |      |     | 2   |      | 2   |     | 2    |                 |   |
| H<br>I<br>G<br>H                | 13   | $g_{fg}$      | Common Gate Forward Transconductance            |      |     | 55  |      | 55  |     | 55   | mmho            | $V_{DG} = 20 \text{ V}, I_D = 25 \text{ mA}$<br>$f = 50 \text{ MHz}$  |
|                                 | 14   | $g_{ig}$      | Common-Gate Input Conductance                   |      |     | 56  |      | 56  |     | 56   |                 |   |
|                                 | 15   | $g_{og}$      | Common-Gate Output Conductance                  |      |     | 0.5 |      | 0.5 |     | 0.5  |                 |   |
|                                 | 16   | $G_{PS}$      | Power Gain (Note 3)                             |      |     | 9   |      | 9   |     | 9    |                 |   |
| F<br>R<br>E<br>Q                | 17   | $F_t$         | Gain-Bandwidth (Note 4)                         |      |     | 400 |      | 400 |     | 400  | MHz             | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$   |
|                                 | 18   | NF            | Noise Figure (Note 3)                           |      |     | 2.5 |      | 2.5 |     | 2.5  | dB              | $V_{DG} = 20 \text{ V}, I_D = 25 \text{ mA}$<br>$f = 30 \text{ MHz}$  |

- NOTES:**
- Approximately doubles for every 10°C increase in  $T_A$ .
  - Pulse test duration = 2 ms.
  - Noise figure (SSB) and power gain measured in circuit shown in Figure 1.
  - Computed as  $g_{fs}/C_{rss}$ .

NIP

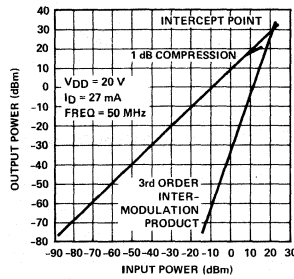
3



T1—6 TURNS #22 AWG TWISTED PAIR WIRE ON 0.375 INCH DIAMETER INDIANA GENERAL F625-9Q2 TOROID CORE.

50 MHz Power Gain and Noise Figure Test Circuit for U320, U321 and U322

Figure 1



Gain - Intermodulation Characteristics Figure 2

# monolithic dual n-channel JFETs designed for . . .



## Performance Curves NNR See Section 5

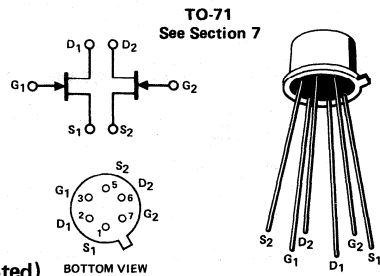
- Low Noise FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

### BENEFITS

- Minimum System Error and Calibration  
5 mV Offset Maximum (U401)  
95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature  
10  $\mu\text{V}/^\circ\text{C}$  Maximum (U401, 02)
- Operates from Low Power Supply Voltages  
 $V_{GS(\text{off})} < 2.5 \text{ V}$
- Simplifies Amplifier Design  
Output Conductance  $< 2 \mu\text{mho}$
- Low Noise  
 $\bar{e}_n = 6 \text{ nV}/\sqrt{\text{Hz}}$  at 10 Hz Typical

### ABSOLUTE MAXIMUM RATINGS (25°C)

|  |              |
|--|--------------|
| Gate-Drain or Gate-Source Voltage . . . . .  | 50 V         |
| Forward Gate Current . . . . .   | 10 mA        |
| Device Dissipation (each side)<br>@ $T_A = 85^\circ\text{C}$ derate 2.6 mW/ $^\circ\text{C}$ . . . . . | 300 mW       |
| Total Device Dissipation<br>@ $T_A = 85^\circ\text{C}$ (derate 5 mW/ $^\circ\text{C}$ ) . . . . .      | 500 mW       |
| Storage Temperature Range . . . . .  | -65 to 200°C |



### ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

| Characteristic  | U401 |      | U402 |      | U403 |      | U404 |      | U405 |      | U406 |      | Unit                         | Test Conditions  |
|---|------|------|------|------|------|------|------|------|------|------|------|------|------------------------------|--|
|   | Min  | Max  | Min  | Max  | Min  | Max  | Min  | Max  | Min  | Max  | Min  | Max  |                              |  |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage   | -50  |      | -50  |      | -50  |      | -50  |      | -50  |      | -50  |      | V                            | $V_{DS} = 0, I_G = -1 \mu\text{A}$   |
| 2  I <sub>GSS</sub>   Gate Reverse Current (Note 1)   |      | -25  |      | -25  |      | -25  |      | -25  |      | -25  |      | -25  | pA                           | $V_{DS} = 0, V_{GS} = -30 \text{ V}$   |
| 3 V <sub>GS(off)</sub> Gate-Source Cutoff Voltage   | -5   | -2.5 | -5   | -2.5 | -5   | -2.5 | -5   | -2.5 | -5   | -2.5 | -5   | -2.5 | V                            | $V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$  |
| 4 V <sub>GS(on)</sub> Gate-Source Voltage (on)  |      | -2.3 |      | -2.3 |      | -2.3 |      | -2.3 |      | -2.3 |      | -2.3 | V                            | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$   |
| 5 I <sub>DSS</sub> Saturation Drain Current (Note 2)  | 0.5  | 10.0 | 0.5  | 10.0 | 0.5  | 10.0 | 0.5  | 10.0 | 0.5  | 10.0 | 0.5  | 10.0 | mA                           | $V_{DS} = 10 \text{ V}, V_{GS} = 0$  |
| 6  I <sub>G</sub>   Gate Current (Note 1)   |      | -15  |      | -15  |      | -15  |      | -15  |      | -15  |      | -15  | pA                           | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}, T_A = 125^\circ\text{C}$  |
| 8 BV <sub>G1 - G2</sub> Gate-Gate Breakdown Voltage   | ±50  |      | ±50  |      | ±50  |      | ±50  |      | ±50  |      | ±50  |      | V                            | $V_{DS} = 0, V_{GS} = 0, I_G = \pm 1 \mu\text{A}$  |
| 9 g <sub>fs</sub> Common-Source Forward Transconductance (Note 2)                               | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | $\mu\text{mho}$              | $V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ kHz}$   |
| 10 g <sub>os</sub> Common-Source Output Conductance   |      | 20   |      | 20   |      | 20   |      | 20   |      | 20   |      | 20   | $\mu\text{mho}$              | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}, f = 1 \text{ kHz}$  |
| 11 g <sub>fs</sub> Common-Source Forward Transconductance                                       | 1000 | 1600 | 1000 | 1600 | 1000 | 1600 | 1000 | 1600 | 1000 | 1600 | 1000 | 1600 | $\mu\text{mho}$              | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}, f = 1 \text{ MHz}$  |
| 12 g <sub>os</sub> Common-Source Output Conductance   |      | 2.0  |      | 2.0  |      | 2.0  |      | 2.0  |      | 2.0  |      | 2.0  | $\mu\text{mho}$              | $V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}, f = 1 \text{ MHz}$  |
| 13 C <sub>iss</sub> Common-Source Input Capacitance   |      | 8.0  |      | 8.0  |      | 8.0  |      | 8.0  |      | 8.0  |      | 8.0  | pF                           | $V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 10 \text{ Hz}$   |
| 14 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance                                  |      | 3.0  |      | 3.0  |      | 3.0  |      | 3.0  |      | 3.0  |      | 3.0  | pF                           | $V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 10 \text{ Hz}$   |
| 15 e <sub>n</sub> Equivalent Short-Circuit Input Noise Voltage                                  |      | 20   |      | 20   |      | 20   |      | 20   |      | 20   |      | 20   | nV/√Hz                       | $V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 10 \text{ Hz}$   |
| 16 CMRR Common-Mode Rejection Ratio (Note 3)  | 95   |      | 95   |      | 95   |      | 95   |      | 90   |      |      |      | dB                           | $V_{DG} = 10 \text{ to } 20 \text{ V}, I_D = 200 \mu\text{A}$  |
| 17  V <sub>GS1</sub> - V <sub>GS2</sub>   Differential Gate-Source Voltage                      |      | 5    |      | 10   |      | 10   |      | 15   |      | 20   |      | 40   | mV                           | $V_{DG} = 10 \text{ V}, I_D = 200 \mu\text{A}$   |
| 18 $\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 4) |      | 10   |      | 10   |      | 25   |      | 25   |      | 40   |      | 80   | $\mu\text{V}/^\circ\text{C}$ | $V_{DG} = 10 \text{ V}, I_D = 200 \mu\text{A}, T_A = -55^\circ\text{C}, T_B = +25^\circ\text{C}, T_C = +125^\circ\text{C}$ |

#### NOTES:

1. Approximately doubles for every 10°C increase in T<sub>A</sub>. 2. Pulse test duration = 300  $\mu\text{s}$ ; duty cycle  $\leq 3\%$ . 3. CMRR = 20 log<sub>10</sub>  $\left[ \frac{\Delta V_{DD}}{\Delta|V_{GS1} - V_{GS2}|} \right], \Delta V_{DD} = 10 \text{ V}$ .

4. Measured at end points, T<sub>A</sub>, T<sub>B</sub> and T<sub>C</sub>.

NNR  
NRL-D

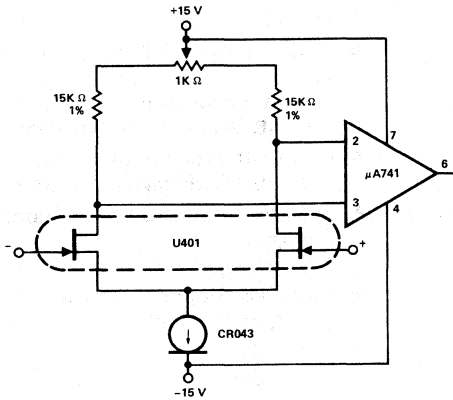
3

Siliconix

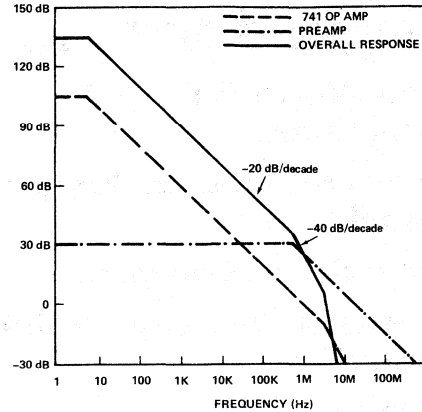
APPLICATIONS



General Purpose FET Input Op Amp



Open Loop Gain and Frequency Response of Op Amp



Typical Specs for General Purpose FET Input Op Amp\*

- Common Mode Range . . . . . +6.7 to -8.8 Volts
- Worst Case Drift Referred to the Input . . .  $\approx 12 \mu\text{V}/^\circ\text{C}$
- Broad Band Noise Referred to the Input (0.1 to 1 kHz) . . . . .  $\approx 188 \text{ nV/Rms}$
- Gain and Bandwidth . . . . . (see graph)

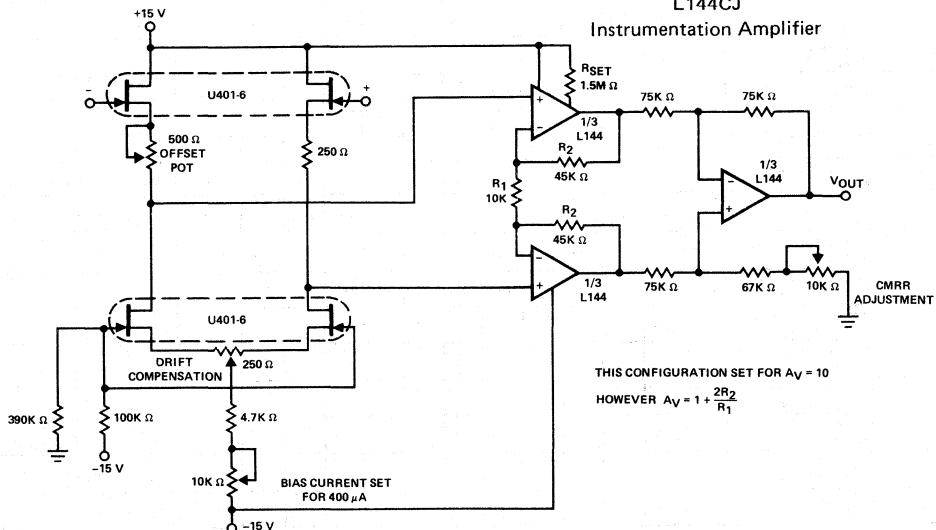
\*These specs depend upon the specifications of the Operational amplifier IC used.

For further design information, write for:

DESIGNING FET-INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included. (16 pages).

FET Input Instrumentation Amplifier



THIS CONFIGURATION SET FOR  $A_V = 10$   
HOWEVER  $A_V = 1 + \frac{2R_2}{R_1}$



# monolithic dual n-channel JFETs designed for . . .



U410 U411 U412

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

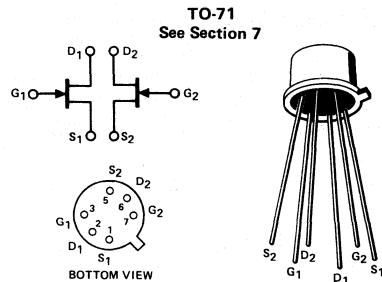
## Performance Curves NQP See Section 5

### BENEFITS

- Low Cost
- Minimum System Error and Calibration  
10 mV Offset Maximum (U410)  
70 dB Minimum CMRR (U410)
- Low Drift with Temperature  
10  $\mu\text{V}/^\circ\text{C}$  Maximum (U410)
- Simplifies Amplifier Design  
Low Output Conductance

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |               |
|---|---------------|
| Gate-To-Gate Voltage                              | ±40 V         |
| Gate-Drain or Gate-Source Voltage                 | -40 V         |
| Gate Current                                      | 50 mA         |
| Total Package Dissipation (25°C Free-Air)         | 375 mW        |
| Power Derating                                    | 3.0 mW/°C     |
| Storage Temperature Range                         | -65 to +150°C |
| Lead Temperature (1/16" from case for 10 seconds) | 300°C         |



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | U410  |     |       | U411  |     |       | U412  |     |       | Unit                                 | Test Conditions  |
|--|-------|-----|-------|-------|-----|-------|-------|-----|-------|--------------------------------------|--|
|  | Min   | Typ | Max   | Min   | Typ | Max   | Min   | Typ | Max   |                                      |  |
| 1   I <sub>GSS</sub>   Gate Reverse Current (Note 1)                                     |       |     | -200  |       |     | -200  |       |     | -200  | pA                                   | V <sub>DS</sub> = 0, V <sub>GS</sub> = -30 V   |
| 2   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage                                    | -1.0  |     | -3.5  | -1.0  |     | -3.5  | -1.0  |     | -3.5  | V                                    | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA  |
| 3   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage                                    | -40   |     |       | -40   |     |       | -40   |     |       |                                      | V <sub>DS</sub> = 0 V, I <sub>G</sub> = -1 $\mu\text{A}$   |
| 4   I <sub>DSS</sub>   Saturation Drain Current (Note 2)                                 | 0.5   |     | 5.0   | 0.5   |     | 5.0   | 0.5   |     | 5.0   | mA                                   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 5   I <sub>G</sub>   Gate Current (Note 1)   |       |     | -200  |       |     | -200  |       |     | -200  | pA                                   | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$   |
| 6   V <sub>GS</sub>   Gate-Source Voltage  | -0.2  |     | -3.0  | -0.2  |     | -3.0  | -0.2  |     | -3.0  | V                                    |  |
| 7   g <sub>fs</sub>   Common-Source Forward Transconductance                             | 1,000 |     | 4,000 | 1,000 |     | 4,000 | 1,000 |     | 4,000 | $\mu\text{mho}$                      | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 8   g <sub>os</sub>   Common-Source Output Conductance                                   | 600   |     | 1,200 | 600   |     | 1,200 | 600   |     | 1,200 |                                      | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$   |
| 9   g <sub>os</sub>   Common-Source Output Conductance                                   |       |     | 20    |       |     | 20    |       |     | 20    |                                      | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 10   g <sub>os</sub>   Common-Source Output Conductance                                  |       |     | 5     |       |     | 5     |       |     | 5     | $\mu\text{mho}$                      | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$   |
| 11   C <sub>iss</sub>   Common-Source Input Capacitance                                  |       | 4.5 |       |       | 4.5 |       |       | 4.5 |       | pF                                   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 12   C <sub>rss</sub>   Common-Source Reverse Transfer Capacitance                       |       | 1.2 |       |       | 1.2 |       |       | 1.2 |       | pF                                   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V  |
| 13   e <sub>n</sub>   Equivalent Short-Circuit Input Noise Voltage                       |       |     | 50    |       |     | 50    |       |     | 50    | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$   |
| 14    V <sub>GS1</sub> -V <sub>GS2</sub>     Differential Gate-Source Voltage            |       |     | 10    |       |     | 20    |       |     | 40    | mV                                   | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$   |
| 15   $\frac{\Delta V_{GS1}-V_{GS2}}{\Delta T}$   Gate-Source Differential Drift (Note 3) |       |     | 10    |       |     | 25    |       |     | 80    | $\mu\text{V}/^\circ\text{C}$         | V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 $\mu\text{A}$<br>T <sub>A</sub> = 25°C to T <sub>B</sub> = 85°C |
| 16   CMRR   Common-Mode Rejection Ratio (Note 4)   |       | 80  |       |       | 80  |       |       | 70  |       | dB                                   | V <sub>DD</sub> = 10 V to V <sub>DD</sub> = 20 V<br>I <sub>D</sub> = 200 $\mu\text{A}$                       |

#### NOTES:

- Approximately doubles for every 10°C increase in T<sub>A</sub>.
- Pulse test duration = 300  $\mu\text{sec}$ ; duty cycle  $\leq$  3%.
- Measured at end points, T<sub>A</sub> and T<sub>B</sub>.
- CMRR = 20 log<sub>10</sub>  $\left[ \frac{\Delta V_{DD}}{\Delta |V_{GS1}-V_{GS2}|} \right]$ ,  $\Delta V_{DD} = 10 \text{ V}$ .

NQP

3

Siliconix

# monolithic dual n-channel JFETs designed for . . .



**Performance Curves NQT**  
See Section 5

**BENEFITS**

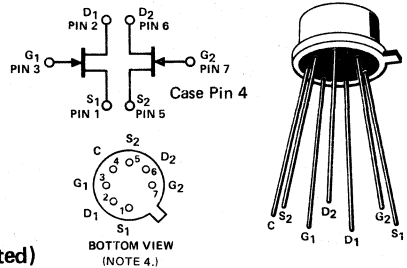
- High Input Impedance  
 $I_G = 0.1 \text{ pA}$  Maximum (U421-3)
- High Gain  $g_{fs} = 140 \text{ } \mu\text{mho}$  Minimum @  
 $I_D = 30 \text{ } \mu\text{A}$  (U421-3)
- Low Power Supply Operation  
 $V_{GS(\text{off})} = 2 \text{ V}$  Maximum (U421-3)
- Minimum System Error and Calibration  
10 mV Maximum Offset  
90 dB Minimum CMRR (U421, U424)

- Very High Input Impedance Differential Amplifiers
- Electrometers
- Impedance Converters

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |               |
|---|---------------|
| Gate-to-Gate Voltage  | ±40 V         |
| Gate-Drain or Gate-Source Voltage   | -40 V         |
| Gate Current  | 10 mA         |
| Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$<br>(Derate 3.2 mW/°C to 150°C) | 400 mW        |
| Total Device Dissipation, $T_A = 25^\circ\text{C}$<br>(Derate 6.0 mW/°C to 150°C)       | 750 mW        |
| Storage Temperature Range   | -65 to +150°C |

TO-78  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

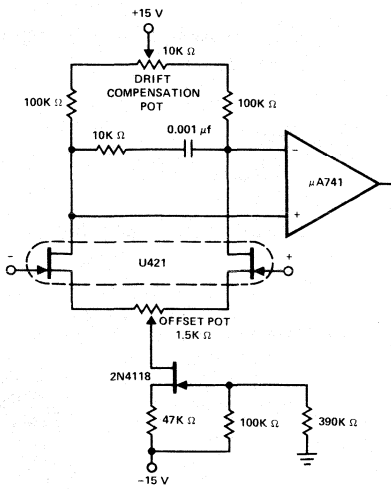
| Characteristic                  |                | U421-3                                 |   |      | U424-6  |      |      | Unit    | Test Conditions                                     |   |   |                       |   |
|---------------------------------|----------------|--|---|------|---------|------|------|---------|---|---|---|-----------------------|---|
|                                 |                | Min                                    | Typ   | Max  | Min     | Typ  | Max  |         |   |   |   |                       |   |
| S<br>T<br>A<br>T<br>I<br>C      | 1              | BV <sub>GS</sub>                       | Gate-Source Breakdown Voltage                                     | -40  | -60     |      |      |         | V   | $I_G = -1 \text{ } \mu\text{A}$ , $V_{DS} = 0$            |   |                       |   |
|                                 | 2              | BV <sub>G1G2</sub>                     | Gate-Gate Breakdown Voltage                                       | ±40  |         |      | ±40  |         |   | $I_G = -1 \text{ } \mu\text{A}$ , $I_D = 0$ , $I_S = 0$   |   |                       |   |
|                                 | 3              | I <sub>GSS</sub>                       | Gate Reverse Current (Note 1)                                     |      |         | 0.2  |      | 1.0     | ρA  | $T = +25^\circ\text{C}$                                   | $V_{GS} = -20 \text{ V}$ , $V_{DS} = 0$                   |                       |   |
|                                 |                |  |   |      |         | 0.5  |      | 1.0     | nA  | $T = +125^\circ\text{C}$                                  |   |                       |   |
| 4                               | I <sub>G</sub> | Gate Operating Current (Note 1)        |   |      | 0.1     |      | 0.5  | ρA      | $T = +25^\circ\text{C}$<br>$T = +125^\circ\text{C}$ | $V_{DG} = 10 \text{ V}$ , $I_D = 30 \text{ } \mu\text{A}$ |   |                       |   |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | 5              | V <sub>GS(off)</sub>                   | Gate-Source Cutoff Voltage  | -0.4 |         | -2.0 | -0.4 |         | -3.0  | V   | $V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ nA}$            |                       |   |
|                                 | 6              | V <sub>GS</sub>                        | Gate-Source Voltage   |      |         | -1.8 |      |         | -2.9  |   | $V_{DG} = 10 \text{ V}$ , $I_D = 30 \text{ } \mu\text{A}$ |                       |   |
|                                 | 7              | I <sub>DSS</sub>                       | Saturation Drain Current  | 60   |         | 1000 | 60   |         | 1800  | μA  | $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$                    |                       |   |
|                                 | 8              | g <sub>fs</sub>                        | Common-Source Forward Transconductance                            | 300  |         | 800  | 300  |         | 1000  | μS  | $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$                    | f = 1 kHz             |   |
|                                 | 9              | g <sub>os</sub>                        | Common-Source Output Conductance                                  |      |         | 3.0  |      |         | 5.0   |   |   | f = 1 MHz             |   |
|                                 | 10             | C <sub>iss</sub>                       | Common-Source Input Capacitance                                   |      |         | 3.0  |      |         | 3.0   | pF  |   | f = 1 MHz             |   |
|                                 | 11             | C <sub>rss</sub>                       | Common-Source Reverse Transfer Capacitance                        |      |         | 1.5  |      |         | 1.5   |   |   | f = 1 MHz             |   |
|                                 | 12             | g <sub>fs</sub>                        | Common-Source Forward Transconductance                            | 140  |         | 250  | 135  |         | 300   | μS  | $V_{DG} = 10 \text{ V}$ , $I_D = 30 \text{ } \mu\text{A}$ | f = 1 kHz             |   |
|                                 | 13             | g <sub>os</sub>                        | Common-Source Output Conductance                                  |      |         | 0.5  |      |         | 1.0   |   |   | f = 10 Hz             |   |
|                                 | 14             | -e <sub>n</sub>                        | Equivalent Short Circuit Input Noise Voltage                      |      |         | 20   | 50   |         | 20  | 70  |   | nV $\sqrt{\text{Hz}}$ | f = 1 kHz   |
| 15                              | NF             | Noise Figure                           |   |      | 1.0     |      |      | 1.0     | dB  |   | f = 10 Hz<br>$R_G = 10 \text{ M } \Omega$                 |                       |   |
| Characteristic                  |                | U421, 4                                |   |      | U422, 5 |      |      | U423, 6 |   |   | Unit  | Test Conditions       |   |
|                                 |                | Min                                    | Typ   | Max  | Min     | Typ  | Max  | Min     | Typ   | Max   |   |                       |   |
| M<br>A<br>T<br>C<br>H           | 16             | V <sub>GS1</sub> - V <sub>GS2</sub>    | Differential Gate-Source Voltage                                  |      |         | 10   |      |         | 15  |   | 25  | mV                    | $V_{DG} = 10 \text{ V}$ , $I_D = 30 \text{ } \mu\text{A}$   |
|                                 | 17             | $\frac{ V_{GS1} - V_{GS2} }{\Delta T}$ | Differential Gate-Source Voltage Change With Temperature (Note 2) |      |         | 10   |      |         | 25  |   | 40  | μV/°C                 | $V_{DG} = 10 \text{ V}$ , $I_D = 30 \text{ } \mu\text{A}$ ,<br>$T_A = -55^\circ\text{C}$ , $T_B = 25^\circ\text{C}$ , $T_C = 125^\circ\text{C}$ |
|                                 | 18             | CMRR                                   | Common Mode Rejection Ratio (Note 3)                              | 90   | 95      |      | 80   | 90      |   | 80  | 90  | dB                    | $I_D = 30 \text{ } \mu\text{A}$ , $V_{DG} = 10 \text{ to } 20 \text{ V}$  |

**NOTES:**

1. Approximately doubles for every 10°C increase in  $T_A$ .
2. Measured at end points  $T_A$ ,  $T_B$  and  $T_C$ .
3.  $CMRR = 20 \log_{10} \left[ \frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right]$   $\Delta V_{DD} = 10 \text{ V}$ .
4. Case lead not connected.

**NQT**

Very Low Leakage FET Input Op Amps



NOTE: Pin 4 (case) is isolated from the substrate and should be left floating.

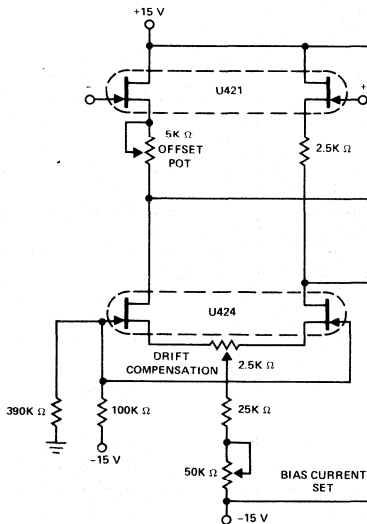
For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

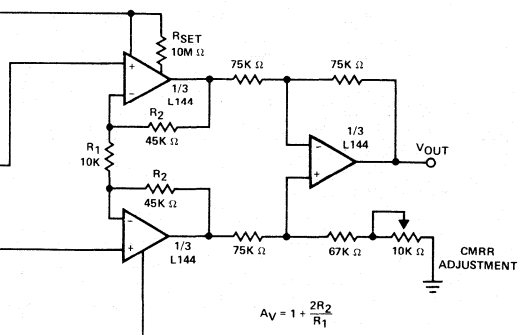
- $I_G$  = 0.1 pA at  $V_{cm} = 0$
- Offset = Can be nulled to 0 volts
- Drift = Can be nulled to  $2 \mu V/^\circ C$
- Slew Rate = 0.5 V/ $\mu s$

Electrometer Amplifier



L144CJ

Instrumentation Amplifier



$$A_V = 1 + \frac{2R_2}{R_1}$$

- Voltage Gain = 10
- Input Current = 0.1 pA
- Compensated Drift =  $3 \mu V/^\circ C$
- Nullified Offset = 0 mV
- CMRR = 80 dB typical
- Power Consumption = Approx. 30 Volt x 120  $\mu A$  = 3.6 mW

# matched dual n-channel JFETs designed for . . .



**Performance Curves NZA**  
See Section 5

- **Balanced Mixers**
- **Differential Amplifiers**

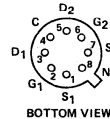
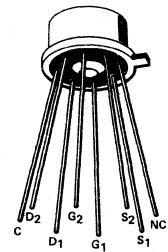
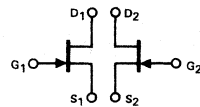
**BENEFITS**

- Low Noise Figure
- Low IMD  
30 dBm Intercept Point

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |                     |
|---|---------------------|
| Gate-Drain or Gate-Source Voltage   | ..... -25 V         |
| Gate Current  | ..... 10 mA         |
| Total Continuous Power Dissipation at<br>(or Below) 25°C Free Air Temperature<br>Derate 4 mW/°C to 150°C          | ..... 500 mW        |
| Continuous Device Dissipation (Each Side) at<br>(or Below) 25°C Free Air Temperature<br>Derate 2.4 mW/°C to 150°C | ..... 300 mW        |
| Storage Temperature Range   | ..... -65 to +200°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)  | ..... 300°C         |

**TO-99**  
See Section 7



**ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)**

| Characteristic                  |    | U430      |  |     | U431 |     |      | Unit       | Test Conditions                |             |                       |
|---------------------------------|----|-----------|--|-----|------|-----|------|------------|--------------------------------|-------------|-----------------------|
|                                 |    | Min       | Typ  | Max | Min  | Typ | Max  |            |                                |             |                       |
| S<br>T<br>A<br>T<br>I<br>C      | 1  | IGSS      | Gate Reverse Current                         |     |      |     | -150 | pA         | VGS = -15 V, VDS = 0 V         | T = 150°C   |                       |
|                                 | 2  |           |  |     | -150 | nA  |      |            |                                |             |                       |
|                                 | 3  | BVGS      | Gate-Source Breakdown Voltage                |     | -25  |     | -25  | V          |                                |             | IG = -1 μA, VDS = 0 V |
|                                 | 4  | VGS(off)  | Gate-Source Cutoff Voltage                   |     | -1.0 |     | -4.0 |            |                                |             |                       |
|                                 | 5  | VGS(f)    | Gate-Source Forward Voltage                  |     |      |     | 1.0  |            |                                |             |                       |
|                                 | 6  | IDSS      | Saturation Drain Current (Note 4)            |     | 12   |     | 30   |            |                                |             |                       |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | 7  | gfs       | Common-Source Forward Transconductance       |     | 10   |     | 20   | mmho       | VDS = 10 V, ID = 10 mA         | f = 1 kHz   |                       |
|                                 | 8  | gos       | Common-Source Output Conductance             |     |      |     | 200  | μmho       |                                |             |                       |
|                                 | 9  | Cgs       | Gate-Source Capacitance                      |     |      |     | 5.0  | pF         | VGS = -10 V, VDS = 0 V         | f = 1 MHz   |                       |
|                                 | 10 | Cgd       | Drain Gate Capacitance                       |     |      |     | 2.5  |            |                                |             |                       |
|                                 | 11 | en        | Equivalent Short-Circuit Input Noise Voltage |     |      |     | 10   | nV/√Hz     | VDS = 10 V, ID = 10 mA         | f = 100 Hz  |                       |
| H<br>I<br>F<br>R<br>E<br>Q      | 12 | gfs       | Common-Source Forward Transconductance       |     |      |     | 12   | mmho       | VDS = 10 V, ID = 10 mA         | f = 100 MHz |                       |
|                                 | 13 | gos       | Common-Source Output Conductance             |     |      |     | 0.15 |            |                                |             |                       |
|                                 | 14 | gig       | Power-Match Source Admittance                |     |      |     | 12   |            |                                |             |                       |
|                                 | 15 | Gc        | Conversion Gain (See Note 1)                 |     |      |     | 3.0  | dB         | VDS = 20 V, VGS = 1/2 VGS(off) |             |                       |
|                                 | 16 | IMD       | Intercept Point (See Notes 1 and 2)          |     |      |     | +30  | dBm        |                                |             |                       |
| M<br>A<br>T<br>C<br>H           | 17 | IDSS1     | Saturation Drain Current Ratio (Note 3)      |     | 0.9  |     | 1.0  | VDS = 10 V | VG = 0 V                       |             |                       |
|                                 | 18 | VGS(off)1 | Gate-Source Cutoff Voltage Ratio (Note 3)    |     | 0.9  |     | 1.0  |            | ID = 1 nA                      |             |                       |
|                                 |    | VGS(off)2 |  |     |      |     |      |            | ID = 10 mA                     |             |                       |
|                                 | 19 | gfs1      | Transconductance Ratio (Note 3)              |     | 0.9  |     | 1.0  |            |                                |             |                       |

**NOTES:**

1. VHF single-balanced mixer drain load impedance 2k Ω.
2. 2-tone 3rd-order IMD.
3. Assumes smaller value in numerator.
4. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

**NZA**

# matched dual n-channel JFETs designed for . . .



U440 U441

## ■ VHF/UHF Amplifiers

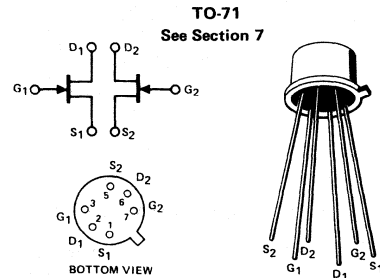
### Performance Curves NZF See Section 5

#### BENEFITS

- High Gain  
     $g_{fs} = 4500 \mu\text{mho}$  Minimum
- Dual Version of J300 with Matched Gate-to-Source Voltage

#### ABSOLUTE MAXIMUM RATINGS (25°C)

|  |               |
|--|---------------|
| Gate-To-Gate Voltage                                     | ±50 V         |
| Gate-Drain or Gate-Source Voltage                        | -25 V         |
| Gate Current   | 50 mA         |
| Total Package Dissipation<br>(25°C Free-Air Temperature) | 350 mW        |
| Power Derating   | 2.8 mW/°C     |
| Storage Temperature Range                                | -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)     | 300°C         |



#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

|    | Characteristic                  | U440          |       |     | U441  |       |       | Unit            | Test Conditions                             |   |
|----|---------------------------------|---------------|-------|-----|-------|-------|-------|-----------------|---|---|
|    |                                 | Min           | Typ   | Max | Min   | Typ   | Max   |                 |   |   |
| 1  | S<br>T<br>A<br>T<br>I<br>C      | $I_{GSS}$     |       |     | -500  |       |       | pA              | $V_{DS} = 0, V_{GS} = -15 \text{ V}$        |   |
| 2  |                                 | $V_{GS(off)}$ | -1    |     | -6    | -1    |       | V               | $V_{DS} = 10 \text{ V}, I_D = 1 \text{ nA}$ |   |
| 3  |                                 | $BV_{GSS}$    | -25   |     |       | -25   |       |                 | $V_{DS} = 0, I_G = -1 \mu\text{A}$          |   |
| 4  | D<br>Y<br>N<br>A<br>M<br>I<br>C | $I_{DSS}$     | 6     |     | 30    | 6     | 30    | mA              | $V_{DS} = 10 \text{ V}, V_{GS} = 0$         |   |
| 5  |                                 | $I_G$         |       |     |       |       |       | -500            | pA  | $V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$ |
| 6  | M<br>A<br>T                     | $g_{fs}$      | 4,500 |     | 9,000 | 4,500 | 9,000 | $\mu\text{mho}$ | $V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$ | $f = 1 \text{ kHz}$                         |
| 7  |                                 | $g_{os}$      |       |     | 200   |       | 200   |                 |   |   |
| 8  |                                 | $C_{iss}$     |       | 3.5 |       |       | 3.5   |                 | pF  | $f = 1 \text{ MHz}$                         |
| 9  | $C_{rss}$                       |               | 0.8   |     |       | 0.8   |       |                 |   |   |
| 10 | $ V_{GS1} - V_{GS2} $           |               |       | 10  |       |       | 20    | mV              | $V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$ |   |

#### NOTES:

1. Approximately doubles for every 10°C increase in  $T_A$ .
2. Pulse test duration = 300  $\mu\text{sec}$ ; duty cycle  $\leq 3\%$ .

NZF

3

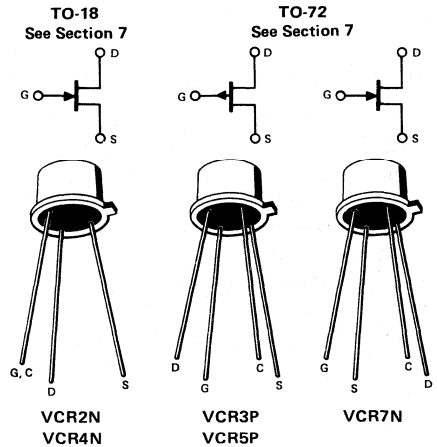
Siliconix

# voltage-controlled resistor FETs designed for . . .



Performance Curves NC NP NT PC PE See Section 5

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control



**ABSOLUTE MAXIMUM RATING (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . 15 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at T<sub>A</sub> = 25°C  
 (Derate at 2.0 mW/°C to 175°C) . . . . . 300 mW  
 Storage Temperature Range . . . . . -55 to +175°C

**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

**N-Channel VCR FETs**

| Characteristic   | VCR2N |     | VCR4N |      | VCR7N |       | Unit | Test Conditions                                      |
|--|-------|-----|-------|------|-------|-------|------|--|
|  | Min   | Max | Min   | Max  | Min   | Max   |      |  |
| 1 <b>S</b>   I <sub>GSS</sub>   Gate Reverse Current           |       | -5  |       | -0.2 |       | -0.1  | nA   | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0         |
| 2 <b>T</b>   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage | -15   |     | -15   |      | -15   |       | V    | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0          |
| 3 <b>A</b>   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage | -3.5  | -7  | -3.5  | -7   | -2.5  | -5    |      | I <sub>D</sub> = 1 μA, V <sub>DS</sub> = 10 V        |
| 4 <b>T</b>   r <sub>ds(on)</sub>   Drain Source ON Resistance  | 20    | 60  | 200   | 600  | 4,000 | 8,000 | Ω    | V <sub>GS</sub> = 0, I <sub>D</sub> = 0<br>f = 1 kHz |
| 5 <b>D</b>   C <sub>dgo</sub>   Drain-Gate Capacitance         |       | 7.5 |       | 3    |       | 1.5   | pF   | V <sub>GD</sub> = -10 V, I <sub>S</sub> = 0          |
| 6 <b>Y</b>   C <sub>sgo</sub>   Source-Gate Capacitance        |       | 7.5 |       | 3    |       | 1.5   |      | V <sub>GS</sub> = -10 V, I <sub>D</sub> = 0          |

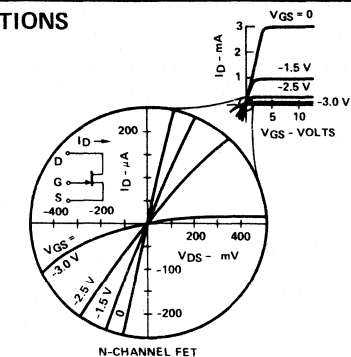
NC NP NT

**P-Channel VCR FETs**

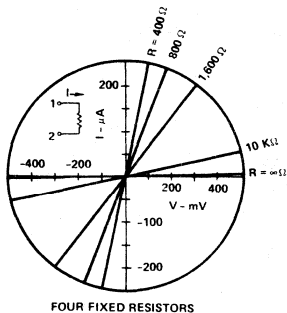
| Characteristic   | VCR3P |     | VCR5P |     | Unit | Test Conditions                                      |
|--|-------|-----|-------|-----|------|--|
|  | Min   | Max | Min   | Max |      |  |
| 1 <b>S</b>   I <sub>GSS</sub>   Gate Reverse Current           |       | 20  |       | 10  | nA   | V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0          |
| 2 <b>T</b>   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage | 15    |     | 15    |     | V    | I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0           |
| 3 <b>A</b>   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage | 3.5   | 7   | 3.5   | 7   |      | I <sub>D</sub> = -1 μA, V <sub>DS</sub> = -10 V      |
| 4 <b>T</b>   r <sub>ds(on)</sub>   Drain-Source ON Resistance  | 70    | 200 | 300   | 900 | Ω    | V <sub>GS</sub> = 0, I <sub>D</sub> = 0<br>f = 1 kHz |
| 5 <b>D</b>   C <sub>dgo</sub>   Drain-Gate Capacitance         |       | 6   |       | 3   | pF   | V <sub>GD</sub> = 10 V, I <sub>S</sub> = 0           |
| 6 <b>Y</b>   C <sub>sgo</sub>   Source-Gate Capacitance        |       | 6   |       | 3   |      | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0           |

PE PC

APPLICATIONS



N-Channel JFET Output Characteristic Enlarged Around  $V_{DS} = 0$  Figure 1



FOUR FIXED RESISTORS V-I Characteristic of Four Fixed Resistors Figure 2

The VCR FET has an a-c drain-source resistance, evaluated around  $V_{DS} = 0$ , that is controlled by d-c bias voltage  $V_{GS}$  applied to the high-impedance gate terminal. Minimum  $r_{ds}$  occurs when  $V_{GS} = 0$  and, as  $V_{GS}$  approaches the pinch-off voltage,  $r_{ds}$  rapidly increases. Comparing Fig. 1 and 2, for  $V_{DS} < \pm 0.1$  volt and  $V_{GS} = \text{constant}$ , the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when  $V_{DS} > \pm 0.1$  volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around  $V_{DS} = 0$ . In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when  $V_{GS}$  is near zero and  $v_{ds} > 0.5$  volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of  $V_{GS}$  and  $v_{ds}$ , it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of  $r_{DS}$  versus normalized  $V_{GS}$  where  $V_{GS(off)}$  is defined as that value of  $V_{GS}$  at  $I_D/I_{DSS} = 0.001$ . The dynamic range of  $r_{DS}$  is shown as greater than 100:1. For best control of  $r_{DS}$  the normalized  $V_{GS}$  should lie between 0 and 0.8  $V_{GS(off)}$  because as

$V_{GS}$  approaches  $V_{GS(off)}$ ,  $r_{DS}$  increases very rapidly so that  $r_{ds}$  control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4,  $r_{ds(on)}$  (drain-source resistance at  $V_{DS} = V_{GS} = 0$ ) varies as an inverse function of  $V_{GS(off)}$ . In Fig. 5  $r_{ds}$  has a typical  $0.7\%/^{\circ}\text{C}$  temperature coefficient for P-channels which decreases as  $V_{GS}$  approaches the zero t.c. point. N-channel devices have a typical  $0.3\%/^{\circ}\text{C}$  t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does  $V_{GS(off)}$ , from device to device.\*

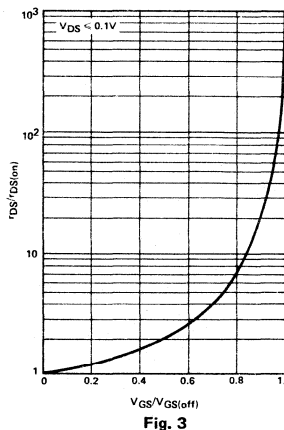


Fig. 3

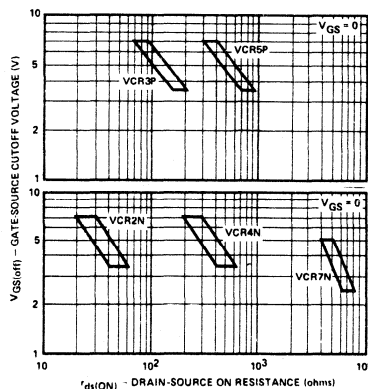


Fig. 4

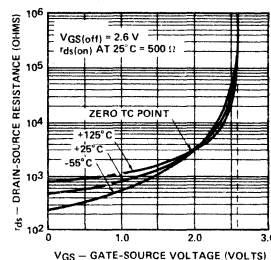


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

\* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.





# **data sheets plastic**

**index 4**



# n-channel JFET designed for . . .



2N3819

- General Purpose Amplifiers
- Analog Switching

Performance Curves NRL  
See Section 5

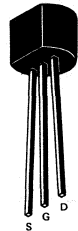
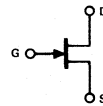
**BENEFITS**

- Low Cost
- Specified at 100 MHz
- Automatic Insertion Package

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |                 |
|--|-----------------|
| Drain-Gate Voltage . . . . .   | 25 V            |
| Drain-Source Voltage . . . . .   | 25 V            |
| Reverse Gate-Source Voltage . . . . .  | -25 V           |
| Gate Current . . . . .   | 10 mA           |
| Continuous Device Dissipation<br>at (or Below) 25°C Free Air Temperature<br>(Note 1) . . . . . | 200 mW          |
| Storage Temperature Range . . . . .  | -55°C to +150°C |
| Lead Temperature<br>(1/16" from Case for 10 seconds) . . . . .                                 | 260°C           |

TO-92  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

|    |                                 | Characteristic  | Min  | Max  | Unit | Test Conditions                                      |                        |
|----|---------------------------------|---|------|------|------|--|------------------------|
| 1  | S<br>T<br>A<br>T<br>I<br>C      | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | -25  |      | V    | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0          |                        |
| 2  |                                 | I <sub>GSS</sub> Gate Reverse Current                       |      | -2   | nA   | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0         | T <sub>A</sub> = 100°C |
| 3  |                                 | I <sub>DSS</sub> Saturation Drain Current                   | 2    | 20   | mA   |  |                        |
| 4  |                                 | V <sub>GS</sub> Gate-Source Voltage                         | -0.5 | -7.5 | V    | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 200 μA      |                        |
| 5  |                                 | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage             |      | -8   | V    | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 nA        |                        |
| 6  |                                 |   |      |      |      |  |                        |
| 7  | D<br>Y<br>N<br>A<br>M<br>I<br>C | y <sub>fs</sub>   Common-Source Forward Transfer Admittance | 2000 | 6500 | μmho | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 2) | f = 1 kHz              |
| 8  |                                 | y <sub>os</sub>   Common Source Output Admittance           |      | 50   | μmho |  |                        |
| 9  |                                 | C <sub>iss</sub> Common Source Input Capacitance            |      | 8    | pF   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0          | f = 1 MHz              |
| 10 |                                 | C <sub>rss</sub> Common Source Reverse Transfer Capacitance |      | 4    | pF   |  |                        |
| 11 |                                 | y <sub>fs</sub>   Common Source Forward Transfer Admittance | 1600 |      | μmho | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0          | f = 100 MHz            |

\*JEDEC registered data

NRL

**NOTES:**

1. Derate linearly to 125°C (free air temperature at a rate of 2 mW/°C).
2. Pulse tested pulse width = 100 ms, duty cycle ≤ 10%.

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Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NRL**  
See Section 5

- General Purpose Amplifiers
- Switches

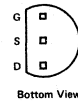
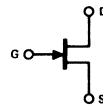
**BENEFITS**

- Low Cost
- Automated Insertion Package

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

|                                  |               |
|----------------------------------|---------------|
| Drain-Source Voltage             | 25 V          |
| Drain-Gate Voltage               | 25 V          |
| Source-Gate Voltage              | 25 V          |
| Total Device Dissipation at 25°C | 310 mW        |
| Derate above 25°C                | 2.82 mW/°C    |
| Operating Junction Temperature   | 135°C         |
| Storage Temperature Range        | -65 to +150°C |

TO-92  
See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic |             | 2N5457            |  |  | 2N5458 |      |       | 2N5459 |       |       | Unit  | Test Conditions  |      |  |   |
|----------------|-------------|-------------------|--|--|--------|------|-------|--------|-------|-------|-------|--|------|--|---|
|                |             | Min               | Typ                                    | Max  | Min    | Typ  | Max   | Min    | Typ   | Max   |       |  |      |  |   |
| 1              | S<br>T<br>A | I <sub>GSS</sub>  | Gate Reverse Current                   |  |        |      |       |        |       |       | nA    | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0<br>T <sub>A</sub> = +100°C                        |      |  |   |
| 2              |             |                   |  | -0.01                                      | -1.0   |      |       |        | -0.01 | -1.0  |       |  |      |  |   |
| 3              | A<br>T<br>I | BV <sub>GSS</sub> | Gate-Source Breakdown Voltage          |  | -25    | -60  |       | -25    | -60   |       | V     | I <sub>G</sub> = -10 μA, V <sub>DS</sub> = 0<br>V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 nA |      |  |   |
| 4              |             |                   | V <sub>GS(off)</sub>                   | Gate-Source Cutoff Voltage                 |        | -0.5 |       | -6.0   | -1.0  |       |       |  | -7.0 | -2.0   |   |
| 5              | C           | I <sub>DSS</sub>  | Saturation Drain Current               |  | 1.0    |      | 5.0   | 2.0    |       | 9.0   | 4.0   | 16   | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 1)     |   |
| 6              | D<br>Y      | g <sub>fs</sub>   | Common-Source Forward Transconductance |  | 1,000  |      | 5,000 | 1,500  |       | 5,500 | 2,000 | 6,000  | μmho | f = 1 kHz<br>V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 |   |
| 7              |             |                   | g <sub>os</sub>                        | Common-Source Output Conductance           |        |      | 10    | 50     |       | 15    | 50    |  |      |  | 20  |
| 8              | N<br>A      | C <sub>iss</sub>  | Common-Source Input Capacitance        |  |        | 4.5  | 7.0   |        | 4.5   | 7.0   |       | 4.5  | 7.0  | pF   | f = 1 MHz   |
| 9              |             |                   | C <sub>rss</sub>                       | Common-Source Reverse Transfer Capacitance |        |      | 1.0   | 3.0    |       | 1.0   | 3.0   |  | 1.0  |  |   |
| 10             | M<br>I<br>C | NF                | Noise Figure                           |  |        | .04  | 3.0   |        | .04   | 3.0   |       | .04  | 3.0  | dB   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0<br>R <sub>G</sub> = 1 MΩ, NBW = 1 Hz<br>f = 1 kHz |

\*JEDEC registered data

**NOTE:**

1. Pulse test pulsewidth = 2 ms.

**NRL**

# n-channel JFETs designed for . . .



- VHF/UHF Amplifiers
- Mixers
- Oscillators
- Analog Switches

## \*ABSOLUTE MAXIMUM RATINGS (25°C)

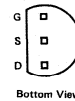
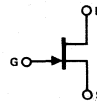
|  |                     |
|--|---------------------|
| Drain-Gate Voltage                                   | ..... 25 V          |
| Source Gate Voltage                                  | ..... 25 V          |
| Drain Current  | ..... 30 mA         |
| Forward Gate Current                                 | ..... 10 mA         |
| Total Device Dissipation @ 25°C                      | ..... 360 mW        |
| Derate above 25°C                                    | ..... 3.27 mW/°C    |
| Operating Junction Temperature Range                 | ..... -65 to +135°C |
| Storage Temperature Range                            | ..... -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) | ..... 240°C         |

## Performance Curves NH See Section 5

### BENEFITS

- Low Cost
- Completely Specified for 400 MHz Operation
- Low Error Analog Switch  
Very Little Charge Coupling  
 $C_{rss} < 1.0$  pF

TO-92  
See Section 7



## \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  | 2N5484                     |                                       | 2N5485 |       | 2N5486 |       | Unit  | Test Conditions  |
|---|----------------------------|---------------------------------------|--------|-------|--------|-------|-------|--|
|   | Min                        | Max                                   | Min    | Max   | Min    | Max   |       |  |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12<br>13<br>14<br>15<br>16<br>17<br>18<br>19<br>20<br>21<br>22<br>23 | S<br>T<br>A<br>T<br>I<br>C | I <sub>GSS</sub> Gate Reverse Current |        | -1.0  | -1.0   | -1.0  | nA    | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0                         |
| BV <sub>GSS</sub> Gate-Source Breakdown Voltage   |                            | -25                                   |        | -25   | -200   | -200  | V     | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0                          |
| V <sub>GS(off)</sub> Gate-Source Cutoff Voltage   |                            | -0.3                                  | -3.0   | -0.5  | -4.0   | -2.0  | -6.0  | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 nA                       |
| I <sub>DSS</sub> Saturation Drain Current   |                            | 1.0                                   | 5.0    | 4.0   | 10     | 8.0   | 20    | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 1)                 |
| g <sub>fs</sub> Common-Source Forward Transconductance  |                            | 3,000                                 | 6,000  | 3,500 | 7,000  | 4,000 | 8,000 | f = 1 kHz  |
| g <sub>os</sub> Common-Source Output Conductance  |                            | 50                                    |        | 60    |        | 75    |       | f = 100 MHz  |
| Re(v <sub>fs</sub> ) Common-Source Forward Transconductance   | 2,500                      |                                       |        | 3,000 |        | 3,500 | μmhos | f = 400 MHz  |
| Re(v <sub>os</sub> ) Common-Source Output Conductance   |                            | 75                                    |        | 100   |        | 100   |       | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0                          |
| Re(v <sub>is</sub> ) Common-Source Input Conductance  |                            | 100                                   |        | 1,000 |        | 1,000 |       | f = 100 MHz  |
| C <sub>iss</sub> Common-Source Input Capacitance  |                            | 5.0                                   |        | 5.0   |        | 5.0   | pF    | f = 400 MHz  |
| C <sub>rss</sub> Common-Source Reverse Transfer Capacitance   |                            | 1.0                                   |        | 1.0   |        | 1.0   |       | f = 1 MHz  |
| C <sub>oss</sub> Common-Source Output Capacitance   |                            | 2.0                                   |        | 2.0   |        | 2.0   |       |  |
| NF Noise Figure   |                            | 2.5                                   |        | 2.5   |        | 2.5   |       | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1 MΩ   |
|   |                            |                                       | 3.0    |       |        |       |       | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 mA, R <sub>G</sub> = 1 kΩ |
|   |                            |                                       |        | 2.0   |        | 2.0   |       | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4 mA, R <sub>G</sub> = 1 kΩ |
| G <sub>ps</sub> Common-Source Power Gain  | 16                         | 25                                    |        |       |        |       |       | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 mA                        |
|   |                            |                                       | 18     | 30    | 18     | 30    |       | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4 mA                        |
|   |                            |                                       | 10     | 20    | 10     | 20    |       | f = 400 MHz  |

\* JEDEC registered data

NH

### NOTE:

1 Pulse Test PW 300 μs, duty cycle ≤ 3%

2N5484 2N5485 2N5486

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Siliconix

# n-channel JFET designed for . . .



**Performance Curves NH**  
**See Section 5**

- **Analog Switches**
- **Choppers**
- **Commutators**

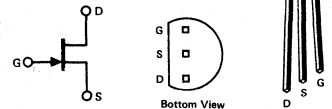
**BENEFITS**

- Low Cost
- Automatic Insertion Package
- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive
- Low Charge Coupling from Driver to Load  
 $C_{RSS} = 0.8 \text{ pF}$  Typically

**\* ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -25 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at (or Below)  $T_A = 25^\circ\text{C}$  . . 360 mW  
 (Derate 3.28 mW/°C to 135°C)  
 Operating Temperature Range . . . . . -55 to +135°C  
 Storage Temperature Range . . . . . -65 to +150°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 240°C

**TO-92**  
See Section 7



**\* ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

|                                 |    | Characteristic                                       | Min                               | Max  | Unit          | Test Conditions  |   |                           |
|---------------------------------|----|--|-----------------------------------|------|---------------|--|---|---------------------------|
| S<br>T<br>A<br>T<br>I<br>C      | 1  | $I_{GSS}$ Gate Reverse Current                       |                                   | -1.0 | nA            | $V_{GS} = -15 \text{ V}, V_{DS} = 0$   | $T_A = 100^\circ\text{C}$                       |                           |
|                                 |    |  |                                   | -0.2 | $\mu\text{A}$ |  |   |                           |
|                                 | 3  | $I_{DGO}$ Drain Leakage Current                      |                                   | 1.0  | nA            | $V_{DG} = 15 \text{ V}, I_S = 0$   | $T_A = 100^\circ\text{C}$                       |                           |
|                                 |    |  |                                   | 0.2  | $\mu\text{A}$ |  |   |                           |
|                                 | 5  | 6  | $I_{D(off)}$ Drain Cutoff Current |      | 10            | nA   | $V_{DS} = 12 \text{ V}, V_{GS} = -10 \text{ V}$ | $T_A = 100^\circ\text{C}$ |
|                                 |    |  |                                   |      | 2.0           | $\mu\text{A}$  |   |                           |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | 7  | $BV_{GSS}$ Gate-Source Breakdown Voltage             | -25                               |      | V             | $I_G = -10 \mu\text{A}, V_{DS} = 0$  |   |                           |
|                                 | 8  | $V_{GS(f)}$ Gate-Source Forward Voltage              |                                   | 1.0  |               | $I_G = 1 \text{ mA}, V_{DS} = 0$   |   |                           |
|                                 | 9  | $V_{DS(on)}$ Drain-Source ON Voltage                 |                                   | 1.5  |               | $I_D = 7 \text{ mA}, V_{GS} = 0$   |   |                           |
|                                 | 10 | $r_{DS(on)}$ Static Drain-Source ON Resistance       |                                   | 150  |               | $I_D = 0.1 \text{ mA}, V_{GS} = 0$   |   |                           |
|                                 | 11 | $I_{DSS}$ Saturation Drain Current                   | 15                                |      |               | $V_{DS} = 15 \text{ V}, V_{GS} = 0$  |   |                           |
| S<br>W<br>I<br>T<br>C<br>H      | 12 | $r_{ds(on)}$ Drain-Source ON Resistance              |                                   | 150  | $\Omega$      | $I_D = 0, V_{GS} = 0$ f = 1 kHz  |   |                           |
|                                 | 13 | $C_{iss}$ Common-Source Input Capacitance            |                                   | 5.0  |               | pF   | $V_{DS} = 15 \text{ V}, V_{GS} = 0$ f = 1 MHz   |                           |
|                                 | 14 | $C_{rss}$ Common-Source Reverse Transfer Capacitance |                                   | 1.2  |               |  | $V_{DS} = 0, V_{GS} = -10 \text{ V}$            |                           |
| S<br>W<br>I<br>T<br>C<br>H      | 15 | $t_{d(on)}$ Turn ON Delay Time                       |                                   | 5    | ns            | $V_{DD} = 10 \text{ V}, I_{D(on)} = 7 \text{ mA}, R_L = 1.21 \text{ K } \Omega$<br>$V_{GS(on)} = 0, V_{GS(off)} = -10 \text{ V}$ |   |                           |
|                                 | 16 | $t_r$ Rise Time                                      |                                   | 5    |               |  |   |                           |
|                                 | 17 | $t_{d(off)}$ Turn OFF Delay Time                     |                                   | 15   |               |  |   |                           |
|                                 | 18 | $t_f$ Fall Time                                      |                                   | 10   |               |  |   |                           |

\*JEDEC registered data

NH

# n-channel JFETs designed for . . .



- Analog Switches
- Commutators
- Choppers

## Performance Curves NC See Section 5

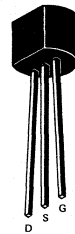
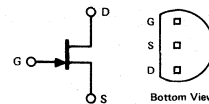
### BENEFITS

- Low Cost
- Industry Standard Package
- Automatic Insertion Package
- Fast Switching  
 $t_{rise} < 5 \text{ ns}$  (2N5638)
- Low Insertion Loss  
 $R_{DS(on)} < 30 \Omega$  (2N5638)
- Short Sample and Hold Aperture Time  
 $C_{rss} < 4 \text{ pF}$

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

|   |               |
|---|---------------|
| Drain-Source Breakdown Voltage                            | 30 V          |
| Drain-Gate Breakdown Voltage                              | 30 V          |
| Source-Gate Breakdown Voltage                             | 30 V          |
| Forward Gate Current                                      | 10 mA         |
| Total Device Dissipation at $T_{LEAD} = 25^\circ\text{C}$ | 625 mW        |
| Derate above 25°C   | 5.68 mW/°C    |
| Operating Junction Temperature Range                      | -65 to +135°C |
| Storage Temperature Range                                 | -65 to +150°C |
| Lead Temperature<br>(1/16" from case for 10 seconds)      | 300°C         |

TO-92  
See Section 7



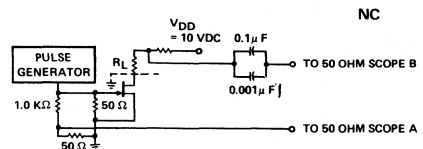
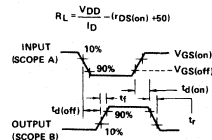
### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | 2N5638 |      | 2N5639 |      | 2N5640 |      | Unit          | Test Conditions   |
|--|--------|------|--------|------|--------|------|---------------|---|
|  | Min    | Max  | Min    | Max  | Min    | Max  |               |   |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage              | -30    |      | -30    |      | -30    |      | V             | $I_G = -10 \mu\text{A}, V_{DS} = 0$   |
| 2 IGSS Gate Reverse Current                                    |        | -1.0 |        | -1.0 |        | -1.0 | nA            | $V_{GS} = -15 \text{ V}, V_{DS} = 0$<br>$T_A = +100^\circ\text{C}$  |
|  | 3      |      | -1.0   |      | -1.0   |      | $\mu\text{A}$ |   |
| 4 ID(off) Drain Cutoff Current                                 |        | 1.0  |        | 1.0  |        | 1.0  | nA            | $V_{DS} = 15 \text{ V}, V_{GS} = -12 \text{ V}$ (2N5638)  |
| 5  |        | 1.0  |        | 1.0  |        | 1.0  | $\mu\text{A}$ | $V_{GS} = -8 \text{ V}$ (2N5639), $V_{GS} = -6 \text{ V}$ (2N5640)<br>$T_A = +100^\circ\text{C}$            |
| 6 IDSS Saturation Drain Current                                | 50     |      | 25     |      | 5.0    |      | mA            | $V_{DS} = 20 \text{ V}, V_{GS} = 0$ (Note 1)  |
| 7 V <sub>DS(on)</sub> Drain-Source ON Voltage                  |        | 0.5  |        | 0.5  |        | 0.5  | V             | $V_{GS} = 0, I_D = 12 \text{ mA}$ (2N5638),<br>$I_D = 6 \text{ mA}$ (2N5639), $I_D = 3 \text{ mA}$ (2N5640) |
| 8 r <sub>DS(on)</sub> Static Drain-Source ON Resistance        |        | 30   |        | 60   |        | 100  | $\Omega$      | $I_D = 1 \text{ mA}, V_{GS} = 0$  |
| 9 r <sub>ds(on)</sub> Drain-Source ON Resistance               |        | 30   |        | 60   |        | 100  | $\Omega$      | $V_{GS} = 0, I_D = 0$<br>$f = 1 \text{ kHz}$  |
| 10 C <sub>iss</sub> Common-Source Input Capacitance            |        | 10   |        | 10   |        | 10   | pF            | $V_{GS} = -12 \text{ V}, V_{DS} = 0$<br>$f = 1 \text{ MHz}$   |
| 11 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |        | 4.0  |        | 4.0  |        | 4.0  | pF            |   |
| 12 t <sub>d(on)</sub> Turn-On Delay Time                       |        | 4.0  |        | 6.0  |        | 8.0  | nsec          | $V_{DD} = 10 \text{ V}, I_{D(on)} = 12 \text{ mA}$ (2N5638) $R_L = 800 \Omega$ (2N5638)                     |
| 13 t <sub>r</sub> Rise Time                                    |        | 5.0  |        | 8.0  |        | 10   |               | $V_{GS(on)} = 0, I_{D(on)} = 6 \text{ mA}$ (2N5639) $R_L = 1.6 \text{ k}\Omega$ (2N5639)                    |
| 14 t <sub>d(off)</sub> Turn-OFF Delay Time                     |        | 5.0  |        | 10   |        | 15   |               | $V_{GS(off)} = -10 \text{ V}, I_{D(on)} = 3 \text{ mA}$ (2N5640) $R_L = 3.2 \text{ k}\Omega$ (2N5640)       |
| 15 t <sub>f</sub> Fall Time                                    |        | 10   |        | 20   |        | 30   |               |   |

\* JEDEC registered data

#### NOTE:

1 Pulse test  $PW \leq 300 \mu\text{sec}$ , duty cycle  $\leq 3.0\%$



SCOPE  
TEKTRONIX 587A  
OR EQUIVALENT

2N5638 2N5639 2N5640

4

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NC**  
See Section 5

- Analog Switches
- Commutators
- Choppers

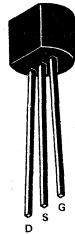
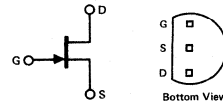
**BENEFITS**

- Low Cost
- Automatic Insertion Package
- High Speed  
 $t_{ON} + t_{OFF} = 24 \text{ ns Max (2N5653)}$
- Low Insertion Loss  
 $R_{DS(on)} = 50 \Omega \text{ Max (2N5653)}$

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Source Voltage . . . . . 30 V  
 Drain-Gate Voltage . . . . . 30 V  
 Source-Gate Voltage . . . . . 30 V  
 Forward Gate Current . . . . . 10 mA  
 Total Device Dissipation at (or Below)  $T_A = 25^\circ\text{C}$   
 (Derate 2.82 mW/°C to 135°C) . . . . . 360 mW  
 Operating Junction Temperature Range . . . . -65 to +135°C  
 Storage Temperature Range . . . . . -65 to +150°C

TO-92  
See Section 7



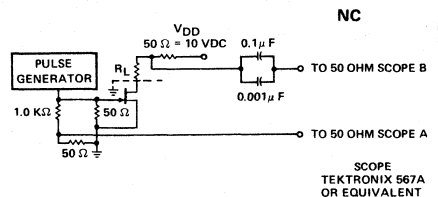
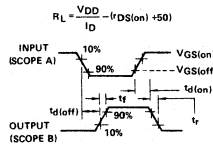
**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | 2N5653 |      | 2N5654 |      | Unit          | Test Conditions  |
|--|--------|------|--------|------|---------------|--|
|  | Min    | Max  | Min    | Max  |               |  |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage                | -30    |      | -30    |      | V             | $I_G = -10 \mu\text{A}, V_{DS} = 0$  |
| 2 S I <sub>GSS</sub> Gate Reverse Current                        |        | -1.0 |        | -1.0 | nA            | $V_{GS} = -15 \text{ V}, V_{DS} = 0$<br>$T_A = +100^\circ\text{C}$   |
| 3 T I <sub>D(off)</sub> Drain Cutoff Current                     |        | -1.0 |        | -1.0 | $\mu\text{A}$ |  |
| 4 A I <sub>D(off)</sub> Drain Cutoff Current                     |        | 1.0  |        | 1.0  | nA            | $V_{DS} = 15 \text{ V}, V_{GS} = -12 \text{ V (2N5653)}$<br>$V_{GS} = -8 \text{ V (2N5654)}$<br>$T_A = +100^\circ\text{C}$   |
| 5 I I <sub>DSS</sub> Saturation Drain Current                    |        | 1.0  |        | 1.0  | $\mu\text{A}$ |  |
| 6 C I <sub>DSS</sub> Saturation Drain Current                    | 40     |      | 15     |      | mA            | $V_{DS} = 20 \text{ V}, V_{GS} = 0$ (Note 1)   |
| 7 V <sub>DS(on)</sub> Drain-Source ON Voltage                    |        | 0.75 |        | 0.75 | V             | $V_{GS} = 0, I_D = 10 \text{ mA (2N5653)}, I_D = 5 \text{ mA (2N5654)}$  |
| 8 r <sub>DS(on)</sub> Static Drain-Source ON Resistance          |        | 50   |        | 100  | $\Omega$      | $I_D = 1 \text{ mA}, V_{GS} = 0$   |
| 9 r <sub>ds(on)</sub> Drain-Source ON Resistance                 |        | 50   |        | 100  |               | $V_{GS} = 0, I_D = 0$<br>$f = 1 \text{ kHz}$   |
| 10 D C <sub>iss</sub> Common-Source Input Capacitance            |        | 10   |        | 10   | $\text{pF}$   | $V_{GS} = -12 \text{ V}, V_{DS} = 0$<br>$f = 1 \text{ MHz}$  |
| 11 Y C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |        | 3.5  |        | 3.5  |               |  |
| 12 W t <sub>d(on)</sub> Turn-ON Delay Time                       |        | 4.0  |        | 6.0  | nsec          | $V_{DD} = 10 \text{ V}, I_{D(on)} = 10 \text{ mA (2N5653)}$<br>$V_{GS(on)} = 0, I_{D(on)} = 5 \text{ mA (2N5654)}$<br>$V_{GS(off)} = -12 \text{ V}, R_L = 925 \Omega \text{ (2N5653)}$<br>$R_L = 1.85\text{K} \Omega \text{ (2N5654)}$ |
| 13 S t <sub>r</sub> Rise Time                                    |        | 5.0  |        | 8.0  |               |  |
| 14 W t <sub>d(off)</sub> Turn-OFF Delay Time                     |        | 5.0  |        | 10   |               |  |
| 15 t <sub>f</sub> Fall Time                                      |        | 10   |        | 20   |               |  |

\*JEDEC registered data

**NOTE:**

1. Pulse test PW < 300  $\mu\text{s}$ , duty cycle < 3%.



SCOPE  
TEKTRONIX 567A  
OR EQUIVALENT



# n-channel JFETs designed for . . .



Performance Curves NH  
See Section 5

- VHF/UHF Amplifiers
- Mixers
- Oscillators

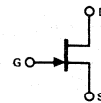
### BENEFITS

- Low Cost
- Automatic Insertion Package
- Specified for 100 MHz Operation

### \* ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Drain-Gate Voltage . . . . .  | 25 V         |
| Source-Gate Voltage . . . . .   | 25 V         |
| Drain-Source Voltage . . . . .  | 25 V         |
| Forward Gate Current . . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |

TO-92  
See Section 7



### \* ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  | 2N5668                          |          | 2N5669                                     |      | 2N5670 |      | Unit | Test Conditions |                      |                        |       |                              |           |
|---|---------------------------------|----------|--|------|--------|------|------|-----------------|----------------------|------------------------|-------|------------------------------|-----------|
|   | Min                             | Max      | Min  | Max  | Min    | Max  |      |                 |                      |                        |       |                              |           |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12<br>13<br>14<br>15 | S<br>T<br>A<br>T<br>I<br>C      | IGSS     | Gate Reverse Current                       |      |        |      |      | nA              | VGS = -15 V, VDS = 0 | TA = +100°C            |       |                              |           |
|   |                                 |          |  | -2.0 | -2.0   | -2.0 | -2.0 | μA              |                      |                        |       |                              |           |
|   | D<br>Y<br>N<br>A<br>M<br>I<br>C | BVGSS    | Gate-Source Breakdown Voltage              |      | -25    |      | -25  |                 | IG = -10 μA, VDS = 0 | VDS = 15 V, ID = 10 nA |       |                              |           |
|   |                                 | VGS(off) | Gate-Source Cutoff Voltage                 |      | 0.2    | 4.0  | 1.0  | 6.0             |                      |                        | 2.0   | 8.0                          |           |
|   |                                 | IDSS     | Saturation Drain Current                   |      | 1.0    | 5.0  | 4.0  | 10              | 8.0                  | 20                     | mA    | VDS = 15 V, VGS = 0 (Note 1) |           |
|   |                                 | gfs      | Common-Source Forward Transconductance     |      | 1500   | 6500 | 2000 | 6500            | 3000                 | 7500                   | μmhos | VDS = 15 V, VGS = 0          | f = 1 kHz |
|   |                                 | gos      | Common-Source Output Conductance           |      |        | 20   |      | 50              |                      | 75                     |       |                              |           |
|   |                                 | Re(yfs)  | Common-Source Forward Transconductance     |      | 1000   |      | 1600 |                 | 2500                 |                        | pF    | f = 100 MHz                  |           |
|   |                                 | Re(yos)  | Common-Source Output Conductance           |      |        | 50   |      | 100             |                      | 150                    |       |                              |           |
|   |                                 | Re(yis)  | Common-Source Input Conductance            |      |        | 800  |      | 800             |                      | 800                    |       |                              |           |
|   |                                 | Ciss     | Common-Source Input Capacitance            |      |        | 7.0  |      | 7.0             |                      | 7.0                    | pF    | f = 1 MHz                    |           |
|   |                                 | Crss     | Common-Source Reverse Transfer Capacitance |      |        | 3.0  |      | 3.0             |                      | 3.0                    |       |                              |           |
|   |                                 | Coss     | Common-Source Output Capacitance           |      |        | 4.0  |      | 4.0             |                      | 4.0                    |       |                              |           |
|   |                                 | NF       | Noise Figure                               |      |        | 2.5  |      | 2.5             |                      | 2.5                    | dB    | f = 100 MHz                  |           |
|   |                                 | Gps      | Common-Source Power Gain                   |      | 16     |      | 16   |                 | 16                   |                        |       |                              |           |

\*JEDEC registered data

NH

**NOTE:**

1. Pulse test PW = 300 μs, duty cycle ≤ 3%.

2N5668 2N5669 2N5670

4

Siliconix



# n-channel JFETs designed for . . .

- Analog Switches
- Choppers
- Commutators

**Performance Curves NVA**  
**See Section 5**

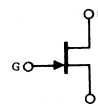
**BENEFITS**

- Very Low Insertion Loss  
 $R_{DS(on)} < 3 \Omega$  (J105)
- No Offset or Error Voltages Generated by Closed Switch  
 Purely Resistive  
 High Isolation Resistance from Driver

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . - 25 V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C). . . . . 360 mW  
 Operating Temperature Range. . . . . -55 to 135°C  
 Storing Temperature Range. . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

**TO-92**  
 See Section 7



(-18)

**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | J105 |     |     | J106 |     |     | J107 |     |      | Unit | Test Conditions  |
|--|------|-----|-----|------|-----|-----|------|-----|------|------|--|
|  | Min  | Typ | Max | Min  | Typ | Max | Min  | Typ | Max  |      |  |
| 1   I <sub>GSS</sub>   Gate Reverse Current (Note 1)                                       |      |     | -3  |      |     | -3  |      |     | -3   | nA   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -15 V   |
| 2   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage                                      | -4.5 |     | -10 | -2   |     | -6  | -0.5 |     | -4.5 | V    | V <sub>DS</sub> = 5 V, I <sub>D</sub> = 1 μA   |
| 3   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage                                      | -25  |     | -25 |      |     | -25 |      |     |      |      | V <sub>DS</sub> = 0 V, I <sub>G</sub> = -1 μA  |
| 4   I <sub>DSS</sub>   Drain Saturation Current (Note 2)                                   | 500  |     | 200 |      |     | 100 |      |     |      | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V  |
| 5   I <sub>D(off)</sub>   Drain Cutoff Current (Note 1)                                    |      |     | 3   |      |     | 3   |      |     | 3    | nA   | V <sub>DS</sub> = 5 V, V <sub>GS</sub> = -10 V   |
| 6   r <sub>DS(on)</sub>   Drain Source ON Resistance                                       |      |     | 3   |      |     | 6   |      |     | 8    | Ω    | V <sub>DS</sub> ≤ 0.1 V, V <sub>GS</sub> = 0 V   |
| 7   C <sub>dg(off)</sub>   Drain Gate OFF Capacitance                                      |      |     | 35  |      |     | 35  |      |     | 35   | pF   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -10 V<br><br>f = 1 MHz  |
| 8   C <sub>sg(off)</sub>   Source Gate OFF Capacitance                                     |      |     | 35  |      |     | 35  |      |     | 35   |      |  |
| 9   C <sub>dg(on)</sub> + C <sub>sg(on)</sub>   Drain Gate plus Source Gate ON Capacitance |      |     | 160 |      |     | 160 |      |     | 160  |      |  |
| 10   t <sub>d(on)</sub>   Turn On Delay Time   |      | 15  |     |      | 15  |     |      | 15  |      | ns   | Switching Time Test Conditions<br>J105 1.5 V J106 1.5 V J107 1.5 V<br>V <sub>DD</sub> 1.5 V 1.5 V 1.5 V<br>V <sub>GS(off)</sub> -12 V -7 V -5 V<br>R <sub>L</sub> 50 Ω 50 Ω 50 Ω |
| 11   t <sub>r</sub>   Rise Time  |      | 20  |     |      | 20  |     |      | 20  |      |      |  |
| 12   t <sub>d(off)</sub>   Turn Off Delay Time   |      | 15  |     |      | 15  |     |      | 15  |      |      |  |
| 13   t <sub>f</sub>   Fall Time  |      | 20  |     |      | 20  |     |      | 20  |      |      |  |

**NOTES:**

1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NVA

# n-channel JFETs designed for . . .



- Analog Switches
- Choppers
- Commutators
- Low Noise Audio Amplifiers

## Performance Curves NIP See Section 5

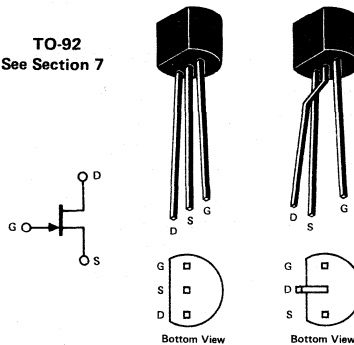
### BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss  
 $R_{DS(on)} < 8 \Omega$  (J108)
- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive  
High Isolation Resistance from Driver
- Fast Switching  
 $t_{D(on)} + t_r = 5$  ns Typical
- Low Noise  
 $\bar{e}_n = 6$  nV/ $\sqrt{\text{Hz}}$  at 10 Hz, Typ (J110)

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |                   |
|---|-------------------|
| Gate-Drain or Gate-Source Voltage                               | .....-25V         |
| Gate Current  | ..... 50 mA       |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | ..... 360 mW      |
| Operating Temperature Range                                     | .....-55 to 135°C |
| Storage Temperature Range                                       | .....-55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | .....300°C        |

TO-92  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | J108 |     |     | J109 |     |     | J110 |     |     | Unit     | Test Conditions   |
|--|------|-----|-----|------|-----|-----|------|-----|-----|----------|---|
|  | Min  | Typ | Max | Min  | Typ | Max | Min  | Typ | Max |          |   |
| 1   S   $I_{GSS}$   Gate Reverse Current (Note 1)                              |      |     | -3  |      |     | -3  |      |     | -3  | nA       | $V_{DS} = 0$ V, $V_{GS} = -15$ V  |
| 2   T   $V_{GS(off)}$   Gate-Source Cutoff Voltage                             | -3   |     | -10 | -2   |     | -6  | -0.5 |     | -4  | V        | $V_{DS} = 5$ V, $I_D = 1$ $\mu$ A   |
| 3   A   $BV_{GSS}$   Gate-Source Breakdown Voltage                             | -25  |     |     | -25  |     |     | -25  |     |     | V        | $V_{DS} = 0$ V, $I_G = -1$ $\mu$ A  |
| 4   I   $I_{DSS}$   Drain Saturation Current (Note 2)                          | 80   |     |     | 40   |     |     | 10   |     |     | mA       | $V_{DS} = 15$ V, $V_{GS} = 0$ V   |
| 5   C   $I_{D(off)}$   Drain Cutoff Current (Note 1)                           |      |     | 3   |      |     | 3   |      |     | 3   | nA       | $V_{DS} = 5$ V, $V_{GS} = -10$ V  |
| 6     $r_{DS(on)}$   Drain-Source ON Resistance                                |      |     | 8   |      |     | 12  |      |     | 18  | $\Omega$ | $V_{DS} \leq 0.1$ V, $V_{GS} = 0$ V   |
| 7     $C_{dg(off)}$   Drain-Gate OFF Capacitance                               |      |     | 15  |      |     | 15  |      |     | 15  | pF       | $V_{DS} = 0$ V, $V_{GS} = -10$ V<br>$V_{DS} = V_{GS} = 0$<br>$f = 1$ MHz  |
| 8     $C_{sg(off)}$   Source-Gate OFF Capacitance                              |      |     | 15  |      |     | 15  |      |     | 15  |          |   |
| 9   D   $C_{dg(on)} + C_{sg(on)}$   Drain-Gate Plus Source-Gate ON Capacitance |      |     | 85  |      |     | 85  |      |     | 85  | ns       | Switching Time Test Conditions<br>J108 J109 J110<br>$V_{DD}$ 1.5 V 1.5 V 1.5 V<br>$V_{GS(off)}$ -12 V -7 V -5 V<br>$R_L$ 150 $\Omega$ 150 $\Omega$ 150 $\Omega$ |
| 10   M   $t_{d(on)}$   Turn ON Delay Time                                      |      | 4   |     | 4    |     | 4   |      |     |     |          |   |
| 11   I   $t_r$   Rise Time   |      | 1   |     | 1    |     | 1   |      |     |     |          |   |
| 12   C   $t_{d(off)}$   Turn OFF Delay Time                                    |      | 6   |     | 6    |     | 6   |      |     |     |          |   |
| 13     $t_f$   Fall Time   |      | 30  |     | 30   |     | 30  |      |     |     |          |   |

#### NOTES:

1. Approximately doubles for every 10°C increase in  $T_A$ .
2. Pulse Test duration 300  $\mu$ s; duty cycle  $\leq$  3%.

NIP

J108 J109 J110  
J108-18 J109-18 J110-18

4

Siliconix

# n-channel FETs designed for . . .

- Analog Switches
- Choppers
- Commutators

**Performance Curves NC**  
**See Section 5**

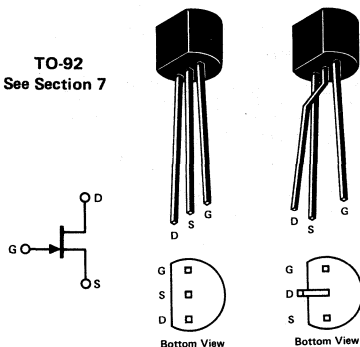
**BENEFITS**

- Low Cost
- Automated Insertion Package
- Low Insertion Loss  
 $R_{DS(on)} < 30 \Omega$  (J111)
- No Offset or Error Voltages Generated by Closed Switch  
 Purely Resistive  
 High Isolation Resistance from Driver
- Fast Switching  
 $t_{D(on)} + t_r = 13 \text{ ns Typical}$
- Short Sample and Hold Aperture Time  
 $C_{gd(off)} < 5 \text{ pF}$   
 $C_{gs(off)} < 5 \text{ pF}$

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -35V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

**TO-92**  
 See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | J111 |     |     | J112 |     |     | J113 |     |     | UNIT | Test Conditions  |
|--|------|-----|-----|------|-----|-----|------|-----|-----|------|--|
|  | Min  | Typ | Max | Min  | Typ | Max | Min  | Typ | Max |      |  |
| 1   I <sub>GSS</sub>   Gate Reverse Current (Note 1)                 |      |     | -1  |      |     | -1  |      |     | -1  | nA   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -15 V   |
| 2   V <sub>GS(off)</sub>   Gate Source Cutoff Voltage                | -3   |     | -10 | -1   |     | -5  | -0.5 |     | -3  | V    | V <sub>DS</sub> = 5 V, I <sub>D</sub> = 1 μA   |
| 3   BV <sub>GSS</sub>   Gate Source Breakdown Voltage                | 35   |     |     | 35   |     |     |      |     | -35 |      | V <sub>DS</sub> = 0 V, I <sub>G</sub> = -1 μA  |
| 4   I <sub>DSS</sub>   Drain Saturation Current (Note 2)             | 20   |     |     | 5    |     |     |      |     | 2   | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V  |
| 5   I <sub>D(off)</sub>   Drain Cutoff Current (Note 1)              |      |     | -1  |      |     | -1  |      |     | -1  | nA   | V <sub>DS</sub> = 5 V, V <sub>GS</sub> = -10 V   |
| 6   r <sub>DS(on)</sub>   Drain Source ON Resistance                 |      |     | 30  |      |     | 50  |      |     | 100 | Ω    | V <sub>DS</sub> = 0.1 V, V <sub>GS</sub> = 0 V   |
| 7   C <sub>dg(off)</sub>   Drain Gate OFF Capacitance                |      |     | 5   |      |     | 5   |      |     | 5   | pF   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -10 V<br>f = 1 MHz  |
| 8   C <sub>sg(off)</sub>   Source Gate OFF Capacitance               |      |     | 5   |      |     | 5   |      |     | 5   |      |  |
| 9   C <sub>dg(on)</sub>   Drain Gate Plus Source Gate ON Capacitance |      |     | 28  |      |     | 28  |      |     | 28  |      | V <sub>DS</sub> = V <sub>GS</sub> = 0  |
| 10   t <sub>d(on)</sub>   Turn On Delay Time                         |      | 7   |     |      | 7   |     |      | 7   |     | ns   | Switching Time Test Conditions<br>J111    J112    J113<br>V <sub>DD</sub> 10 V    10 V    10 V<br>V <sub>GS(off)</sub> -12 V    -7 V    -5 V<br>R <sub>L</sub> 800 Ω    1,600 Ω    3,200 Ω |
| 11   t <sub>r</sub>   Rise Time                                      |      | 6   |     |      | 6   |     |      | 6   |     |      |  |
| 12   t <sub>d(off)</sub>   Turn Off Delay Time                       |      | 20  |     |      | 20  |     |      | 20  |     |      |  |
| 13   t <sub>f</sub>   Fall Time                                      |      | 15  |     |      | 15  |     |      | 15  |     |      |  |

**NOTES:**

1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse Test duration 300 μs; duty cycle ≤ 3%.

**NC**

# n-channel JFET designed for . . .

- Analog Switches
- Choppers
- Commutators

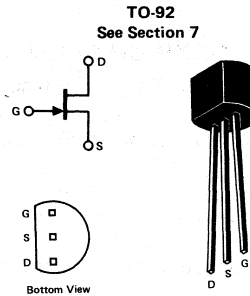
## Performance Curves NZF See Section 5

### BENEFITS

- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Very Fast Switching
  - $t_{D(on)} + t_r = 6$  ns Typical
- Short Sample and Hold Aperture Time
  - $C_{gd(off)} < 2$  pF
  - $C_{gs(off)} < 2$  pF

### ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                  |   | J114                                       |     |     | Unit | Test Conditions |  |
|---------------------------------|---|--|-----|-----|------|-----------------|--|
|                                 |   | Min  | Typ | Max |      |                 |  |
| S<br>T<br>A<br>T<br>I<br>C      | I <sub>GSS</sub>                          | Gate Reverse Current (Note 1)              |     |     | -1   | nA              | V <sub>DS</sub> = 0, V <sub>GS</sub> = -15 V   |
|                                 | V <sub>GS(off)</sub>                      | Gate-Source Cutoff Voltage                 |     |     | -3   | V               | V <sub>DS</sub> = 5 V, I <sub>D</sub> = 1 μA   |
|                                 | BV <sub>GSS</sub>                         | Gate-Source Breakdown Voltage              |     |     | -25  |                 | V <sub>DS</sub> = 0, I <sub>G</sub> = -1 μA  |
|                                 | I <sub>DSS</sub>                          | Saturation Drain Current (Note 2)          |     |     | 15   | mA              | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0  |
| D<br>Y<br>N<br>A<br>M<br>I<br>C | I <sub>D(off)</sub>                       | Drain Cutoff Current (Note 1)              |     |     | 1    | nA              | V <sub>DS</sub> = 5 V, V <sub>GS</sub> = -10 V   |
|                                 | r <sub>DS(on)</sub>                       | Drain-Source ON Resistance                 |     |     | 150  | Ω               | V <sub>DS</sub> ≤ 0.1 V, V <sub>GS</sub> = 0   |
|                                 | C <sub>dg(off)</sub>                      | Drain-Gate OFF Capacitance                 |     |     | 2    | pF              | V <sub>DS</sub> = 0, V <sub>GS</sub> = -10 V   |
|                                 | C <sub>sg(off)</sub>                      | Source-Gate OFF Capacitance                |     |     | 2    |                 |  |
|                                 | C <sub>dg(on)</sub> + C <sub>sg(on)</sub> | Drain-Gate Plus Source-Gate ON Capacitance |     |     | 8    |                 | V <sub>DS</sub> = V <sub>GS</sub> = 0  |
|                                 | t <sub>d(on)</sub>                        | Turn On Delay Time                         |     |     | 3    | ns              | Switching Time Test Conditions<br>V <sub>DD</sub> = 10 V, V <sub>GS(off)</sub> = -12 V<br>R <sub>L</sub> = 1 KΩ, V <sub>GS(on)</sub> = 0 |
|                                 | t <sub>r</sub>                            | Rise Time                                  |     |     | 3    |                 |  |
| t <sub>d(off)</sub>             | Turn Off Delay Time                       |  |     | 12  |      |                 |  |
| t <sub>f</sub>                  | Fall Time                                 |  |     | 8   |      |                 |  |

- NOTES:  
 1. Approximately doubles for every 10°C increase in T<sub>A</sub>.  
 2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NZF

# p-channel JFETs designed for . . .



- Analog Switches
- Choppers
- Commutators

## Performance Curves PS See Section 5

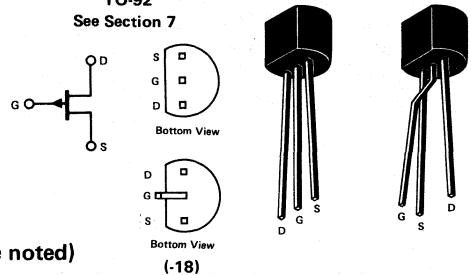
### BENEFITS

- Low Cost
- Simplifies Series-Shunt Switching when Combined with J113, its N-Channel Complement
- Low Insertion Loss  
 $R_{DS(on)} < 85 \Omega$  (J174)
- No Offset or Error Voltages Generated by Closed Switch  
 Purely Resistive  
 High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time  
 $C_{sg(off)} < 5.5 \text{ pF}$   
 $C_{dg(off)} < 5.5 \text{ pF}$
- Fast Switching  
 $t_d(on) + t_r = 7 \text{ ns Typical}$

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Gate-Drain or Gate-Source Voltage (Note 1)                      | 30V          |
| Gate Current  | 50 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | 360 mW       |
| Operating Temperature Range                                     | -55 to 135°C |
| Storage Temperature Range                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | 300°C        |

TO-92  
 See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristics  | J174         |                |                | J175          |     |     | J176 |     |     | J177 |     |      | Unit     | Test Conditions  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
|--|--------------|----------------|----------------|---------------|-----|-----|------|-----|-----|------|-----|------|----------|--|--|------|------|------|------|----------|-------|------|------|------|---------------|------|-----|-----|-----|-------|--------------|----------------|----------------|---------------|--------------|-----|-----|-----|-----|
|  | Min          | Typ            | Max            | Min           | Typ | Max | Min  | Typ | Max | Min  | Typ | Max  |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 1   $I_{GSS}$   Gate Reverse Current (Note 2)                              |              |                | 1              |               |     | 1   |      |     | 1   |      |     | 1    | nA       | $V_{DS} = 0, V_{GS} = 20 \text{ V}$  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 2   $V_{GS(off)}$   Gate-Source Cutoff Voltage                             | 5            |                | 10             | 3             |     | 6   | 1    |     | 4   | 0.8  |     | 2.25 | V        | $V_{DS} = -15 \text{ V}, I_D = -10 \text{ nA}$   |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 3   $BV_{GSS}$   Gate-Source Breakdown Voltage                             | 30           |                |                | 30            |     |     | 30   |     |     |      |     | 30   |          | $V_{DS} = 0, I_G = 1 \mu\text{A}$  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 4   $I_{DSS}$   Saturation Drain Current (Note 3)                          | -20          |                | -100           | -7            |     | -60 | -2   |     | -25 | -1.5 |     | -20  | mA       | $V_{DS} = -15 \text{ V}, V_{GS} = 0$   |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 5   $I_{D(off)}$   Drain Cutoff Current (Note 2)                           |              |                | -1             |               |     | -1  |      |     | -1  |      |     | -1   | nA       | $V_{DS} = -15 \text{ V}, V_{GS} = 10 \text{ V}$  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 6   $r_{DS(on)}$   Drain-Source ON Resistance                              |              |                | 85             |               |     | 125 |      |     | 250 |      |     | 300  | $\Omega$ | $V_{GS} = 0, V_{DS} = -0.1 \text{ V}$  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 7   $C_{dg(off)}$   Drain-Gate OFF Capacitance                             |              | 5.5            |                |               | 5.5 |     |      | 5.5 |     |      |     | 5.5  | pF       | $V_{DS} = 0, V_{GS} = 10 \text{ V}$<br><br>$V_{DS} = V_{GS} = 0$<br><br>$f = 1 \text{ MHz}$  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 8   $C_{sg(off)}$   Source-Gate OFF Capacitance                            |              | 5.5            |                |               | 5.5 |     |      | 5.5 |     |      |     | 5.5  |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 9   $C_{dg(on)} + C_{sg(on)}$   Drain-Gate Plus Source-Gate ON Capacitance |              | 32             |                |               | 32  |     |      | 32  |     |      |     | 32   |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 10   $t_d(on)$   Turn On Delay Time  |              | 2              |                |               | 5   |     |      | 15  |     |      |     | 20   | ns       | Switching Time Test Conditions<br><table border="0" style="font-size: small;"> <tr> <td></td> <td>J174</td> <td>J175</td> <td>J176</td> <td>J177</td> </tr> <tr> <td><math>V_{DD}</math></td> <td>-10 V</td> <td>-6 V</td> <td>-6 V</td> <td>-6 V</td> </tr> <tr> <td><math>V_{GS(off)}</math></td> <td>12 V</td> <td>8 V</td> <td>6 V</td> <td>3 V</td> </tr> <tr> <td><math>R_L</math></td> <td>560 <math>\Omega</math></td> <td>1.2 K<math>\Omega</math></td> <td>5.6 K<math>\Omega</math></td> <td>10 K<math>\Omega</math></td> </tr> <tr> <td><math>V_{GS(on)}</math></td> <td>0 V</td> <td>0 V</td> <td>0 V</td> <td>0 V</td> </tr> </table> |  | J174 | J175 | J176 | J177 | $V_{DD}$ | -10 V | -6 V | -6 V | -6 V | $V_{GS(off)}$ | 12 V | 8 V | 6 V | 3 V | $R_L$ | 560 $\Omega$ | 1.2 K $\Omega$ | 5.6 K $\Omega$ | 10 K $\Omega$ | $V_{GS(on)}$ | 0 V | 0 V | 0 V | 0 V |
|  | J174         | J175           | J176           | J177          |     |     |      |     |     |      |     |      |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| $V_{DD}$   | -10 V        | -6 V           | -6 V           | -6 V          |     |     |      |     |     |      |     |      |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| $V_{GS(off)}$  | 12 V         | 8 V            | 6 V            | 3 V           |     |     |      |     |     |      |     |      |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| $R_L$  | 560 $\Omega$ | 1.2 K $\Omega$ | 5.6 K $\Omega$ | 10 K $\Omega$ |     |     |      |     |     |      |     |      |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| $V_{GS(on)}$   | 0 V          | 0 V            | 0 V            | 0 V           |     |     |      |     |     |      |     |      |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 11   $t_r$   Rise Time   |              | 5              |                |               | 10  |     |      | 20  |     |      |     | 25   |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 12   $t_d(off)$   Turn Off Delay Time                                      |              | 5              |                |               | 10  |     |      | 15  |     |      |     | 20   |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |
| 13   $t_f$   Fall Time   |              | 10             |                |               | 20  |     |      | 20  |     |      |     | 25   |          |  |  |      |      |      |      |          |       |      |      |      |               |      |     |     |     |       |              |                |                |               |              |     |     |     |     |

**NOTES:**

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.

2. Approximately doubles for every 10°C increase in  $T_A$ . PS

3. Pulse test duration = 300  $\mu\text{s}$ ; duty cycle  $\leq 3\%$ .

# n-channel JFETs designed for . . .



## Performance Curves NP See Section 5

### ■ General Purpose Amplifiers

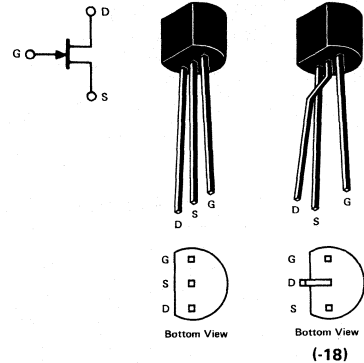
#### BENEFITS

- High Input Impedance  
 $I_G = 35 \text{ pA Typical}$
- Good for Low Power Supply Operation  
 $V_{GS(off)} < 1.5 \text{ V (J201)}$

#### ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -40 V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C). . . . . 360 mW  
 Operating Temperature Range. . . . . -55 to 135°C  
 Storage Temperature Range. . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92  
See Section 7



#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | J201 |     |      | J202  |     |      | J203  |     |       | Unit                   | Test Conditions                              |
|--|------|-----|------|-------|-----|------|-------|-----|-------|------------------------|--|
|  | Min  | Typ | Max  | Min   | Typ | Max  | Min   | Typ | Max   |                        |  |
| 1   <b>S</b>   $I_{GSS}$   Gate Reverse Current (Note 2)                   |      |     | -100 |       |     | -100 |       |     | -100  | pA                     | $V_{DS} = 0, V_{GS} = -20 \text{ V}$         |
| 2   <b>A</b>   $V_{GS(off)}$   Gate-Source Cutoff Voltage                  | -0.3 |     | -1.5 | -0.8  |     | -4.0 | -2.0  |     | -10.0 | V                      | $V_{DS} = 20 \text{ V}, I_D = 10 \text{ nA}$ |
| 3   <b>T</b>   $BV_{GSS}$   Gate-Source Breakdown Voltage                  | -40  |     |      | -40   |     |      | -40   |     |       |                        | $V_{DS} = 0, I_G = -1 \text{ }\mu\text{A}$   |
| 4   <b>I</b>   $I_{DSS}$   Saturation Drain Current (Note 3)               | 0.2  |     | 1.0  | 0.9   |     | 4.5  | 4.0   |     | 20    | mA                     | $V_{DS} = 20 \text{ V}, V_{GS} = 0$          |
| 5   <b>C</b>   $I_G$   Gate Current (Note 2)                               |      | -35 |      |       | -35 |      |       | -35 |       | pA                     | $V_{DG} = 20 \text{ V}, I_D = I_{DSS(min)}$  |
| 6   <b>D</b>   $g_{fs}$   Common-Source Forward Transconductance (Note 3)  | 500  |     |      | 1,000 |     |      | 1,500 |     |       | $\mu\text{mho}$        | $V_{DS} = 20 \text{ V}, V_{GS} = 0$          |
| 7   <b>Y</b>   $g_{os}$   Common-Source Output Conductance                 |      | 1   |      |       | 3.5 |      |       | 10  |       |                        |  |
| 8   <b>N</b>   $C_{iss}$   Common-Source Input Capacitance                 |      | 4   |      |       | 4   |      |       | 4   |       | pF                     | $f = 1 \text{ MHz}$                          |
| 9   <b>A</b>   $C_{rss}$   Common-Source Reverse Transfer Capacitance      |      | 1   |      |       | 1   |      |       | 1   |       |                        |  |
| 10   <b>M</b>   $\bar{e}_n$   Equivalent Short-Circuit Input Noise Voltage |      | 5   |      |       | 5   |      |       | 5   |       | $\frac{nV}{\sqrt{Hz}}$ | $V_{DS} = 10 \text{ V}, V_{GS} = 0$          |

- NOTES:**
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
  2. Approximately doubles for every 10°C increase in  $T_A$ .
  3. Pulse test duration = 2 ms.

NP

J201 J202 J203  
J201-18 J202-18 J203-18

# n-channel JFETs designed for . . .



**Performance Curves NP**  
**See Section 5**

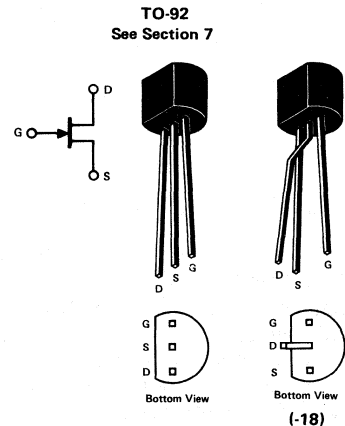
## ■ General Purpose Switching

### BENEFITS

- Very Low Leakage

### ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -25V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C). . . . . 360 mW  
 Operating Temperature Range. . . . . -55 to 135°C  
 Storage Temperature Range. . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  |               | J204   |      |      | Unit                   | Test Conditions                  |           |
|---|---------------|--|------|------|------------------------|----------------------------------|-----------|
|   |               | Min  | Typ  | Max  |                        |                                  |           |
| 1<br>2<br>3<br>4<br>5<br>S<br>T<br>A<br>T<br>I<br>C       | $I_{GSS}$     | Gate Reverse Current<br>(Note 2)                   |      | -100 | pA                     | $V_{DS} = 0, V_{GS} = -20 V$     |           |
|   | $V_{GS(off)}$ | Gate-Source Cutoff<br>Voltage                      | -0.5 | -2.0 | V                      | $V_{DS} = 20 V, I_D = 10 nA$     |           |
|   | $BV_{GSS}$    | Gate-Source Breakdown<br>Voltage                   | -25  |      |                        | $V_{DS} = 0, I_G = -1 \mu A$     |           |
|   | $I_{DSS}$     | Saturation Drain Current<br>(Note 3)               |      | 1.2  | mA                     | $V_{DS} = 20 V, V_{GS} = 0$      |           |
|   | $I_G$         | Gate Current (Note 2)                              |      | -35  | pA                     | $V_{DG} = 20 V, I_D = 200 \mu A$ |           |
| 6<br>7<br>8<br>9<br>10<br>D<br>Y<br>N<br>A<br>M<br>I<br>C | $g_{fs}$      | Common Source Forward<br>Transconductance (Note 3) |      | 1500 | $\mu mho$              | $V_{DS} = 20 V, V_{GS} = 0$      | f = 1 kHz |
|   | $g_{os}$      | Common-Source Output<br>Conductance                |      | 2.5  |                        |                                  |           |
|   | $C_{iss}$     | Common-Source Input<br>Capacitance                 |      | 4    | pF                     |                                  | f = 1 MHz |
|   | $C_{rss}$     | Common-Source Reverse<br>Transfer Capacitance      |      | 1    |                        |                                  |           |
|   | $\bar{e}_n$   | Equivalent Short-Circuit<br>Input Noise Voltage    |      | 10   | $\frac{nV}{\sqrt{Hz}}$ | $V_{DS} = 10 V, V_{GS} = 0$      | f = 1 kHz |

**NOTES:**

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in  $T_A$ .
3. Pulse test duration = 2 ms.

NP



# n-channel JFETs designed for . . .



## ■ General Purpose Amplifiers

### Performance Curves NZF See Section 5

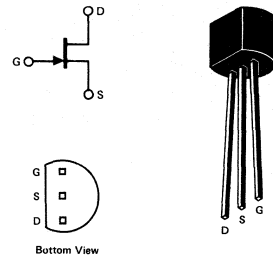
#### BENEFITS

- High Gain  
 $G_{FS} = 7000 \mu\text{mho}$  Minimum  
 (J211, J212)
- High Input Impedance  
 $I_{GSS} = 100 \text{ pA}$  Maximum  
 $C_{iss} = 5 \text{ pF}$  Typical

#### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Gate-Drain or Gate-Source Voltage                               | -25 V        |
| Gate Current  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | 360 mW       |
| Operating Temperature Range                                     | -55 to 135°C |
| Storage Temperature Range                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | 300°C        |

TO-92  
See Section 7



#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                  | J210          |       |        | J211  |        |       | J212 |        |      | Unit                                 | Test Conditions                             |
|---------------------------------|---------------|-------|--------|-------|--------|-------|------|--------|------|--------------------------------------|---|
|                                 | Min           | Typ   | Max    | Min   | Typ    | Max   | Min  | Typ    | Max  |                                      |   |
| 1 S<br>2 T<br>3 A<br>4 I<br>5 C | $I_{GSS}$     |       | -100   |       |        | -100  |      |        | -100 | pA                                   | $V_{DS} = 0, V_{GS} = -15 \text{ V}$        |
|                                 | $V_{GS(off)}$ | -1    | -3     | -2.5  | -4.5   | -4    |      |        | -6   | V                                    | $V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$ |
|                                 | $BV_{GSS}$    | -25   |        | -25   |        | -25   |      |        |      |                                      | $V_{DS} = 0, I_G = -1 \mu\text{A}$          |
|                                 | $I_{DSS}$     | 2     | 15     | 7     | 20     | 15    |      |        | 40   | mA                                   | $V_{DS} = 15 \text{ V}, V_{GS} = 0$         |
|                                 | $I_G$         |       | -10    |       | -10    |       |      |        | -10  | pA                                   | $V_{DG} = 10 \text{ V}, I_D = 1 \text{ mA}$ |
| 6                               | $g_{fs}$      | 4,000 | 12,000 | 7,000 | 12,000 | 7,000 |      | 12,000 |      | $\mu\text{mho}$                      | $V_{DS} = 15 \text{ V}, V_{GS} = 0$         |
| 7                               | $g_{os}$      |       | 150    |       | 200    |       |      | 200    |      |                                      |   |
| 8                               | $C_{iss}$     |       | 4      |       | 4      |       |      | 4      |      | pF                                   | $f = 1 \text{ MHz}$                         |
| 9                               | $C_{rss}$     |       | 1      |       | 1      |       |      | 1      |      |                                      | $f = 1 \text{ kHz}$                         |
| 10                              | $\bar{e}_n$   |       | 10     |       | 10     |       |      | 10     |      | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |   |

#### NOTES:

1. Approximately doubles for every 10°C increase in  $T_A$ .
2. Pulse test duration = 2 ms.

NZF

J210 J211 J212

4

Siliconix

# n-channel JFETs designed for . . .



**Performance Curves NS**  
 See Section 5

## ■ Audio and Sub-Audio Amplifiers

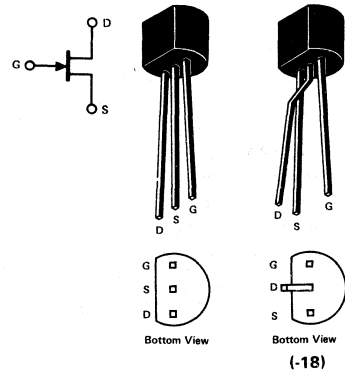
### BENEFITS

- Ultra Low Noise  
 $\bar{e}_n = 8 \text{ nV}/\sqrt{\text{Hz}}$  Typical at 10 Hz  
 $\bar{e}_n = 2 \text{ nV}/\sqrt{\text{Hz}}$  Typical at 1 kHz

### ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -40V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C). . . . . 360 mW  
 Operating Temperature Range. . . . . -55 to 135°C  
 Storage Temperature Range. . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92  
 See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  | J230  |     |       | J231  |     |       | J232  |     |       | Unit   | Test Conditions                                 |
|---|-------|-----|-------|-------|-----|-------|-------|-----|-------|--------|---|
|   | Min   | Typ | Max   | Min   | Typ | Max   | Min   | Typ | Max   |        |   |
| 1   I <sub>GSS</sub>   Gate Reverse Current (Note 2)                      |       |     | -250  |       |     | -250  |       |     | -250  | µA     | V <sub>DS</sub> = 0, V <sub>GS</sub> = -30 V    |
| 2   S   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage                 | -1    |     | -3    | -2    |     | -5    | -4    |     | -6    | V      | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 µA   |
| 3   A   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage                 | -40   |     |       | -40   |     |       | -40   |     |       |        | V <sub>DS</sub> = 0, I <sub>G</sub> = -1 µA     |
| 4   I   I <sub>DSS</sub>   Saturation Drain Current (Note 3)              | 0.7   |     | 3     | 2     |     | 6     | 5     |     | 10    | mA     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0     |
| 5   C   I <sub>G</sub>   Gate Current (Note 2)                            |       | -10 |       |       | -10 |       |       | -10 |       | µA     | V <sub>DG</sub> = 10 V, I <sub>D</sub> = 0.5 mA |
| 6   D   g <sub>fs</sub>   Common-Source Forward Transconductance (Note 3) | 1,000 |     | 2,500 | 1,500 |     | 3,000 | 2,500 |     | 4,000 | µmho   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0     |
| 7   Y   g <sub>os</sub>   Common-Source Output Conductance                |       |     | 2     |       |     | 4     |       |     | 6     |        |   |
| 8   A   C <sub>iss</sub>   Common-Source Input Capacitance                |       | 12  |       |       | 12  |       |       | 12  |       | pF     | f = 1 MHz                                       |
| 9   M   C <sub>rss</sub>   Common-Source Reverse Transfer Capacitance     |       | 2   |       |       | 2   |       |       | 2   |       |        |   |
| 10   I   $\bar{e}_n$   Equivalent Short Circuit Input Noise Voltage       |       | 8   | 30    |       | 8   | 30    |       | 8   | 30    | nV/√Hz | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0     |
| 11   C   $\bar{e}_n$   Equivalent Short Circuit Input Noise Voltage       |       | 2   |       |       | 2   |       |       | 2   |       |        | f = 10 Hz<br>f = 1 kHz                          |

**NOTES:**

1. Geometry is symmetrical. Unit may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T<sub>A</sub>.
3. Pulse test duration = 2 ms.

NS

# p-channel JFETs designed for . . .



J270 J271  
J270-18 J271-18

## ■ General Purpose Amplifiers

Performance Curves PS  
See Section 5

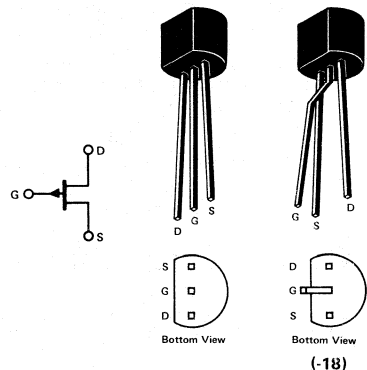
### BENEFITS

- Low Cost
- Automatic Insertion Package
- High Gain Amplifiers  
 $g_{fs} = 14,000 \mu\text{mho}$  Typical (J271)
- Low Noise  
 $e_n = 6 \text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz Typical

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Gate-Drain or Gate Source Voltage (Note 1)                      | 30 V         |
| Gate Current  | -50 mA       |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | 360 mW       |
| Operating Temperature Range                                     | -55 to 135°C |
| Storage Temperature Range                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | 300°C        |

TO-92  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic                  | J270          |       |        | J271  |     |        | Unit                                 | Test Conditions  |
|---------------------------------|---------------|-------|--------|-------|-----|--------|--------------------------------------|--|
|                                 | Min           | Typ   | Max    | Min   | Typ | Max    |                                      |  |
| 1 S<br>2 T<br>3 A<br>4 T<br>5 C | $I_{GSS}$     |       | 200    |       |     | 200    | pA                                   | $V_{DS} = 0, V_{GS} = 20 \text{ V}$                              |
|                                 | $V_{GS(off)}$ | 0.5   | 2.0    | 1.5   |     | 4.5    | V                                    | $V_{DS} = -15 \text{ V}, I_D = -1 \text{ nA}$                    |
|                                 | $BV_{GSS}$    | 30    |        | 30    |     |        |                                      | $V_{DS} = 0, I_G = 1 \mu\text{A}$                                |
|                                 | $I_{DSS}$     | -2    | -15    | -6    |     | -50    | mA                                   | $V_{DS} = -15 \text{ V}, V_{GS} = 0$                             |
|                                 | $I_G$         |       | 15     |       | 60  |        | pA                                   | $V_{DG} = -15 \text{ V}, I_D = I_{DSS(min)}$                     |
| 6<br>7<br>8<br>9<br>10          | $g_{fs}$      | 6,000 | 15,000 | 8,000 |     | 18,000 | $\mu\text{mho}$                      | $V_{DS} = -15 \text{ V}, V_{GS} = 0$                             |
|                                 | $g_{os}$      |       | 200    |       |     | 500    |                                      |  |
|                                 | $C_{iss}$     |       | 32     |       | 32  |        | pF                                   | $f = 1 \text{ MHz}$  |
|                                 | $C_{rss}$     |       | 4      |       | 4   |        |                                      |  |
|                                 | $e_n$         |       | 6      |       | 6   |        | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ | $V_{DS} = -10 \text{ V}, I_D = I_{DSS(min)}$ $f = 1 \text{ kHz}$ |

#### NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in  $T_A$ .
3. Pulse test duration = 2 ms.

PS

4

Siliconix

# n-channel JFETs designed for . . .



- VHF/UHF Amplifiers
- Oscillators
- Mixers

## Performance Curves NZF See Section 5

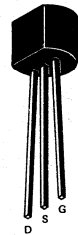
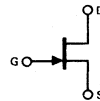
### BENEFITS

- High Power Gain  
20–23 dB Typical at 100 MHz,  
Common-Source  
17.5–20.5 dB Typical at 100 MHz,  
Common-Gate
- Low Noise Figure  
1.3 dB Typical at 100 MHz
- High Dynamic Range  
Greater than 100 dB

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Gate-Drain or Gate-Source Voltage . . . . .                               | -25 V        |
| Gate Current . . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |

TO-92  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

| Characteristic |                      | Min              | Max                  | Unit | Test Conditions  |  |
|----------------|----------------------|------------------|----------------------|------|--|--|
| 1              | S<br>T<br>A<br>T     | I <sub>GSS</sub> | Gate Reverse Current | -0.5 | nA   | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0<br>T <sub>A</sub> = 125°C |
|                |                      |                  |                      | -0.1 | μA   |  |
| 3              | BV <sub>GSS</sub>    | -25              |                      | V    | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0              |  |
| 4              | V <sub>GS(off)</sub> | -1.5             | -7.0                 |      | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA            |  |
| 5              | I <sub>DSS</sub>     | 4                | 45                   | mA   | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0              |  |
| 6              | g <sub>fs</sub>      | 4500             | 9000                 | μmho | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA, f = 1 kHz |  |
| 7              | g <sub>os</sub>      |                  | 200                  |      |  |  |
| 8              | C <sub>rss</sub>     |                  | 1.7                  | pF   | V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA, f = 1 MHz |  |
| 9              | C <sub>iss</sub>     |                  | 5.5                  |      |  |  |

NOTES:

1. I<sub>DSS</sub> and V<sub>GS(off)</sub> are selected into 5 ranges and labeled according to above table.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

NZF

# n-channel JFETs designed for . . .



J304 J305

- VHF/UHF Amplifiers
- Oscillators
- Mixers

**Performance Curves NH**  
See Section 5

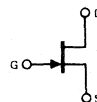
**BENEFITS**

- Characterized for Operation at 100 and 400 MHz
- Low Noise  
NF = 1.7 dB Typical at 100 MHz

TO-92  
See Section 7

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |                    |
|---|--------------------|
| Gate-Drain or Gate-Source Voltage                               | ..... -30 V        |
| Gate Current  | ..... 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | ..... 360 mW       |
| Operating Temperature Range                                     | ..... -55 to 135°C |
| Storage Temperature Range                                       | ..... -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | ..... 300°C        |



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | J304  |       |       | J305  |       |      | Unit | Test Conditions                               |             |
|--|-------|-------|-------|-------|-------|------|------|---|-------------|
|  | Min   | Typ   | Max   | Min   | Typ   | Max  |      |   |             |
| 1 <b>S</b> <b>I</b> <b>G</b> <b>S</b> Gate Reverse Current (Note 1)              |       |       | -100  |       |       | -100 | pA   | V <sub>DS</sub> = 0, V <sub>GS</sub> = -20 V  |             |
| 2 <b>V</b> <b>G</b> <b>S</b> <b>(off)</b> Gate Source Cutoff Voltage             | -2    |       | -6    | -0.5  |       | -3   | V    | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 nA |             |
| 3 <b>B</b> <b>V</b> <b>G</b> <b>S</b> Gate Source Breakdown Voltage              | -30   |       |       | -30   |       |      |      | V <sub>DS</sub> = 0, I <sub>G</sub> = -1 μA   |             |
| 4 <b>I</b> <b>D</b> <b>S</b> Saturation Drain Current (Note 2)                   | 5     |       | 15    | 1     |       | 8    | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0   |             |
| 5 <b>g</b> <b>f</b> <b>s</b> Common-Source Forward Transconductance (Note 2)     | 4,500 |       | 7,500 | 3,000 |       |      | μmho | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0   |             |
| 6 <b>g</b> <b>o</b> <b>s</b> Common-Source Output Transconductance               |       |       | 50    |       |       | 50   |      |   | f = 1 kHz   |
| 7 <b>C</b> <b>i</b> <b>s</b> <b>s</b> Common-Source Input Capacitance            |       | 3.5   |       |       | 3.5   |      | pF   | f = 1 MHz                                     |             |
| 8 <b>C</b> <b>r</b> <b>s</b> <b>s</b> Common-Source Reverse Transfer Capacitance |       | 0.85  |       |       | 0.85  |      |      |   |             |
| 9 <b>C</b> <b>o</b> <b>s</b> <b>s</b> Common-Source Output Capacitance           |       | 1.0   |       |       | 1.0   |      |      |   |             |
| 10 <b>g</b> <b>f</b> <b>s</b> Common-Source Forward Transconductance             |       |       |       |       | 3,000 |      |      | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0   |             |
| 11 <b>g</b> <b>o</b> <b>s</b> Common-Source Output Conductance                   |       | 60    |       |       | 60    |      |      |   | f = 100 MHz |
| 12 <b>b</b> <b>o</b> <b>s</b> <b>s</b> Common-Source Output Susceptance          |       | 800   |       |       | 800   |      |      |   | f = 400 MHz |
| 13 <b>g</b> <b>i</b> <b>s</b> <b>s</b> Common-Source Input Conductance           |       | 80    |       |       | 80    |      |      |   | f = 100 MHz |
| 14 <b>b</b> <b>i</b> <b>s</b> <b>s</b> Common-Source Input Susceptance           |       | 2,000 |       |       | 2,000 |      |      |   | f = 400 MHz |
| 15 <b>G</b> <b>p</b> <b>s</b> Common-Source Power Gain                           |       | 20    |       |       |       |      |      |   | f = 100 MHz |
| 16 <b>N</b> <b>F</b> Noise Figure (Single Sideband)                              |       | 1.7   |       |       |       |      |      |   | f = 400 MHz |
| 17 <b>N</b> <b>F</b> Noise Figure (Single Sideband)                              |       | 3.8   |       |       |       |      |      |   | f = 100 MHz |
| 18 <b>N</b> <b>F</b> Noise Figure (Single Sideband)                              |       | 3.8   |       |       |       |      |      |   | f = 400 MHz |
| 19 <b>N</b> <b>F</b> Noise Figure (Single Sideband)                              |       | 3.8   |       |       |       |      |      |   | f = 400 MHz |

**NOTES:**

1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse test duration = 2 ms.

NH

4

Siliconix

# n-channel JFETs designed for . . .



- VHF/UHF Amplifiers
- Oscillators
- Mixers

## Performance Curves NZA See Section 5

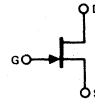
### BENEFITS

- Industry Standard Part  
In Low Cost Plastic Package
- High Power Gain  
11 dB Typical at 450 MHz  
Common-Gate
- Low Noise  
2.7 dB Typical at 450 MHz
- Wide Dynamic Range  
Greater than 100 dB
- Easily Matches to 75 Ω Input

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |                   |
|---|-------------------|
| Drain-Gate Voltage  | .....25 V         |
| Source-Gate Voltage   | .....25 V         |
| Forward Gate Current  | .....10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | .....360 mW       |
| Operating Temperature Range                                     | .....-55 to 135°C |
| Storage Temperature Range                                       | .....-55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | .....300°C        |

TO-92  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | J308  |        |        | J309   |        |        | J310  |        |        | Unit   | Test Conditions                                |           |
|--|-------|--------|--------|--------|--------|--------|-------|--------|--------|--------|--|-----------|
|  | Min   | Typ    | Max    | Min    | Typ    | Max    | Min   | Typ    | Max    |        |  |           |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage              | -25   |        |        | -25    |        |        | -25   |        |        | V      | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0    |           |
| 2 I <sub>GSS</sub> Gate Reverse Current                        |       |        | -1.0   |        |        | -1.0   |       |        | -1.0   | nA     | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0   |           |
| 3 T I <sub>GSS</sub> Gate Reverse Current                      |       |        | -1.0   |        |        | -1.0   |       |        | -1.0   | μA     | T = +125°C                                     |           |
| 4 A V <sub>GS(off)</sub> Gate-Source Cutoff Voltage            | -1.0  |        | -6.5   | -1.0   |        | -4.0   | -2.0  |        | -6.5   | V      | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA  |           |
| 5 C I <sub>DSS</sub> Saturation Drain Current (Note 1)         | 12    |        | 60     | 12     |        | 30     | 24    |        | 60     | mA     | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0    |           |
| 6 V <sub>GS(f)</sub> Gate-Source Forward Voltage               |       |        | 1.0    |        |        | 1.0    |       |        | 1.0    | V      | V <sub>DS</sub> = 0, I <sub>G</sub> = 1 mA     |           |
| 7 g <sub>fs</sub> Common-Source Forward Transconductance       | 8,000 |        | 20,000 | 10,000 |        | 20,000 | 8,000 |        | 18,000 | μmhos  | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA |           |
| 8 g <sub>os</sub> Common-Source Output Conductance             |       |        | 200    |        |        | 200    |       |        | 200    |        |  | f = 1 kHz |
| 9 Y g <sub>fs</sub> Common-Gate Forward Transconductance       |       | 13,000 |        |        | 13,000 |        |       | 12,000 |        |        |  |           |
| 10 A g <sub>og</sub> Common-Gate Output Conductance            |       | 150    |        |        | 100    |        |       | 150    |        |        |  |           |
| 11 C C <sub>gd</sub> Gate-Drain Capacitance                    |       | 1.8    | 2.5    |        | 1.8    | 2.5    |       | 1.8    | 2.5    | pF     | V <sub>DS</sub> = 0, V <sub>GS</sub> = -10 V   |           |
| 12 C <sub>gs</sub> Gate-Source Capacitance                     |       | 4.3    | 5.0    |        | 4.3    | 5.0    |       | 4.3    | 5.0    | pF     | V <sub>DS</sub> = 0, V <sub>GS</sub> = -10 V   |           |
| 13 e <sub>n</sub> Equivalent Short-Circuit Input Noise Voltage |       | 10     |        |        | 10     |        |       | 10     |        | nV/√Hz | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA |           |
| 14 Re(Y <sub>fs</sub> ) Common-Source Forward Transconductance |       | 12     |        |        | 12     |        |       | 12     |        | mmho   | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA |           |
| 15 Re(Y <sub>ig</sub> ) Common-Gate Input Conductance          |       | 14     |        |        | 14     |        |       | 14     |        |        |  |           |
| 16 H Re(Y <sub>is</sub> ) Common-Source Input Conductance      |       | 0.4    |        |        | 0.4    |        |       | 0.4    |        |        |  |           |
| 17 F Re(Y <sub>os</sub> ) Common-Source Output Conductance     |       | 0.15   |        |        | 0.15   |        |       | 0.15   |        |        |  |           |
| 18 E G <sub>pg</sub> Common-Gate Power Gain at Noise Match     |       | 16     |        |        | 16     |        |       | 16     |        | dB     | f = 105 MHz                                    |           |
| 19 NF Noise Figure   |       | 1.5    |        |        | 1.5    |        |       | 1.5    |        |        |  |           |
| 20 G <sub>pg</sub> Common-Gate Power Gain at Noise Match       |       | 11     |        |        | 11     |        |       | 11     |        |        |  |           |
| 21 NF Noise Figure   |       | 2.7    |        |        | 2.7    |        |       | 2.7    |        |        | f = 450 MHz                                    |           |

NOTE:  
1. Pulse test PW 300 μs, duty cycle ≤ 3%.

NZA

# n-channel JFETs current regulator diodes designed for . . .

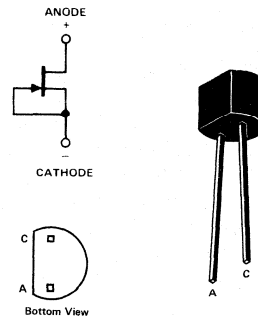
- Current Regulation
- Current Limiting
- Biasing
- Linear Ramp and Staircase Generator

**Performance Curves NCL**  
**See Section 5**

**BENEFITS**

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources  
No Power Supplies Required
- Good Operating Current Tolerance  
±20%

TO-92  
See Section 7



**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |              |
|---|--------------|
| Peak Operating Voltage  | 50 V         |
| Forward Current   | 20 mA        |
| Reverse Current   | 50 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | 360 mW       |
| Operating Temperature Range                                     | -55 to 135°C |
| Storage Temperature Range                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | 300°C        |

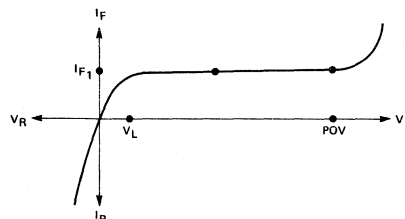
**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                  |                 |  | J500    | J501                      | J502  | J503  | J504  | J505  | Unit  | Test Conditions |  |
|---------------------------------|-----------------|--|---------|---------------------------|-------|-------|-------|-------|-------|-----------------|--|
| 1<br>S<br>T<br>A<br>T<br>I<br>C | I <sub>F1</sub> | Forward Current (Note 1)                   | Min     | 0.192                     | 0.264 | 0.344 | 0.448 | 0.600 | 0.800 | mA              | V <sub>F</sub> = 25 V                      |
|                                 |                 |  | Nominal | 0.240                     | 0.330 | 0.430 | 0.560 | 0.750 | 1.000 |                 |  |
|                                 |                 |  | Max     | 0.288                     | 0.396 | 0.516 | 0.672 | 0.900 | 1.200 |                 |  |
| 4<br>T<br>I<br>C                | POV             | Peak Operating Voltage<br>(Notes 1 and 2)  | Min     | 50                        | 50    | 50    | 50    | 50    | 50    | V               | I <sub>F</sub> = 1.1 I <sub>F1</sub> (Max) |
|                                 |                 |  | Max     | 1.2                       | 1.3   | 1.5   | 1.7   | 1.9   | 2.1   |                 |  |
|                                 |                 |  | Typ     | 0.8                       | 0.9   | 1.1   | 1.2   | 1.4   | 1.5   |                 |  |
| 5<br>D<br>Y<br>N                | Z <sub>F1</sub> | Small-Signal Dynamic<br>Impedance (Note 1) | Min     | 5.0                       | 3.0   | 2.0   | 1.4   | 1.0   | 0.6   | MΩ              | V <sub>F</sub> = 25 V, f = 1 kHz           |
|                                 |                 |  | Typ     | 8.0                       | 6.0   | 4.4   | 3.4   | 2.5   | 1.9   |                 |  |
|                                 |                 |  | CF      | Anode-Cathode Capacitance | Typ   | 2     | 2     | 2     | 2     |                 |  |

**NOTES:**

1. Pulse test duration = 2 ms.
2. Maximum V<sub>F</sub> where I<sub>F</sub> < 1.1 I<sub>F1</sub>(Max) is guaranteed.
3. Minimum V<sub>F</sub> required to insure I<sub>F</sub> > 0.9 I<sub>F1</sub>(Min).

**Current-Limiter Diode  
V-I Characteristic**



NCL

4



# n-channel JFETs current regulator diodes designed for . . .

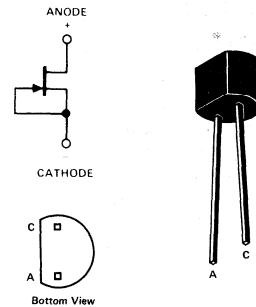
- Current Regulation
- Current Limiting
- Biasing
- Linear Ramp and Staircase Generator

## Performance Curves NCL See Section 5

### BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources  
No Power Supplies Required
- Good Operating Current Tolerance  
±20%

TO-92  
See Section 7



### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Peak Operating Voltage  | 50 V         |
| Forward Current   | 20 mA        |
| Reverse Current   | 50 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | 360 mW       |
| Operating Temperature Range                                     | -55 to 135°C |
| Storage Temperature Range                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | 300°C        |

### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

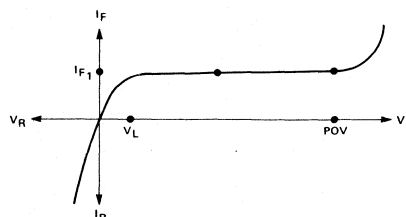
| Characteristic                            |   | J506                                     | J507  | J508  | J509 | J510 | J511 | Unit | Test Conditions   |
|---|---|--|-------|-------|------|------|------|------|---|
| 1<br>2<br>3<br>S<br>T<br>A<br>T<br>I<br>C | I <sub>F1</sub> Forward Current (Note 1)                | Min                                      | 1.120 | 1.440 | 1.9  | 2.4  | 2.9  | 3.8  | mA<br>V <sub>F</sub> = 25 V   |
|   |   | Nominal                                  | 1.400 | 1.800 | 2.4  | 3.0  | 3.6  | 4.7  |   |
|   |   | Max                                      | 1.680 | 2.160 | 2.9  | 3.6  | 4.3  | 5.6  |   |
| 4<br>5<br>6<br>P<br>O<br>V<br>V<br>L      | POV Peak Operating Voltage (Notes 1 and 2)              | Min                                      | 50    | 50    | 50   | 50   | 50   | 50   | V<br>I <sub>F</sub> = 1.1 I <sub>F1</sub> (Max)<br>I <sub>F</sub> = 0.9 I <sub>F1</sub> (Min) |
|   |   | Max                                      | 2.5   | 2.8   | 3.1  | 3.5  | 3.9  | 4.2  |   |
|   |   | Typ                                      | 1.8   | 2.0   | 2.2  | 2.5  | 2.8  | 3.0  |   |
| 7<br>8<br>9<br>D<br>Y<br>N                | Z <sub>F1</sub> Small-Signal Dynamic Impedance (Note 1) | Min                                      | 0.4   | 0.25  | 0.25 | 0.20 | 0.20 | 0.15 | MΩ<br>V <sub>F</sub> = 25 V, f = 1 kHz  |
|   |   | Typ                                      | 1.4   | 1.0   | 0.70 | 0.60 | 0.50 | 0.30 |   |
|   |   | C <sub>F</sub> Anode-Cathode Capacitance | Typ   | 2     | 2    | 2    | 2    | 2    |   |

### NOTES:

1. Pulse test duration = 2 ms.
2. Maximum V<sub>F</sub> where I<sub>F</sub> < 1.1 I<sub>F1</sub>(Max) is guaranteed.
3. Minimum V<sub>F</sub> required to insure I<sub>F</sub> > 0.9 I<sub>F1</sub>(Min).

### NCL

Current-Limiter Diode  
V-I Characteristic





# low-leakage pico-amp diodes designed for . . .

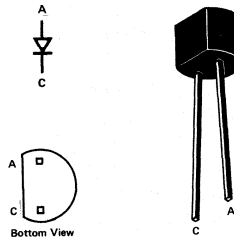
- High Impedance Diode Switching
- High Dynamic Range Log Amps
- High Isolation Protection Circuits

**BENEFITS**  
• Low Cost

TO-92  
See Section 7

### ABSOLUTE MAXIMUM RATINGS (25°C)

|  |                 |
|--|-----------------|
| Forward Current . . . . .                                      | 10 mA           |
| Total Device Dissipation . . . . .                             | 360 mW          |
| Storage Temperature Range . . . . .                            | -65°C to +135°C |
| Lead Temperature<br>(1/16" from case for 10 seconds) . . . . . | 300°C           |



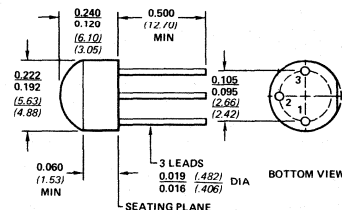
Also Available As EPAD50,  
100, 200, 500 (TO-106)

### ELECTRICAL CHARACTERISTICS (25°C)

| Characteristic             |   | Min     | Typ | Max  | Unit | Test Conditions                  |
|----------------------------|---|---------|-----|------|------|----------------------------------|
| S<br>T<br>A<br>T<br>I<br>C | I <sub>R</sub> Reverse Current (Note 1)     | JPAD50  |     | -50  | pA   | V <sub>R</sub> = -20 V           |
|                            |   | JPAD100 |     | -100 |      |                                  |
|                            |   | JPAD200 |     | -200 |      |                                  |
|                            |   | JPAD500 |     | -500 |      |                                  |
| 5                          | BV <sub>R</sub> Breakdown Voltage (Reverse) | -35     | -80 |      | V    | I <sub>R</sub> = -1 μA           |
| 6                          | V <sub>F</sub> Forward Voltage Drop         |         | 0.8 | 1.5  | V    | I <sub>F</sub> = 5 mA            |
| D<br>Y<br>N                | C <sub>R</sub> Capacitance                  |         | 1.5 | 2.0  | pF   | V <sub>R</sub> = -5 V, f = 1 MHz |

**NOTE:**

- The JPAD type number denotes its maximum reverse current value in pico amps. Devices with I<sub>R</sub> values intermediate to those shown are also available on request.



TO-106

# n-channel JFET designed for . . .



- Analog Switches
- Choppers
- Commutators

## Performance Curves NZF See Section 5

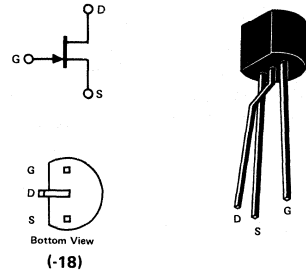
### BENEFITS

- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive  
High Isolation Resistance from Driver
- Very Fast Switching  
 $t_{D(on)} + t_r = 6 \text{ ns Typical}$
- Short Sample and Hold Aperture Time  
 $C_{gd(off)} < 2 \text{ pF}$   
 $C_{gs(off)} < 2 \text{ pF}$

### ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92 Lead-form  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

|    |  | Characteristic                              | K114 |     |     | Unit     | Test Conditions   |
|----|--|---|------|-----|-----|----------|---|
|    |  |   | Min  | Typ | Max |          |   |
| 1  | S<br>T<br>A  | $I_{GSS}$ Gate Reverse Current (Note 1)     |      |     | -1  | nA       | $V_{DS} = 0, V_{GS} = -15 \text{ V}$  |
| 2  |  | $V_{GS(off)}$ Gate-Source Cutoff Voltage    | -3   |     | -10 | V        | $V_{DS} = 5 \text{ V}, I_D = 1 \mu\text{A}$   |
| 3  |  | $BV_{GSS}$ Gate-Source Breakdown Voltage    | -25  |     |     |          | $V_{DS} = 0, I_G = -1 \mu\text{A}$  |
| 4  | T<br>I<br>C  | $I_{DSS}$ Saturation Drain Current (Note 2) | 15   |     |     | mA       | $V_{DS} = 15 \text{ V}, V_{GS} = 0$   |
| 5  |  | $I_{D(off)}$ Drain Cutoff Current (Note 1)  |      |     | 1   | nA       | $V_{DS} = 5 \text{ V}, V_{GS} = -10 \text{ V}$  |
| 6  |  | $r_{DS(on)}$ Drain-Source ON Resistance     |      |     | 150 | $\Omega$ | $V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0$   |
| 7  |  | $C_{dg(off)}$ Drain-Gate OFF Capacitance    |      |     | 2   | pF       | $V_{DS} = 0, V_{GS} = -10 \text{ V}$<br><br>$V_{DS} = V_{GS} = 0$   |
| 8  | $C_{sg(off)}$ Source-Gate OFF Capacitance                            |   |      | 2   |     |          |   |
| 9  | $C_{dg(on)} + C_{sg(on)}$ Drain-Gate Plus Source-Gate ON Capacitance |   |      | 8   |     |          |   |
| 10 | M<br>I<br>C  | $t_{d(on)}$ Turn On Delay Time              |      | 3   |     | ns       | Switching Time Test Conditions<br>$V_{DD} = 10 \text{ V}, V_{GS(off)} = -12 \text{ V}$<br>$R_L = 1 \text{ K}\Omega, V_{GS(on)} = 0$ |
| 11 |  | $t_r$ Rise Time                             |      | 3   |     |          |   |
| 12 |  | $t_{d(off)}$ Turn Off Delay Time            |      | 12  |     |          |   |
| 13 |  | $t_f$ Fall Time                             |      | 8   |     |          |   |

NOTES:

1. Approximately doubles for every 10°C increase in  $T_A$ .
2. Pulse test duration = 300  $\mu\text{s}$ ; duty cycle  $\leq 3\%$ .

NZF

# n-channel JFET designed for . . .



K1837-18

- VHF/UHF Amplifiers
- Mixers
- Oscillators

**Performance Curves NH**  
See Section 5

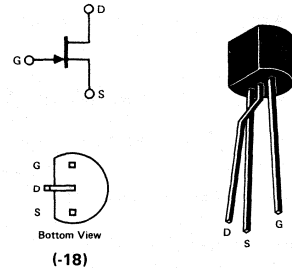
**BENEFITS**

- Specified for 200 MHz Operation

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |              |
|---|--------------|
| Drain-Gate Voltage . . . . .  | 25 V         |
| Source-Gate Voltage . . . . .   | 25 V         |
| Drain-Source Voltage . . . . .  | 25 V         |
| Forward Gate Current . . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |

TO-92  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic |                                 | Min                           | Max  | Unit  | Test Conditions |   |                        |             |
|----------------|---------------------------------|-------------------------------|--|-------|-----------------|---|------------------------|-------------|
| 1              | S<br>I <sub>GSS</sub>           | Gate Reverse Current          |  | -250  | pA              | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0                                  | T <sub>A</sub> = +85°C |             |
|                |                                 |                               |  |       | -15             |   |                        | nA          |
|                |                                 |                               |  |       |                 |   |                        |             |
| 3              | T<br>BV <sub>GSS</sub>          | Gate-Source Breakdown Voltage | -30  |       | V               | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0                                   |                        |             |
|                |                                 |                               |  |       |                 |   |                        |             |
| 4              | I<br>V <sub>GS(off)</sub>       | Gate-Source Cutoff Voltage    | -0.5                                       | -8.0  |                 | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 μA                                 |                        |             |
| 5              | D<br>I <sub>DSS</sub>           | Saturation Drain Current      | 4.0  | 25    | mA              | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 1)                          |                        |             |
| 6              | A<br>r <sub>DS(on)</sub>        | Drain-Source ON Resistance    |  | 300   | Ω               | I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0                                    |                        |             |
| 7              | D<br>Y<br>N<br>A<br>M<br>I<br>C | g <sub>fs</sub>               | Common-Source Forward Transconductance     | 4,500 | 10,000          | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0                                   | f = 1 kHz              |             |
| 8              |                                 | Re(y <sub>fs</sub> )          | Common-Source Forward Transconductance     | 4,000 |                 |   | μmhos                  | f = 200 MHz |
| 9              |                                 | Re(y <sub>os</sub> )          | Common-Source Output Conductance           |       | 150             |   |                        |             |
| 10             |                                 | Re(y <sub>is</sub> )          | Common-Source Input Conductance            |       | 800             |   |                        |             |
| 11             |                                 | C <sub>iss</sub>              | Common-Source Input Capacitance            |       | 6.0             |   | pF                     | f = 1 MHz   |
| 12             |                                 | C <sub>rss</sub>              | Common-Source Reverse Transfer Capacitance |       | 2.0             |   |                        |             |
| 13             | M<br>I<br>C                     | NF                            | Noise Figure                               |       | dB              | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1K Ω            | f = 200 MHz            |             |
| 14             |                                 |                               |  |       |                 | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1M Ω, BW = 5 Hz | f = 10 Hz              |             |
| 15             |                                 |                               |  |       |                 | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0                                   | f = 200 MHz            |             |

**NOTE:**

1. Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH

4

Siliconix

# n-channel JFETs designed for . . .



## ■ General Purpose Amplifiers

**Performance Curves NZF**  
See Section 5

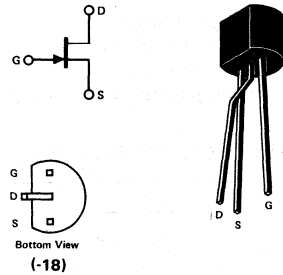
**BENEFITS**

- High Gain  
 $G_{FS} = 7000 \mu\text{mho}$  Minimum  
(K211-18, K212-18)
- High Input Impedance  
 $I_{GSS} = 100 \text{ pA}$  Maximum  
 $C_{iss} = 5 \text{ pF}$  Typical

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -25V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92 Lead-form  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic  | J210  |     |        | J211  |     |        | J212  |     |        | Unit                          | Test Conditions                             |
|---|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------------------------------|---|
|   | Min   | Typ | Max    | Min   | Typ | Max    | Min   | Typ | Max    |                               |   |
| 1 S $I_{GSS}$ Gate Reverse Current (Note 1)                   |       |     | -100   |       |     | -100   |       |     | -100   | pA                            | $V_{DS} = 0, V_{GS} = -15 \text{ V}$        |
| 2 T $V_{GS(off)}$ Gate-Source Cutoff Voltage                  | -1    |     | -3     | -2.5  |     | -4.5   | -4    |     | -6     | V                             | $V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$ |
| 3 A $BV_{GSS}$ Gate-Source Breakdown Voltage                  | -25   |     | -25    |       |     | -25    |       |     | -25    | V                             | $V_{DS} = 0, I_G = -1 \mu\text{A}$          |
| 4 I $I_{DSS}$ Saturation Drain Current (Note 2)               | 2     |     | 15     | 7     |     | 20     | 15    |     | 40     | mA                            | $V_{DS} = 15 \text{ V}, V_{GS} = 0$         |
| 5 C $I_G$ Gate Current (Note 1)                               |       | -10 |        |       | -10 |        |       | -10 |        | pA                            | $V_{DG} = 10 \text{ V}, I_D = 1 \text{ mA}$ |
| 6 $g_{fs}$ Common-Source Forward Transconductance (Note 2)    | 4,000 |     | 12,000 | 7,000 |     | 12,000 | 7,000 |     | 12,000 | $\mu\text{mho}$               | $V_{DS} = 15 \text{ V}, V_{GS} = 0$         |
| 7 D $g_{os}$ Common-Source Output Conductance                 |       |     | 150    |       |     | 200    |       |     | 200    |                               |   |
| 8 A $C_{iss}$ Common-Source Input Capacitance                 |       | 4   |        |       | 4   |        |       | 4   |        | pF                            | f = 1 MHz                                   |
| 9 I $C_{rss}$ Common-Source Reverse Transfer Capacitance      |       | 1   |        |       | 1   |        |       | 1   |        | pF                            | f = 1 MHz                                   |
| 10 C $\bar{e}_n$ Equivalent Short-Circuit Input Noise Voltage |       | 10  |        |       | 10  |        |       | 10  |        | $\frac{nV}{\sqrt{\text{Hz}}}$ | f = 1 kHz                                   |

**NOTES:**

1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse test duration = 2 ms.

NZF

# n-channel JFET designed for . . .



K300-18

- VHF/UHF Amplifiers
- Oscillators
- Mixers

## Performance Curves NZF See Section 5

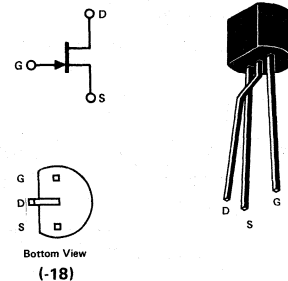
### BENEFITS

- High Power Gain  
22 dB Typical at 100 MHz  
Common-Source  
17 dB Typical at 100 MHz  
Common-Gate
- Low Noise  
NF = 2 dB Typical at 100 MHz
- High Dynamic Range Greater than 100 dB

TO-92 Lead-form  
See Section 7

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |       |              |
|---|-------|--------------|
| Gate-Drain or Gate-Source Voltage                               | ..... | -25V         |
| Gate Current (FWD)  | ..... | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | ..... | 360 mW       |
| Operating Temperature Range                                     | ..... | -55 to 135°C |
| Storage Temperature Range                                       | ..... | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | ..... | 300°C        |



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic |   | Min   | Typ   | Max   | Unit | Test Conditions                    |                      |
|----------------|---|-------|-------|-------|------|------------------------------------|----------------------|
| 1              | S   IGSS Gate Reverse Current (Note 1)              |       |       | -500  | pA   | VGS = -15 V, VDS = 0               |                      |
| 2              | T   VGS(off) Gate-Source Cutoff Voltage             | -1    |       | -6    | V    | VDS = 10 V, ID = 1 nA              |                      |
| 3              | A   BVGSS Gate-Source Breakdown Voltage             | -25   |       |       |      | VDS = 0, IG = -1 μA                |                      |
| 4              | I   IDSS Saturation Drain Current (Note 2)          | 6     |       | 30    | mA   | VDS = 10 V, VGS = 0                |                      |
| 5              | C   VGS(f) Gate-Source Forward Voltage              |       |       | 1     | V    | IG = 1 mA, VDS = 0                 |                      |
| 6              | gfs Common-Source Forward Transconductance (Note 2) | 4,500 |       | 9,000 | μmho | VDG = 10 V, ID = 5 mA<br>f = 1 kHz |                      |
| 7              | D   gos Common-Source Output Transconductance       |       |       | 200   |      |                                    |                      |
| 8              | Y   Ciss Common-Source Input Capacitance            |       | 4     | 5.5   | pF   | VDG = 10 V, ID = 5 mA<br>f = 1 MHz |                      |
| 9              | N   Crss Common-Source Reverse Transfer Capacitance |       | 1     | 1.7   |      |                                    |                      |
| 10             | C   Coss Common-Source Output Capacitance           |       | 1.5   |       |      |                                    |                      |
| 11             | H    yfs  Common-Source Forward Transadmittance     |       | 6,200 |       | μmho | VDG = 15 V, ID = 5 mA              | f = 100 MHz          |
| 12             |   |       | 6,000 |       |      |                                    | f = 450 MHz          |
| 13             | F    yfg  Common-Gate Forward Transadmittance       |       | 6,000 |       | μmho |                                    | f = 100 MHz          |
| 14             |   |       | 5,500 |       |      |                                    | f = 450 MHz          |
| 15             | E   Gfg Common-Gate Power Gain                      |       | 17    |       | dB   |                                    | f = 100 MHz (Note 3) |
| 16             | Q   NF Noise Figure (Single Sideband)               |       | 2     |       |      |                                    |                      |

#### NOTES:

1. Approximately doubles for every 10°C increase in TA.
2. Pulse test duration = 2 ms.
3. Typical values for performance at 100 MHz in a common-gate circuit operating 3 dB bandwidth is 2 MHz.

NZF

4

Siliconix

K304-18 K305-18

# n-channel JFETs designed for . . .



**Performance Curves NH**  
See Section 5

- VHF/UHF Amplifiers
- Oscillators
- Mixers

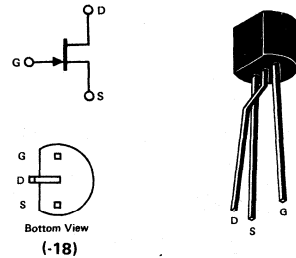
**BENEFITS**

- Characterized for Operation at 100 and 400 MHz
- Low Noise  
NF = 1.7 dB Typical at 100 MHz

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -30V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92 Lead-form  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic   | K304-18 |       |       | K305-18 |       |      | Unit   | Test Conditions                               |           |
|--|---------|-------|-------|---------|-------|------|--|---|-----------|
|  | Min     | Typ   | Max   | Min     | Typ   | Max  |  |   |           |
| 1 <b>S</b> IGSS Gate Reverse Current (Note 1)                  |         |       | -100  |         |       | -100 | pA   | V <sub>DS</sub> = 0, V <sub>GS</sub> = -20 V  |           |
| 2 <b>T</b> VGS(off) Gate Source Cutoff Voltage                 | -2      |       | -6    | -0.5    |       | -3   | V  | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 nA |           |
| 3 <b>A</b> BVGSS Gate Source Breakdown Voltage                 | -30     |       |       | -30     |       |      |  | V <sub>DS</sub> = 0, I <sub>G</sub> = -1 μA   |           |
| 4 <b>C</b> IDSS Saturation Drain Current (Note 2)              | 5       |       | 15    | 1       |       | 8    | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0   |           |
| 5 <b>D</b> gfs Common-Source Forward Transconductance (Note 2) | 4,500   |       | 7,500 | 3,000   |       |      | μmho   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0   |           |
| 6 <b>N</b> gos Common-Source Output Transconductance           |         |       | 50    |         |       | 50   |  |   | f = 1 kHz |
| 7 <b>A</b> Ciss Common-Source Input Capacitance                |         | 3.5   |       |         | 3.5   |      |  |   | f = 1 MHz |
| 8 <b>M</b> Crss Common-Source Reverse Transfer Capacitance     |         | 0.85  |       |         | 0.85  |      | pF   |   |           |
| 9 <b>I</b> Coss Common-Source Output Capacitance               |         | 1.0   |       |         | 1.0   |      |  |   |           |
| 10 <b>H</b> gfs Common-Source Forward Transconductance         |         |       |       |         | 3,000 |      | μmho   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0   |           |
| 11 <b>F</b> gos Common-Source Output Conductance               |         | 4,200 |       |         |       |      |  | f = 100 MHz                                   |           |
| 12 <b>R</b> goss Common-Source Output Conductance              |         | 60    |       |         | 60    |      |  | f = 400 MHz                                   |           |
| 13 <b>E</b> boss Common-Source Output Susceptance              |         | 80    |       |         |       |      |  | f = 100 MHz                                   |           |
| 14 <b>N</b> boss Common-Source Output Susceptance              |         | 800   |       |         | 800   |      |  | f = 400 MHz                                   |           |
| 15 <b>F</b> giss Common-Source Input Conductance               |         | 3,600 |       |         |       |      |  | f = 100 MHz                                   |           |
| 16 <b>R</b> giss Common-Source Input Conductance               |         | 80    |       |         | 80    |      |  | f = 400 MHz                                   |           |
| 17 <b>E</b> biss Common-Source Input Susceptance               |         | 800   |       |         |       |      |  | f = 100 MHz                                   |           |
| 18 <b>N</b> biss Common-Source Input Susceptance               |         | 2,000 |       |         | 2,000 |      |  | f = 400 MHz                                   |           |
| 19 <b>F</b> biss Common-Source Input Susceptance               |         | 7,500 |       |         |       |      |  | f = 100 MHz                                   |           |
| 20 <b>R</b> Gps Common-Source Power Gain                       |         | 20    |       |         |       |      |  | f = 400 MHz                                   |           |
| 21 <b>E</b> Gps Common-Source Power Gain                       |         | 11    |       |         |       |      |  | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA |           |
| 22 <b>N</b> NF Noise Figure (Single Sideband)                  |         | 1.7   |       |         |       |      | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA, R <sub>G</sub> = 1 KΩ |   |           |
| 23 <b>F</b> NF Noise Figure (Single Sideband)                  |         | 3.8   |       |         |       |      | f = 100 MHz  |   |           |
|  |         |       |       |         |       |      | f = 400 MHz  |   |           |

**NOTES:**

1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse test duration = 2 ms.

NH

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# n-channel JFETs designed for . . .



- VHF/UHF Amplifiers
- Oscillators
- Mixers

### \* ABSOLUTE MAXIMUM RATINGS (25°C)

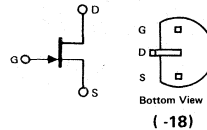
|   |              |
|---|--------------|
| Drain-Gate Voltage  | 25 V         |
| Source-Gate Voltage   | 25 V         |
| Forward Gate Current  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | 360 mW       |
| Operating Temperature Range                                     | -55 to 135°C |
| Storage Temperature Range                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | 300°C        |

### Performance Curves NZA See Section 5

#### BENEFITS

- Industry Standard Part  
In Low Cost Plastic Package
- High Power Gain  
11 dB Typical at 450 MHz  
Common-Gate
- Low Noise  
2.7 dB Typical at 450 MHz
- Wide Dynamic Range  
Greater than 100 dB
- Easily Matches to 75 Ω Input

TO-92 Lead-form  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  | K308   |      |        | K309   |      |        | K310   |      |        | Unit   | Test Conditions                                |
|---|--------|------|--------|--------|------|--------|--------|------|--------|--------|--|
|   | Min    | Typ  | Max    | Min    | Typ  | Max    | Min    | Typ  | Max    |        |  |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage                           | -25    |      |        | -25    |      |        | -25    |      |        | V      | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0    |
| 2 I <sub>GSS</sub> Gate Reverse Current                                     |        |      | -1.0   |        |      | -1.0   |        |      | -1.0   | nA     | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0   |
| 3 V <sub>GS(off)</sub> Gate-Source Cutoff Voltage                           | -1.0   |      | -6.5   | -1.0   |      | -4.0   | -2.0   |      | -6.5   | V      | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA  |
| 4 I <sub>DSS</sub> Saturation Drain Current (Note 1)                        | 12     |      | 60     | 12     |      | 30     | 24     |      | 60     | mA     | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0    |
| 5 V <sub>GS(f)</sub> Gate-Source Forward Voltage                            |        |      | 1.0    |        |      | 1.0    |        |      | 1.0    | V      | V <sub>DS</sub> = 0, I <sub>G</sub> = 1 mA     |
| 6 g <sub>fs</sub> Common-Source Forward Transconductance                    | 8,000  |      | 20,000 | 10,000 |      | 20,000 | 8,000  |      | 18,000 | μmhos  | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA |
| 7 g <sub>os</sub> Common-Source Output Conductance                          |        |      | 200    |        |      | 200    |        |      | 200    |        |  |
| 8 g <sub>fg</sub> Common-Gate Forward Transconductance                      | 13,000 |      |        | 13,000 |      |        | 12,000 |      |        |        |  |
| 9 g <sub>og</sub> Common-Gate Output Conductance                            |        | 150  |        |        | 100  |        |        | 150  |        |        |  |
| 10 C <sub>gd</sub> Gate-Drain Capacitance                                   |        | 1.8  | 2.5    |        | 1.8  | 2.5    |        | 1.8  | 2.5    | pF     | V <sub>DS</sub> = 0, V <sub>GS</sub> = -10 V   |
| 11 C <sub>gs</sub> Gate-Source Capacitance                                  |        | 4.3  | 5.0    |        | 4.3  | 5.0    |        | 4.3  | 5.0    |        |  |
| 12 e <sub>n</sub> Equivalent Short-Circuit Input Noise Voltage              |        | 10   |        |        | 10   |        |        | 10   |        | nV/√Hz | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA |
| 13 R <sub>e</sub> (v <sub>fs</sub> ) Common-Source Forward Transconductance |        | 12   |        |        | 12   |        |        | 12   |        |        |  |
| 14 R <sub>e</sub> (v <sub>ig</sub> ) Common-Gate Input Conductance          |        | 14   |        |        | 14   |        |        | 14   |        | mmho   | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA |
| 15 R <sub>e</sub> (v <sub>is</sub> ) Common-Source Input Conductance        |        | 0.4  |        |        | 0.4  |        |        | 0.4  |        |        |  |
| 16 R <sub>e</sub> (v <sub>os</sub> ) Common-Source Output Conductance       |        | 0.15 |        |        | 0.15 |        |        | 0.15 |        |        |  |
| 17 G <sub>pg</sub> Common-Gate Power Gain at Noise Match                    |        | 16   |        |        | 16   |        |        | 16   |        |        |  |
| 18 NF Noise Figure  |        | 1.5  |        |        | 1.5  |        |        | 1.5  |        | dB     | f = 105 MHz                                    |
| 19 G <sub>pg</sub> Common-Gate Power Gain at Noise Match                    |        | 11   |        |        | 11   |        |        | 11   |        |        | f = 450 MHz                                    |
| 20 NF Noise Figure  |        | 2.7  |        |        | 2.7  |        |        | 2.7  |        |        |  |

**NOTE:**

1. Pulse test PW 300 μs, duty cycle ≤ 3%.

**NZA**

K308-18 K309-18 K310-18

4

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# n-channel JFET designed for . . .



**Performance Curves NH**  
See Section 5

- VHF Amplifiers
- Mixers

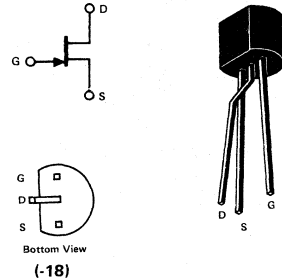
**BENEFITS**

- Low Noise  
NF = 3 dB Typical at 400 MHz
- Wide Bandwidth
- Low Cost

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -30V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92 Lead-form  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

|                            |          | Characteristic           |   | Min     | Max  | Unit      | Test Conditions              |                             |                             |
|----------------------------|----------|--------------------------|---|---------|------|-----------|------------------------------|-----------------------------|-----------------------------|
| S<br>T<br>A                | 1        | $I_{GSS}$                | Gate Reverse Current                            |         | -1.0 | nA        | $V_{GS} = -15 V, V_{DS} = 0$ |                             |                             |
|                            | 2        | $BV_{GSS}$               | Gate-Source Breakdown Voltage                   | -30     |      | V         | $I_G = -1 \mu A, V_{DS} = 0$ |                             |                             |
|                            | 3        | $V_{GS(off)}$            | Gate-Source Cutoff Voltage                      |         | -6   |           | $V_{DS} = 15 V, I_D = 1 nA$  |                             |                             |
|                            | 4        | $I_{DSS}$                | Saturation Drain Current (Note 1)               | 5       | 15   | mA        |                              |                             |                             |
| D<br>Y<br>N                | 5        | $g_{fs}$                 | Common-Source Forward Transconductance (Note 1) | 4500    | 7500 | $\mu mho$ | $V_{DS} = 15 V, V_{GS} = 0$  | f = 1 kHz                   |                             |
|                            | 6        | $g_{os}$                 | Common-Source Output Conductance                |         | 50   |           |                              |                             |                             |
|                            | 7        | $C_{rss}$                | Common-Source Reverse Transfer Capacitance      |         | 1.0  | pF        |                              | f = 1 MHz                   |                             |
|                            | 8        | $C_{iss}$                | Common-Source Input Capacitance                 |         | 4    |           |                              |                             |                             |
|                            | 9        | $C_{oss}$                | Common-Source Output Capacitance                |         | 2    |           |                              |                             |                             |
|                            |          | Characteristic           |   | 100 MHz |      | 400 MHz   |                              | Unit                        | Test Conditions             |
|                            |          |                          |   | Min     | Max  | Min       | Max                          |                             |                             |
| H<br>I<br>F<br>R<br>E<br>Q | 10       | $g_{iss}$                | Common-Source Input Conductance                 |         | 100  |           | 1000                         | $\mu mho$                   | $V_{DS} = 15 V, V_{GS} = 0$ |
|                            | 11       | $b_{iss}$                | Common-Source Input Susceptance                 |         | 2500 |           | 10,000                       |                             |                             |
|                            | 12       | $g_{oss}$                | Common-Source Output Conductance                |         | 75   |           | 100                          |                             |                             |
|                            | 13       | $b_{oss}$                | Common-Source Output Susceptance                |         | 1000 |           | 4000                         |                             |                             |
|                            | 14       | $g_{fs}$                 | Common-Source Forward Transconductance (Note 1) |         |      | 4000      |                              |                             |                             |
| 15                         | $G_{ps}$ | Common-Source Power Gain | 18  |         | 10   |           | dB                           | $V_{DS} = 15 V, I_D = 5 mA$ |                             |
| 16                         | NF       | Noise Figure             |   | 2       |      | 4         |                              |                             | $R_G = 1K \Omega$           |

**NOTE:**  
1. Pulse test duration = 300  $\mu s$ .

NH



# n-channel JFET designed for . . .



MPF102

- VHF/UHF Amplifiers
- Mixers
- Oscillators

**Performance Curves NH**  
See Section 5

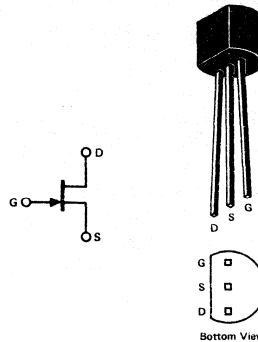
**BENEFITS**

- Low Cost
- Automatic Insertion Package

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |              |
|---|--------------|
| Drain-Gate Voltage  | 25 V         |
| Source-Gate Voltage   | 25 V         |
| Drain-Source Voltage  | 25 V         |
| Forward Gate Current  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | 360 mW       |
| Operating Temperature Range                                     | -55 to 135°C |
| Storage Temperature Range                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | 300°C        |

TO-92  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                                  |  | Min  | Max  | Unit   | Test Conditions   |             |
|---|--|------|------|--|---|-------------|
| S<br>T<br>A<br>T<br>I<br>C                      | 1   I <sub>GSS</sub>   Gate Reverse Current                        |      | -2.0 | nA   | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0<br>T <sub>A</sub> = +100°C |             |
|   | 2  |      | -2.0 | μA   |   |             |
|   | 3   BV <sub>GSS</sub>   Gate-Source Breakdown Voltage              | -25  |      | V  | I <sub>G</sub> = -10 μA, V <sub>DS</sub> = 0                            |             |
|   | 4   V <sub>GS(off)</sub>   Gate-Source Cutoff Voltage              |      | -8.0 |  |   |             |
| 5   I <sub>DSS</sub>   Saturation Drain Current | 2.0  | 20   | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 1) |   |             |
| 6   V <sub>GS</sub>   Gate-Source Voltage       | -0.5   | -7.5 | V    | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 200 μA      |   |             |
| D<br>Y<br>N<br>A<br>M<br>I<br>C                 | 7   g <sub>fs</sub>   Common-Source Forward Transconductance       | 2000 | 7500 | μmhos  | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0                             | f = 1 kHz   |
|   | 8   Re(y <sub>fs</sub> )   Common-Source Forward Transconductance  | 1600 |      |  |   | f = 100 MHz |
|   | 9   Re(y <sub>os</sub> )   Common-Source Output Conductance        |      | 200  |  |   |             |
|   | 10   Re(y <sub>is</sub> )   Common-Source Input Conductance        |      | 800  |  |   |             |
|   | 11   C <sub>iss</sub>   Common-Source Input Capacitance            |      | 7.0  | pF   |   | f = 1 MHz   |
|   | 12   C <sub>rss</sub>   Common-Source Reverse Transfer Capacitance |      | 3.0  |  |   |             |

**NOTE:**

1. Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH

4

Siliconix

# n-channel JFET designed for . . .



## Performance Curves NH See Section 5

- VHF/UHF Amplifiers
- Mixers
- Oscillators

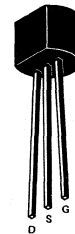
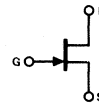
### BENEFITS

- Low Cost
- Automatic Insertion Package

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |       |              |
|---|-------|--------------|
| Drain-Gate Voltage  | ..... | 25 V         |
| Source-Gate Voltage   | ..... | 25 V         |
| Drain-Source Voltage  | ..... | 25 V         |
| Forward Gate Current  | ..... | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | ..... | 360 mW       |
| Operating Temperature Range                                     | ..... | -55 to 135°C |
| Storage Temperature Range                                       | ..... | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | ..... | 300°C        |

TO-92  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  |   | Min  | Max  | Unit       | Test Conditions                              |                      |
|---|---|------|------|------------|--|----------------------|
| 1<br>2<br>3<br>4<br>5<br>S<br>T<br>A<br>T<br>I<br>C                   | $I_{GSS}$ Gate Reverse Current                      |      | -1.0 | nA         | $V_{GS} = -15 V, V_{DS} = 0$                 | $T_A = +100^\circ C$ |
|   |   |      | -1.0 | $\mu A$    |  |                      |
|   | $BV_{GSS}$ Gate-Source Breakdown Voltage            | -25  |      | V          | $I_G = -10 \mu A, V_{DS} = 0$                |                      |
|   | $V_{GS(off)}$ Gate-Source Cutoff Voltage            | -0.5 | -8.0 |            | $V_{DS} = 15 V, I_D = 10 \mu A$              |                      |
|   | $I_{DSS}$ Saturation Drain Current                  | 1.5  | 24   | mA         | $V_{DS} = 15 V, V_{GS} = 0$ (Note 1)         |                      |
| 6<br>7<br>8<br>9<br>10<br>11<br>12<br>D<br>Y<br>N<br>A<br>M<br>I<br>C | $g_{fs}$ Common-Source Forward Transconductance     | 2000 | 7500 | $\mu mhos$ | $V_{DS} = 15 V, V_{GS} = 0$                  | f = 1 kHz            |
|   | $g_{os}$ Common-Source Output Conductance           |      | 75   |            |  |                      |
|   | $Re(y_{fs})$ Common-Source Forward Transconductance | 1600 |      |            |  |                      |
|   | $Re(y_{os})$ Common-Source Output Conductance       |      | 200  |            |  | f = 100 MHz          |
|   | $Re(y_{is})$ Common-Source Input Conductance        |      | 800  |            |  | f = 1 MHz            |
|   | $C_{iss}$ Common-Source Input Capacitance           |      | 6.5  | pF         |  |                      |
| $C_{rss}$ Common-Source Reverse Transfer Capacitance                  |   | 2.5  |      |            |  |                      |
| 13<br>14  | NF Noise Figure                                     |      | 2.5  | dB         | $V_{DS} = 15 V, V_{GS} = 0, R_G = 1M \Omega$ | f = 1 kHz            |
|   |   |      | 3.0  |            | $V_{DS} = 15 V, V_{GS} = 0, R_G = 1K \Omega$ | f = 100 MHz          |

NOTE:

1. Pulse test, pulse width = 300  $\mu s$ , duty cycle  $\leq$  3%.

NH



# n-channel JFET designed for . . .

- General Purpose Amplifiers
- Analog Switches

**Performance Curves NRL  
See Section 5**

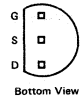
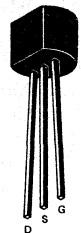
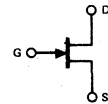
**BENEFITS**

- Low Cost
- Automatic Insertion Package

TO-92  
See Section 7

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |              |
|---|--------------|
| Drain-Gate Voltage . . . . .  | 25 V         |
| Source-Gate Voltage . . . . .   | 25 V         |
| Drain-Source Voltage . . . . .  | 25 V         |
| Forward Gate Current . . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic  |  | Min  | Typ   | Max  | Unit | Test Conditions  |           |
|---|--|------|-------|------|------|--|-----------|
| S<br>T<br>A<br>T<br>I<br>C                                  | I <sub>GSS</sub> Gate Reverse Current                  |      | -0.01 | -1.0 | nA   | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0                       |           |
|   | BV <sub>GSS</sub> Gate-Source Breakdown Voltage        | -25  | -60   |      | V    | I <sub>G</sub> = -10 μA, V <sub>DS</sub> = 0                       |           |
|   | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage        | -0.2 |       | -8.0 |      | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 μA                     |           |
|   | I <sub>DSS</sub> Saturation Drain Current              | 0.5  |       | 24   | mA   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 1)               |           |
| D<br>Y<br>N<br>A<br>M<br>I<br>C                             | g <sub>fs</sub> Common-Source Forward Transconductance | 800  |       | 6000 | μmho | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0                        | f = 1 kHz |
|   | g <sub>os</sub> Common-Source Output Conductance       |      | 10    | 75   |      |  |           |
|   | C <sub>iss</sub> Common-Source Input Capacitance       |      | 4.5   | 7.0  | pF   |  | f = 1 MHz |
| C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |  | 1.0  | 3.0   |      |      |  |           |
| NF  | Noise Figure   |      | 0.04  | 2.5  | dB   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1M Ω | f = 1 kHz |

**NOTE:**

1. Pulse test PW < 630 ms, duty cycle < 10%.

NRL

4

# n-channel JFET designed for . . .



Performance Curves NRL  
See Section 5

- General Purpose Amplifiers
- Analog Switches

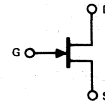
**BENEFITS**

- Low Cost
- Automatic Insertion Package

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|  |              |
|--|--------------|
| Drain-Gate Voltage . . . . .   | 20V          |
| Source-Gate Voltage . . . . .  | 20V          |
| Drain-Source Voltage. . . . .  | 20V          |
| Forward Gate Current. . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C). . . . . | 360 mW       |
| Operating Temperature Range. . . . .                                     | -55 to 135°C |
| Storage Temperature Range. . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .     | 300°C        |

TO-92  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic |                                  | Min           | Typ  | Max  | Unit | Test Conditions |                 |  |           |
|----------------|----------------------------------|---------------|--|------|------|-----------------|-----------------|--|-----------|
| 1              | ST<br>A<br>T<br>I<br>C<br>I<br>C | $I_{GSS}$     | Gate-Reverse Current                       |      | -0.1 | -100            | nA              | $V_{GS} = -10\text{ V}, V_{DS} = 0$                |           |
| 2              |                                  | $BV_{GSS}$    | Gate-Source Breakdown Voltage              | -20  |      |                 | V               | $I_G = -10\text{ }\mu\text{A}, V_{DS} = 0$         |           |
| 3              |                                  | $V_{GS(off)}$ | Gate-Source Cutoff Voltage                 | -0.5 |      | -10.0           |                 | $V_{DS} = 10\text{ V}, I_D = 1\text{ }\mu\text{A}$ |           |
| 4              |                                  | $I_{DSS}$     | Saturation Drain Current                   | 0.5  |      | 20              | mA              | $V_{DS} = 10\text{ V}, V_{GS} = 0$ (Note 1)        |           |
| 5              | D<br>Y<br>N<br>A<br>M<br>I<br>C  | $g_{fs}$      | Common-Source Forward Transconductance     | 500  |      |                 | $\mu\text{mho}$ | $V_{DS} = 10\text{ V}, V_{GS} = 0$                 | f = 1 kHz |
| 6              |                                  | $g_{os}$      | Common-Source Output Conductance           |      |      | 10              |                 |  |           |
| 7              |                                  | $C_{iss}$     | Common-Source Input Capacitance            |      |      | 4.5             | pF              | $V_{DS} = 10\text{ V}, V_{GS} = 0$                 | f = 1 MHz |
| 8              |                                  | $C_{rss}$     | Common-Source Reverse Transfer Capacitance |      |      | 1.0             |                 |  |           |

NRL

**NOTE:**

1. Pulse test PW  $\leq$  630 msec, duty cycle  $\leq$  10%.

# n-channel JFET designed for . . .



Performance Curves NH  
See Section 5

- VHF/UHF Amplifiers
- Mixers
- Oscillators

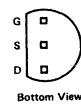
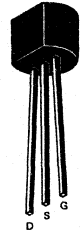
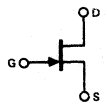
**BENEFITS**

- Low Cost
- Automatic Insertion Package

**ABSOLUTE MAXIMUM RATINGS (25°C)**

|   |              |
|---|--------------|
| Drain-Gate Voltage . . . . .  | 25 V         |
| Source-Gate Voltage . . . . .   | 25 V         |
| Drain-Source Voltage . . . . .  | 25 V         |
| Forward Gate Current . . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |

TO-92  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

|                            |   | Characteristic  | Min  | Typ   | Max   | Unit | Test Conditions                                       |
|----------------------------|---|---|------|-------|-------|------|---|
| S<br>T<br>A<br>T<br>I<br>C | 1 | I <sub>GSS</sub> Gate Reverse Current                       |      | -0.01 | -100  | nA   | V <sub>GS</sub> = -10 V, V <sub>DS</sub> = 0          |
|                            | 2 | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | -25  |       |       | V    | I <sub>G</sub> = -10 μA, V <sub>DS</sub> = 0          |
|                            | 3 | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage             | -0.5 |       | -10.0 |      | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 μA         |
|                            | 4 | I <sub>DSS</sub> Saturation Drain Current                   | 1    |       | 25    | mA   | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, (Note 1) |
| D<br>Y<br>N                | 5 | g <sub>fs</sub> Common-Source Forward Transconductance      | 1000 |       | 7500  | μmho | f = 1 kHz   |
|                            | 6 | Re(y <sub>fs</sub> ) Common-Source Forward Transconductance | 800  |       |       |      | f = 100 MHz   |
|                            | 7 | C <sub>iss</sub> Common-Source Input Capacitance            |      | 3.5   |       | pF   | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0           |
|                            | 8 | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |      | 0.85  |       |      |   |

**NOTE:**  
1. Pulse test PW = 300 μs, duty cycle < 3%.

NH

# p-channel JFETs designed for . . .



Performance Curves PS  
See Section 5

- Analog Switches
- Choppers
- Commutators

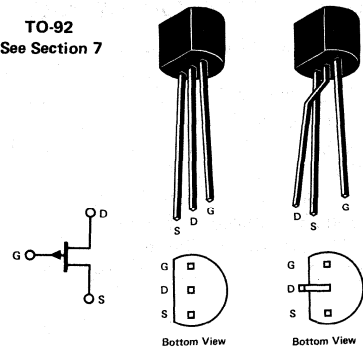
**BENEFITS**

- Low Insertion Loss  
 $R_{DS(on)} = 75 \Omega$  Maximum (P1086E)
- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

(-18)

|                            | Characteristic  | P1086 |      | P1087 |      | Unit | Test Conditions  |
|----------------------------|---|-------|------|-------|------|------|--|
|                            |   | Min   | Max  | Min   | Max  |      |  |
| S<br>T<br>A<br>T<br>I<br>C | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | 30    |      | 30    |      | V    | I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0   |
|                            | I <sub>GSS</sub> Gate Reverse Current                       |       | 2    |       | 2    | nA   | V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0  |
|                            | I <sub>D(off)</sub> Drain Cutoff Current                    |       | -10  |       | -10  | μA   | V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 12 V (P1086E)<br>V <sub>GS</sub> = 7 V (P1087E) |
|                            | I <sub>DGO</sub> Drain Reverse Current                      |       | 2    |       | 2    | nA   | V <sub>DG</sub> = -15 V, I <sub>S</sub> = 0  |
|                            | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage             |       | 10   |       | 5    | V    | V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1 μA  |
|                            | I <sub>DSS</sub> Saturation Drain Current                   |       | -10  |       | -5   | mA   | V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0   |
| D<br>Y<br>N                | V <sub>DS(on)</sub> Drain-Source ON Voltage                 |       | -0.5 |       | -0.5 | V    | V <sub>GS</sub> = 0, I <sub>D</sub> = -6 mA (P1086E), I <sub>D</sub> = -3 mA (P1087E)      |
|                            | r <sub>DS(on)</sub> Static Drain-Source ON Resistance       |       | 75   |       | 150  | Ω    | I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0  |
|                            | r <sub>ds(on)</sub> Drain-Source ON Resistance              |       | 75   |       | 150  | Ω    | I <sub>D</sub> = 0, V <sub>GS</sub> = 0  |
| S<br>W<br>I<br>T<br>C<br>H | C <sub>iss</sub> Common-Source Input Capacitance            |       | 45   |       | 45   | pF   | V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0   |
|                            | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |       | 10   |       | 10   |      | V <sub>DS</sub> = 0, V <sub>GS</sub> = 12 V (P1086E)<br>V <sub>GS</sub> = 7 V (P1087E)     |
| S<br>W<br>I<br>T<br>C<br>H | t <sub>d(on)</sub> Turn-ON Delay Time                       |       | 15   |       | 15   | ns   | V <sub>DD</sub> = -6 V, V <sub>GS(on)</sub> = 0  |
|                            | t <sub>r</sub> Rise Time                                    |       | 20   |       | 75   |      | V <sub>GS(off)</sub> I <sub>D(on)</sub> R <sub>L</sub>                                     |
|                            | t <sub>d(off)</sub> Turn-OFF Delay Time                     |       | 15   |       | 25   |      | P1086E    12 V    -6 mA    910 Ω   |
|                            | t <sub>f</sub> Fall Time                                    |       | 50   |       | 100  |      | P1087E    7 V    -3 mA    1.8K Ω   |

**NOTE:**

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

PS

# n-channel JFETs designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

**Performance Curves NC**  
See Section 5

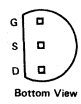
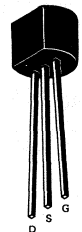
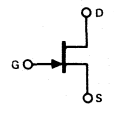
**BENEFITS**

- Low Insertion Loss  
High Accuracy in Test Systems  
 $R_{ON} < 30 \Omega$  (PN4091)
- High Off-Isolation  
 $I_{D(off)} < 200 \text{ pA}$
- High Speed  
 $t_{rise} < 10 \text{ ns}$  (PN4091)
- Short Sample and Hold Aperture Time  
 $C_{rss} < 5 \text{ pF}$

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . -40 V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

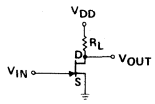
TO-92  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic                                     | PN4091 |     | PN4092 |     | PN4093 |     | Unit   | Test Conditions                                |                         |       |
|--|--------|-----|--------|-----|--------|-----|--------|--|-------------------------|-------|
|  | Min    | Max | Min    | Max | Min    | Max |        |  |                         |       |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage  | -40    |     | -40    |     | -40    |     | V      | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0    |                         |       |
| 2 IDGO Drain Reverse Current                       |        | 200 |        | 200 |        | 200 | pA     | V <sub>GS</sub> = -20 V, I <sub>S</sub> = 0    |                         |       |
| 3  |        | 400 |        | 400 |        | 400 | nA     | 150°C  |                         |       |
| 4 ID(off) Drain Cutoff Current                     |        |     |        |     |        | 200 | pA     | V <sub>DS</sub> = 20 V                         | V <sub>GS</sub> = -6 V  | 150°C |
|  |        |     |        |     |        | 400 | nA     |  |                         |       |
|  |        |     |        |     |        | 200 | pA     |  | V <sub>GS</sub> = -8 V  | 150°C |
|  |        |     |        |     |        | 400 | nA     |  |                         |       |
|  |        |     |        |     |        |     |        |  | V <sub>GS</sub> = -12 V | 150°C |
|  |        |     |        |     |        |     |        |  |                         |       |
| 7 VGS(off) Gate-Source Cutoff Voltage              | -5     | -10 | -2     | -7  | -1     | -5  | V      | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 mA  |                         |       |
| 11 IDSS Saturation Drain Current (Note 1)          | 30     |     | 15     |     | 8      |     | mA     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0    |                         |       |
| 12 VDS(on) Drain-Source ON Voltage                 |        |     |        |     |        | 0.2 | V      | V <sub>GS</sub> = 0                            | I <sub>D</sub> = 2.5 mA |       |
|  |        |     |        |     |        |     |        |  | I <sub>D</sub> = 4 mA   |       |
|  |        |     |        |     |        |     |        |  | I <sub>D</sub> = 6.6 mA |       |
| 14 rDS(on) Static Drain-Source ON Resistance       |        | 30  |        | 50  |        | 80  | Ω      | V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA     |                         |       |
| 16 rds(on) Drain-Source ON Resistance              |        | 30  |        | 50  |        | 80  | Ω      | V <sub>GS</sub> = 0, I <sub>D</sub> = 0        |                         |       |
| 17 Ciss Common-Source Input Capacitance            |        | 16  |        | 16  |        | 16  | pF     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0    |                         |       |
| 18 Crss Common-Source Reverse Transfer Capacitance |        | 5   |        | 5   |        | 5   |        | V <sub>DS</sub> = 0, V <sub>GS</sub> = -20 V   |                         |       |
| 19 tD(on) Turn-ON Delay Time                       |        | 15  |        | 15  |        | 20  | ns     | V <sub>DD</sub> = 3 V, V <sub>GS(on)</sub> = 0 |                         |       |
| 20 tr Rise Time                                    |        | 10  |        | 20  |        | 40  |        | I <sub>D(on)</sub>                             | V <sub>GS(off)</sub>    | RL    |
| 21 tOff Turn-OFF Time                              |        | 40  |        | 60  |        | 80  |        | PN4091   | -12 V                   | 425 Ω |
|  |        |     |        |     |        |     | PN4092 | -8   | 700                     |       |
|  |        |     |        |     |        |     | PN4093 | -6   | 1120                    |       |

**NOTE:**  
1. Pulswidth = 300 μs, duty cycle ≤ 3%.



**INPUT PULSE**  
 RISE TIME < 1 ns  
 FALL TIME < 1 ns  
 PULSE WIDTH 1 μs  
 PULSE DUTY CYCLE ≤ 10%  
 PULSE GENERATOR IMPEDANCE 50Ω

**SAMPLING SCOPE**  
 RISE TIME 0.4 ns  
 INPUT RESISTANCE 10 M  
 INPUT CAPACITANCE 1.7 pF

# n-channel JFETs designed for . . .



**Performance Curves NP**  
**See Section 5**

## ■ General Purpose Amplifiers

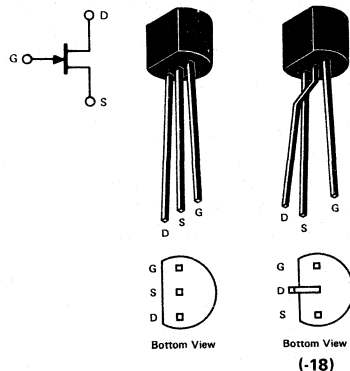
### BENEFITS

- Low Cost
- High Input Impedance  
 $I_G = 35 \text{ pA}$  Typically
- Low Noise  
 $\bar{e}_n = 5 \text{ nV}/\sqrt{\text{Hz}}$  Typically @ 1 kHz

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Gate-Drain or Gate-Source Voltage (Note 1) . . . . .                      | -30V         |
| Gate Current . . . . .  | 50 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |

TO-92  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic  | PN4302   |                               | PN4303 |      | PN4304 |      | Unit          | Test Conditions                                 |  |
|---|--|-------------------------------|--------|------|--------|------|---------------|---|--|
|   | Min  | Max                           | Min    | Max  | Min    | Max  |               |   |  |
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12<br>S<br>T<br>A<br>T<br>I<br>C | $I_{GSS}$  |                               | 1      |      | -1     |      | nA            | $V_{GS} = -10 \text{ V}$ ,<br>$V_{DS} = 0$      | $T_A = 85^\circ \text{C}$  |
|   | Gate Reverse Current (Note 2)                                |                               | 0.1    |      | -0.1   |      | $\mu\text{A}$ |   |  |
|   | $BV_{GSS}$   | Gate-Source Breakdown Voltage | -30    |      | -30    |      | -30           | V   |  |
| $V_{GS(off)}$   | Gate-Source Cutoff Voltage                                   |                               | -4.0   |      | -6.0   |      | -10           | $V_{DS} = 20 \text{ V}$ , $I_D = 10 \text{ nA}$ |  |
| $I_{DSS}$   | Saturation Drain Current (Note 3)                            | 0.5                           | 5.0    | 4.0  | 10     | 0.5  | 15            | mA  |  |
| $g_{fs}$  | Common-Source Forward Transconductance (Note 3)              | 1000                          |        | 2000 |        | 1000 |               | $\mu\text{mho}$                                 | $V_{DS} = 20 \text{ V}$ ,<br>$V_{GS} = 0$                                      |
| $g_{os}$  | Common-Source Output Conductance                             |                               | 50     |      | 50     |      | 50            | $\mu\text{mho}$                                 |  |
| $C_{rss}$   | Common-Source Reverse Transfer Capacitance                   |                               | 3      |      | 3      |      | 3             | pF  | f = 1 MHz  |
| $C_{iss}$   | Common-Source Input Capacitance                              |                               | 6      |      | 6      |      | 6             | pF  | f = 140 kHz  |
| $CDG$   | Drain-Gate Capacitance                                       |                               | 2      |      | 2      |      | 2             | pF  | $V_{DG} = 10 \text{ V}$ ,<br>$I_S = 0$   |
| NF  | Noise Figure   |                               | 2.0    |      | 2.0    |      | 3.0           | dB  | $V_{DS} = 10 \text{ V}$ ,<br>$V_{GS} = 0$ ,<br>$R_{gen} = 1.0 \text{ M}\Omega$ |
| $ y_{fs} $  | Common-Source Short Circuit Forward Transadmittance (Note 3) | 700                           |        | 1400 |        | 700  |               | $\mu\text{mho}$                                 | $V_{DS} = 20 \text{ V}$ ,<br>$V_{GS} = 0$                                      |

NP

**NOTES:**

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in  $T_A$ .
3. Pulse test duration = 2 ms.



# n-channel JFETs designed for ...



Performance Curves NC  
See Section 5

- Analog Switches
- Commutators
- Choppers

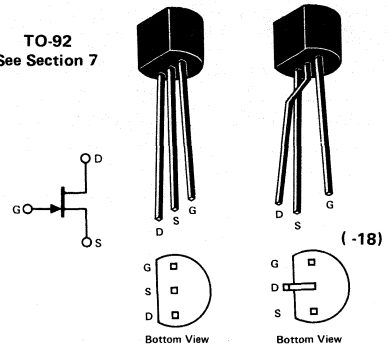
### BENEFITS

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive  
High Isolation Resistance from Driver
- Low Cost

### ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage ..... -40 V  
 Forward Gate Current ..... 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) ..... 360 mW  
 Operating Temperature Range ..... -55 to 135°C  
 Storage Temperature Range ..... -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) ..... 300°C

TO-92  
See Section 7



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic |                      | PN4391                                     |     | PN4392 |      | PN4393 |      | Unit | Test Conditions                                 |           |
|----------------|----------------------|--|-----|--------|------|--------|------|------|---|-----------|
|                |                      | Min  | Max | Min    | Max  | Min    | Max  |      |   |           |
| 1              | I <sub>GSS</sub>     | Gate Reverse Current                       |     | -1.0   | -1.0 | -1.0   | -1.0 | nA   | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0    | 100°C     |
| 2              |                      | BV <sub>GSS</sub>                          |     | -40    | -40  | -40    | -40  |      |   |           |
| 3              | I <sub>D(off)</sub>  | Gate-Source Breakdown Voltage              |     | -40    | -40  | -40    | -40  | nA   | V <sub>DS</sub> = 20 V                          | 100°C     |
| 4              |                      | Drain Cutoff Current                       |     |        |      |        | 1.0  |      |   |           |
| 5              |                      | Drain Cutoff Current                       |     |        |      |        | 200  |      |   |           |
| 6              |                      | Drain Cutoff Current                       |     |        | 1.0  |        |      |      |   |           |
| 7              | V <sub>GS(off)</sub> | Gate-Source Cutoff Voltage                 |     | -4     | -10  | -2     | -5   | V    | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA   | 100°C     |
| 8              |                      | Saturation Drain Current (Note 1)          |     | 50     | 150  | 25     | 75   |      |   |           |
| 9              |                      | Saturation Drain Current (Note 1)          |     | 5      | 30   | 5      | 30   |      |   |           |
| 10             | V <sub>DS(on)</sub>  | Drain-Source ON Voltage                    |     |        |      |        | 0.4  | V    | V <sub>GS</sub> = 0                             | 100°C     |
| 11             |                      | Static Drain-Source ON Resistance          |     | 30     | 60   | 100    | 100  |      |   |           |
| 12             |                      | Drain-Source ON Resistance                 |     | 30     | 60   | 100    | 100  |      |   |           |
| 13             | C <sub>iss</sub>     | Common-Source Input Capacitance            |     | 14     | 14   | 14     | 14   | pF   | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0     | f = 1 kHz |
| 14             |                      | Common-Source Reverse Transfer Capacitance |     |        |      |        | 3.5  |      |   |           |
| 15             |                      | Common-Source Reverse Transfer Capacitance |     |        |      |        | 3.5  |      |   |           |
| 16             |                      | Common-Source Reverse Transfer Capacitance |     | 3.5    |      |        |      |      |   |           |
| 17             | t <sub>d(on)</sub>   | Turn-ON Delay Time                         |     | 15     | 15   | 15     | 15   | ns   | V <sub>DD</sub> = 10 V, V <sub>GS(on)</sub> = 0 | f = 1 MHz |
| 18             | t <sub>r</sub>       | Rise Time                                  |     | 5      | 5    | 5      | 5    |      |   |           |
| 19             | t <sub>d(off)</sub>  | Turn-OFF Delay Time                        |     | 20     | 35   | 50     | 50   |      |   |           |
| 20             | t <sub>f</sub>       | Fall Time                                  |     | 15     | 20   | 30     | 30   |      |   |           |
| 21             |                      |  |     |        |      |        |      |      |   |           |
| 22             |                      |  |     |        |      |        |      |      |   |           |
| 23             |                      |  |     |        |      |        |      |      |   |           |
| 24             |                      |  |     |        |      |        |      |      |   |           |

#### NOTE:

1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

NC

PN4391 PN4392 PN4393  
PN4391-18 PN4392-18 PN4393-18

4

Siliconix

# n-channel JFETs designed for . . .



- VHF Amplifiers
- Mixers

**Performance Curves NH**  
See Section 5

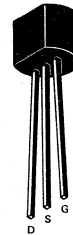
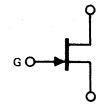
**BENEFITS**

- Low Noise  
NF = 3 dB Typical at 400 MHz
- Wide Band  
High  $g_{fs}/C_{iss}$  Ratio

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -30V  
 Gate Current . . . . . 10 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92  
See Section 7



Bottom View

| Characteristic                              |  | Min  | Max  | Unit | Test Conditions        |  |           |  |
|---|--|------|------|------|------------------------|--|-----------|--|
| S<br>T<br>A<br>T<br>I<br>C                  | 1<br>2<br>IGSS Gate Reverse Current                  |      | 1.0  | nA   | VGS = -15 V, VDS = 0 V |  |           |  |
|   | 3<br>BVGSS Gate-Source Breakdown Voltage             | -30  |      | V    | IG = -1 μA, VDS = 0 V  |  |           |  |
|   | 4<br>VGS(off) Gate-Source Cutoff Voltage             |      | -6   |      | VDS = 15 V, ID = 1 nA  |  |           |  |
| D<br>Y<br>N<br>A<br>M<br>I<br>C             | 5<br>IDSS Saturation Drain Current (Note 1)          | 5    | 15   | mA   | VDS = 15 V, VGS = 0 V  |  |           |  |
|   | 6<br>gfs Common-Source Forward Transconductance      | 4500 | 7500 | μmho |                        |  | f = 1 kHz |  |
|   | 7<br>gos Common-Source Output Conductance            |      | 50   |      |                        |  | f = 1 MHz |  |
|   | 8<br>Crss Common-Source Reverse Transfer Capacitance |      | 0.8  | pF   |                        |  |           |  |
|   | 9<br>Ciss Common-Source Input Capacitance            |      | 4    |      |                        |  |           |  |
| 10<br>Coss Common-Source Output Capacitance |  | 2    |      |      |                        |  |           |  |

| Characteristic  |  | 100 MHz |      | 400 MHz |        | Unit                             | Test Conditions       |
|---|--|---------|------|---------|--------|----------------------------------|-----------------------|
|   |  | Min     | Max  | Min     | Max    |                                  |                       |
| H<br>I<br>G<br>H<br>F<br>R<br>E<br>Q<br>U<br>E<br>N<br>C<br>Y | 11<br>giss Common-Source Input Conductance       |         | 100  |         | 1000   | μmho                             | VDS = 15 V, VGS = 0 V |
|   | 12<br>biss Common-Source Input Susceptance       |         | 2500 |         | 10,000 |                                  |                       |
|   | 13<br>goss Common-Source Output Conductance      |         | 75   |         | 100    |                                  |                       |
|   | 14<br>boss Common-Source Output Susceptance      |         | 1000 |         | 4000   |                                  |                       |
|   | 15<br>gfs Common-Source Forward Transconductance |         |      | 4000    |        |                                  |                       |
| 16<br>Gps Common-Source Power Gain                            | 18   |         | 10   |         | dB     | VDS = 15 V, ID = 5 mA            |                       |
| 17<br>NF Noise Figure   |  | 2       |      | 4       |        | VDS = 15 V, ID = 5 mA, RG = 1K Ω |                       |

NH

**NOTES:**

1. Pulse test duration = 300 μs.

# n-channel JFET designed for . . .



PN5163

## ■ Low and Medium Frequency Amplifiers

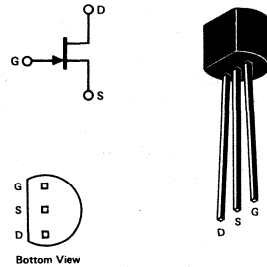
### BENEFITS

- Low Cost

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |       |              |
|---|-------|--------------|
| Gate-Drain or Gate-Source Voltage                               | ..... | -25V         |
| Gate Current (FWD)  | ..... | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) | ..... | 360 mW       |
| Operating Temperature Range                                     | ..... | -55 to 135°C |
| Storage Temperature Range                                       | ..... | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds)      | ..... | 300°C        |

TO-92  
See Section 7



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

|                            |                                 | Characteristic  | Min  | Max         | Unit                   | Test Conditions                                 |                       |
|----------------------------|---------------------------------|---|------|-------------|------------------------|---|-----------------------|
| 1<br>2<br>3<br>4<br>5<br>6 | S<br>T<br>A<br>T<br>I<br>C      | I <sub>GSS</sub> Gate Reverse Current                       |      | -10<br>-0.6 | nA<br>μA               | V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0    | T <sub>A</sub> = 85°C |
|                            |                                 | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | -25  |             |                        |   |                       |
|                            |                                 | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage             | -0.4 | -8.0        | V                      |   |                       |
| 5<br>6                     | C                               | V <sub>GS</sub> Gate-Source Voltage                         |      | -7.5        |                        | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 100 μA |                       |
|                            |                                 | I <sub>DSS</sub> Saturation Drain Current                   | 1.0  | 40          | mA                     | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0     |                       |
| 7                          |                                 | r <sub>ds(on)</sub> Drain-Source ON Resistance              |      | 500         | Ω                      | V <sub>GS</sub> = 0, I <sub>D</sub> = 0         |                       |
| 8<br>9<br>10<br>11<br>12   | D<br>Y<br>N<br>A<br>M<br>I<br>C | g <sub>fs</sub> Common-Source Forward Transconductance      | 2000 | 9000        |                        | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0     | f = 1 kHz             |
|                            |                                 | g <sub>os</sub> Common-Source Output Conductance            |      | 200         | μmho                   |   |                       |
|                            |                                 | g <sub>fs</sub> Common-Source Forward Transconductance      | 1800 |             |                        |   | f = 1 MHz             |
|                            |                                 | C <sub>iss</sub> Common-Source Input Capacitance            |      | 20          | pF                     |   |                       |
|                            |                                 | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |      | 5.0         |                        |   |                       |
| 13                         |                                 | NF Common-Source Spot Noise Figure                          |      | 3.0         | dB                     | R <sub>G</sub> = 150k Ω                         | f = 1 kHz             |
| 14                         |                                 | e <sub>N</sub> Equivalent Short Circuit Input Noise Voltage |      | 50          | $\frac{nV}{\sqrt{Hz}}$ | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 mA   | NBW = 150 Hz          |

\*JEDEC registered data

4

Siliconix

# n-channel JFET

## designed for . . .



**Performance Curves NH**  
See Section 5

- VHF/UHF Amplifiers
- Mixers
- Oscillators

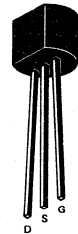
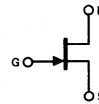
### BENEFITS

- Specified for 200 MHz Operation

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Drain-Gate Voltage . . . . .  | 30V          |
| Source-Gate Voltage . . . . .   | 30V          |
| Drain-Source Voltage . . . . .  | 30V          |
| Forward Gate Current . . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |

TO-92  
See Section 7



Bottom View

### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic |                                 | Min   | Max                                      | Unit   | Test Conditions |   |   |   |
|----------------|---------------------------------|---|--|--------|-----------------|---|---|---|
| 1              | S<br>T<br>A<br>T<br>I<br>C      | I <sub>GSS</sub> Gate Reverse Current                       |  | -250   | pA              | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0                                  | T <sub>A</sub> = +85°C                      |   |
| 2              |                                 |   |  | -15    | nA              |   |   |   |
| 3              | D<br>Y<br>N<br>A<br>M<br>I<br>C | BV <sub>GSS</sub> Gate-Source Breakdown Voltage             | -30                                      |        | V               | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0                                   |   |   |
| 4              |                                 | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage             | -0.5                                     | -8.0   |                 |   |   | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 μA |
| 5              |                                 | I <sub>DSS</sub> Saturation Drain Current                   | 4.0                                      | 25     | mA              | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 (Note 1)                          |   |   |
| 6              |                                 | r <sub>DS(on)</sub> Drain-Source ON Resistance              |  | 300    | Ω               |   |   | I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0    |
| 7              |                                 | g <sub>fs</sub> Common-Source Forward Transconductance      | 4,500                                    | 10,000 | μmhos           | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0                                   | f = 1 kHz                                   |   |
| 8              |                                 | Re(y <sub>fs</sub> ) Common-Source Forward Transconductance | 4,000                                    |        |                 |   | f = 200 MHz                                 |   |
| 9              |                                 | Re(y <sub>os</sub> ) Common-Source Output Conductance       |  | 150    |                 |   |   |   |
| 10             |                                 | Re(y <sub>is</sub> ) Common-Source Input Conductance        |  | 800    |                 |   |   |   |
| 11             |                                 | C <sub>iss</sub> Common-Source Input Capacitance            |  | 6.0    |                 |   |   | pF  |
| 12             |                                 | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |  | 2.0    |                 |   |   |   |
| 13             |                                 | NF Noise Figure   |  | 3.0    | dB              | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1K Ω            | f = 200 MHz                                 |   |
| 14             |                                 |   |  | 5.0    |                 | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1M Ω, BW = 5 Hz | f = 10 Hz                                   |   |
| 15             |                                 |   | G <sub>PS</sub> Common-Source Power Gain | 15     |                 |   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 | f = 200 MHz                                   |

#### NOTE:

- Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH

# n-channel JFETs designed for . . .



U1897 U1898 U1899  
U1897-18 U1898-18 U1899-18

- Analog Switches
- Choppers
- Commutators

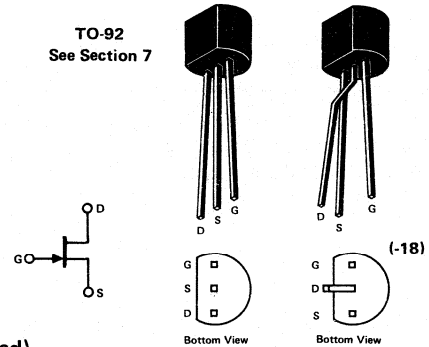
Performance Curves NC  
See Section 5

### BENEFITS

- Low Insertion Loss  
 $R_{DS(on)} < 30 \Omega$  (U1897E)
- No Error or Offset Voltage Generated by Closed Switch  
Purely Resistive

### ABSOLUTE MAXIMUM RATINGS (25°C)

|   |              |
|---|--------------|
| Gate-Drain or Gate-Source Voltage . . . . .                               | -40V         |
| Gate Current . . . . .  | 10 mA        |
| Total Device Dissipation at 25°C Ambient<br>(Derate 3.27 mW/°C) . . . . . | 360 mW       |
| Operating Temperature Range . . . . .                                     | -55 to 135°C |
| Storage Temperature Range . . . . .                                       | -55 to 150°C |
| Lead Temperature Range<br>(1/16" from case for 10 seconds) . . . . .      | 300°C        |



### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| Characteristic   | U1897 |      | U1898 |      | U1899 |      | Unit     | Test Conditions  |  |
|--|-------|------|-------|------|-------|------|----------|--|--|
|  | Min   | Max  | Min   | Max  | Min   | Max  |          |  |  |
| 1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage              | -40   |      | -40   |      | -40   |      | V        | $I_G = -1 \mu A, V_{DS} = 0$   |  |
| 2 BV <sub>DGO</sub> Drain-Gate Breakdown Voltage               | 40    |      | 40    |      | 40    |      | V        | $I_G = -1 \mu A, I_S = 0$  |  |
| 3 BV <sub>SGO</sub> Source-Gate Breakdown Voltage              | 40    |      | 40    |      | 40    |      | V        | $I_G = -1 \mu A, I_D = 0$  |  |
| 4 I <sub>GSS</sub> Gate Reverse Current                        |       | -400 |       | -400 |       | -400 | pA       | $V_{GS} = -20 V, V_{DS} = 0$   |  |
| 5 I <sub>DGO</sub> Drain-Gate Leakage Current                  |       | 200  |       | 200  |       | 200  |          | $V_{DG} = 20 V, I_S = 0$   |  |
| 6 I <sub>SGO</sub> Source-Gate Leakage Current                 |       | 200  |       | 200  |       | 200  |          | $V_{SG} = 20 V, I_D = 0$   |  |
| 7 I <sub>D(off)</sub> Drain Cutoff Current                     |       | 200  |       | 200  |       | 200  | nA       | $V_{DS} = 20 V, V_{GS} = -12 V$ (U1897E)   |  |
| 8 I <sub>D(off)</sub> Drain Cutoff Current                     |       | 10   |       | 10   |       | 10   |          | $V_{GS} = -8 V$ (U1898E)<br>$V_{GS} = -6 V$ (U1899E) $T_A = 85^\circ C$                    |  |
| 9 V <sub>GS(off)</sub> Gate-Source Cutoff Voltage              | -5.0  | -10  | -2.0  | -7.0 | -1.0  | -5.0 | V        | $V_{DS} = 20 V, I_D = 1 mA$  |  |
| 10 I <sub>DSS</sub> Saturation Drain Current (Note 1)          | 30    |      | 15    |      | 8.0   |      | mA       | $V_{DS} = 20 V, V_{GS} = 0$  |  |
| 11 V <sub>DS(on)</sub> Drain-Source ON Voltage                 |       | 0.2  |       | 0.2  |       | 0.2  | V        | $V_{GS} = 0, I_D = 6.6 mA$ (U1897E)<br>$I_D = 4.0 mA$ (U1898E),<br>$I_D = 2.5 mA$ (U1899E) |  |
| 12 r <sub>DS(on)</sub> Static Drain-Source ON Resistance       |       | 30   |       | 50   |       | 80   | $\Omega$ | $I_D = 1 mA, V_{GS} = 0$   |  |
| 13 C <sub>DG</sub> Drain-Gate Capacitance                      |       | 5    |       | 5    |       | 5    | pF       | $V_{DG} = 20 V, I_S = 0$   |  |
| 14 C <sub>SG</sub> Source-Gate Capacitance                     |       | 5    |       | 5    |       | 5    |          | $V_{SG} = 20 V, I_D = 0$   |  |
| 15 C <sub>iss</sub> Common-Source Input Capacitance            |       | 16   |       | 16   |       | 16   |          | $V_{DS} = 20 V, V_{GS} = 0$<br>$f = 1 MHz$   |  |
| 16 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance |       | 3.5  |       | 3.5  |       | 3.5  | ns       | Switching Time Test Conditions<br>U1897E U1898E U1899E                                     |  |
| 17 t <sub>d(on)</sub> Turn ON Delay Time                       |       | 15   |       | 15   |       | 20   |          |  | $V_{DD} \quad 3 V \quad 3 V \quad 3 V$   |
| 18 t <sub>r</sub> Rise Time                                    |       | 10   |       | 20   |       | 40   |          |  | $V_{GS(on)} \quad 0 \quad 0 \quad 0$<br>$V_{GS(off)} \quad -12 V \quad -8 V \quad -6 V$<br>$R_L \quad 430 \Omega \quad 700 \Omega \quad 1100 \Omega$<br>$I_D(on) \quad 6.6 mA \quad 4 mA \quad 2.5 mA$ |
| 19 t <sub>off</sub> Turn OFF Time                              |       | 40   |       | 60   |       | 80   |          |  |  |

**NOTE:**

1. Pulse test pulsewidth = 300  $\mu s$ ; duty cycle  $\leq 3\%$ .

NC

4

Siliconix

# n-channel silicon JFET

## designed for . . .



**Performance Curves NH**  
See Section 5

- VHF Amplifiers
- Mixers

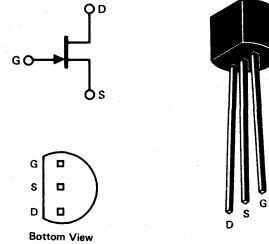
**BENEFITS**

- Low Noise  
NF = 3 dB Typical at 400 MHz
- Wideband  
High  $G_{fs}/C_{iss}$  Ratio
- Specified for Operation at 400 MHz

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -30V  
 Forward Gate Current . . . . . 10 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C

TO-92  
See Section 7



**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

| Characteristic |   | Min     | Max  | Unit    | Test Conditions                                 |                        |  |
|----------------|---|---------|------|---------|---|------------------------|--|
| 1              | I <sub>GSS</sub> Gate Reverse Current                           |         | -100 | pA      | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0    | T <sub>A</sub> = 100°C |  |
|                |   |         | -10  | nA      |   |                        |  |
| 3              | BV <sub>GSS</sub> Gate-Source Breakdown Voltage                 | -30     |      | V       | I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0     |                        |  |
| 4              | V <sub>GS(off)</sub> Gate-Source Cutoff Voltage                 |         | -6   | V       | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 nA   |                        |  |
| 5              | V <sub>GS</sub> Gate-Source Voltage                             | -1.0    | -5.5 | V       | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 500 μA |                        |  |
| 6              | I <sub>DSS</sub> Saturation Drain Current (Note 1)              | 5       | 15   | mA      | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0     |                        |  |
| 7              | g <sub>fs</sub> Common-Source Forward Transconductance (Note 1) | 4500    | 7500 | μmho    | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0     | f = 1 kHz              |  |
| 8              | g <sub>os</sub> Common-Source Output Conductance                |         | 50   | μmho    |   |                        |  |
| 9              | C <sub>rss</sub> Common-Source Reverse Transfer Capacitance     |         | 1    | pF      |   |                        |  |
| 10             | C <sub>iss</sub> Common-Source Input Capacitance                |         | 4    | pF      | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0     | f = 1 MHz              |  |
| 11             | C <sub>oss</sub> Common-Source Output Capacitance               |         | 2    |         |   |                        |  |
| Characteristic |   | 100 MHz |      | 400 MHz |   | Unit                   | Test Conditions  |
|                |   | Min     | Max  | Min     | Max   |                        |  |
| 12             | g <sub>iss</sub> Common-Source Input Conductance                |         | 100  |         | 1000  | μmho                   | V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0                          |
| 13             | b <sub>iss</sub> Common-Source Input Susceptance                |         | 2500 |         | 10,000  | μmho                   |  |
| 14             | g <sub>oss</sub> Common-Source Output Conductance               |         | 75   |         | 100   | μmho                   |  |
| 15             | b <sub>oss</sub> Common-Source Output Susceptance               |         | 1000 |         | 4000  | μmho                   |  |
| 16             | g <sub>fs</sub> Common-Source Forward Transconductance (Note 1) |         |      | 4000    |   | μmho                   |  |
| 17             | G <sub>ps</sub> Common-Source Power Gain                        | 18      |      | 10      |   | dB                     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA                        |
| 18             | NF Noise Figure   |         | 2    |         | 4   | dB                     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 mA, R <sub>G</sub> = 1K Ω |

**NOTE:**

1. Pulse test duration = 300 μs.

NH

# **geometry characteristics**

**index 5**



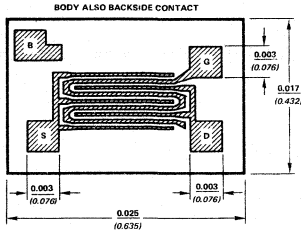


### enhancement-type p-channel MOSFET designed for . . .

- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

**BENEFITS:**

- High Gate Transient Voltage Breakdown Eliminates Need for Gate Protective Diode
- Ultra-High Input Impedance
- Low Leakage
- Normally OFF

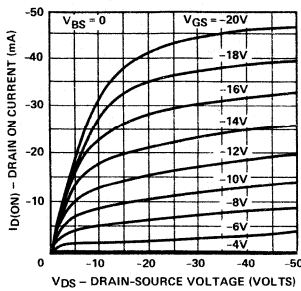


ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

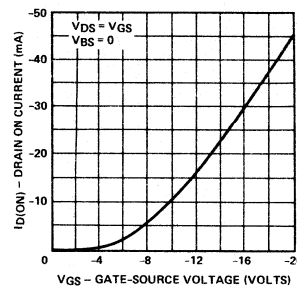
| TYPE   | PACKAGE | PRINCIPAL DEVICES      |
|--------|---------|------------------------|
| Single | TO-18   | MFE823                 |
| Single | TO-72   | 3N163-64               |
| Single | Chip    | 3N163-64CHP, MFE823CHP |

### PERFORMANCE CURVES (25°C unless otherwise noted)

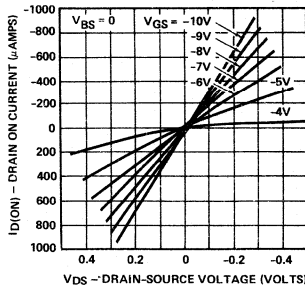
Output Characteristics



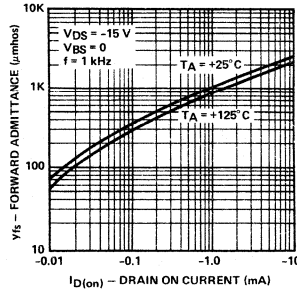
Transfer Characteristic



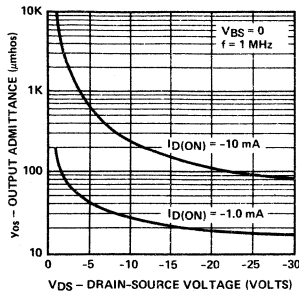
Low-Level Output Characteristics



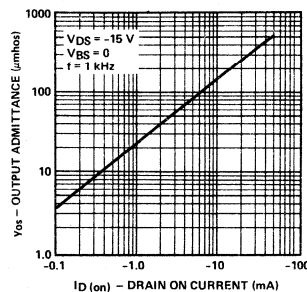
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage

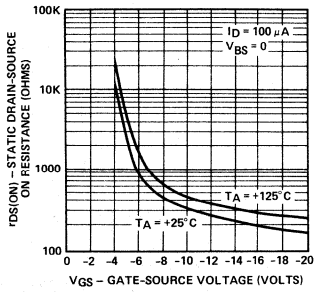


Common-Source, Short-Circuit, Output Admittance vs Drain Current

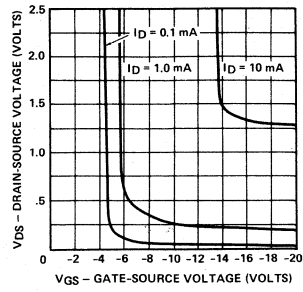


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

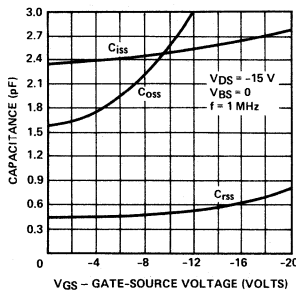
Drain-Source ON Resistance vs Gate-Source Voltage



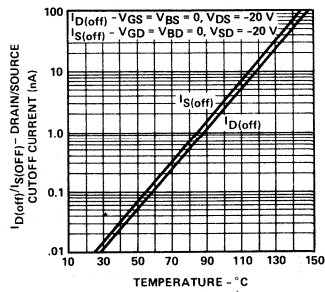
Low-Level ON Drain-Source Voltage vs Gate-Source Voltage



Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature



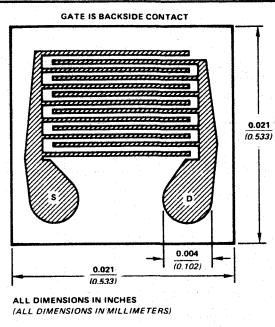


### n-channel JFETs designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

#### BENEFITS:

- No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance From Driver
- High Off-Isolation  $I_{D(off)} < 100 \text{ pA}$
- High Speed  $t_{ON} < 20 \text{ ns}$



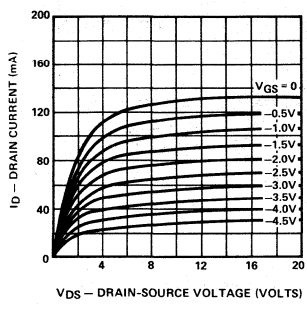
| TYPE   | PACKAGE         |
|--------|-----------------|
| Single | TO-18           |
| Dual   | TO-71           |
| Single | TO-92           |
|        | TO-92 Lead-form |
| Single | Chip            |
| Dual   | Chip            |

#### PRINCIPAL DEVICES

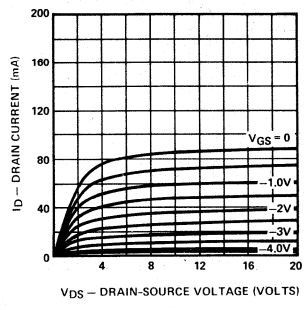
2N3970-72, 2N4091-93, 2N4391-93  
 2N4856-61, 2N4856A-61A, U200-02, UCR2N  
 2N5564-66  
 2N5638-40, 2N5653-54, J111-13, PN4091-93,  
 PN4302-04, PN4391-93, U1897-99  
 J111-18 - J113-18, PN4302-18 - PN4304-18,  
 PN4391-18 - PN4393-18, U1897-18 - U1899-18  
 All of above single devices  
 2N5566 CHP

### PERFORMANCE CURVES (25°C unless otherwise noted)

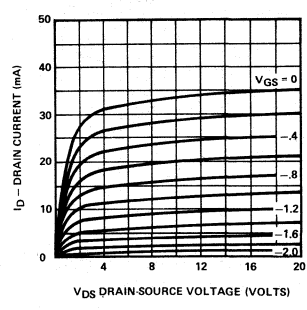
Output Characteristic



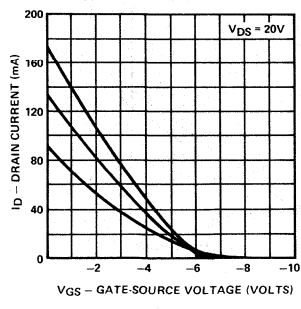
Output Characteristic



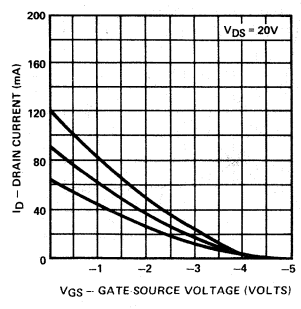
Output Characteristic



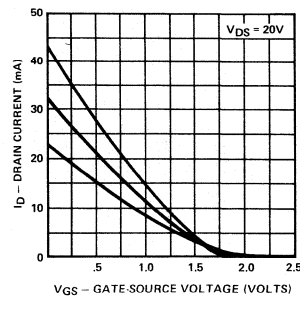
Transfer Characteristics



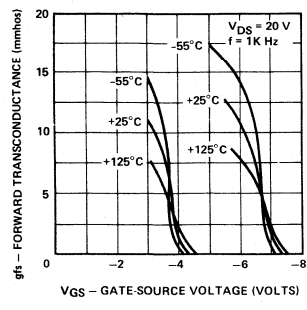
Transfer Characteristics



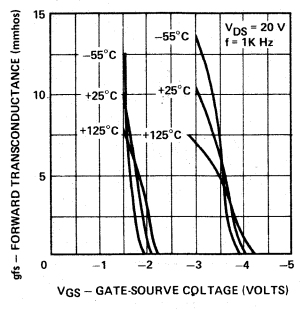
Transfer Characteristics



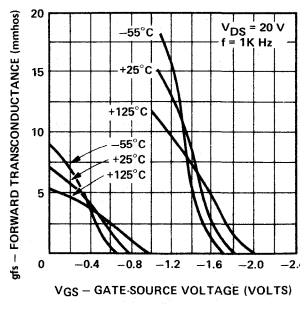
Transconductance Characteristics



Transconductance Characteristics

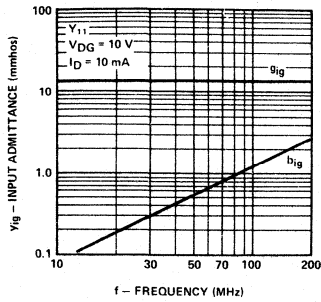


Transconductance Characteristics

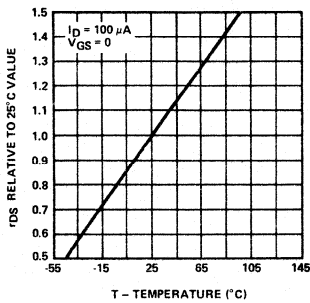


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

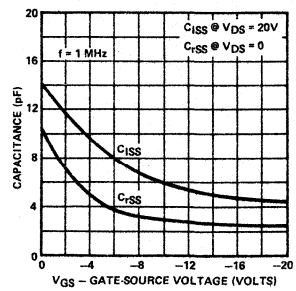
Common-Gate Input Admittance vs Frequency



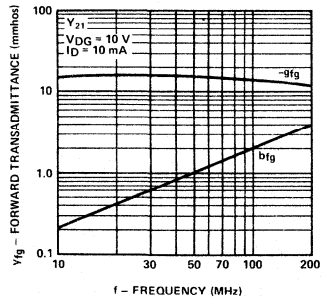
ON Resistance vs Ambient Temperature



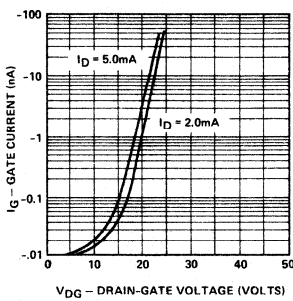
Common-Source Capacitances vs Gate-Source Voltage



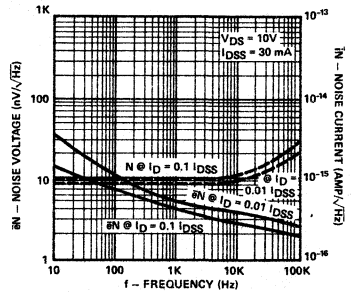
Common-Gate Forward Transadmittance vs Frequency



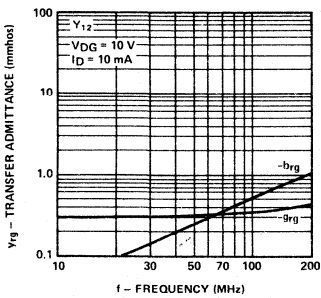
Gate Operating Current vs Drain-Gate Voltage



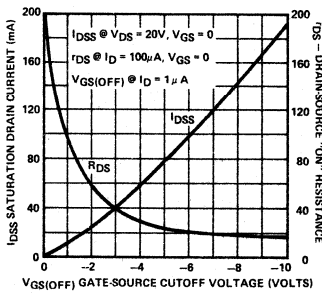
Equivalent Input Noise Voltage and Noise Current vs Frequency



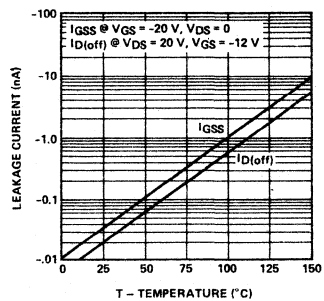
Common-Gate Reverse Transfer Admittance vs Frequency



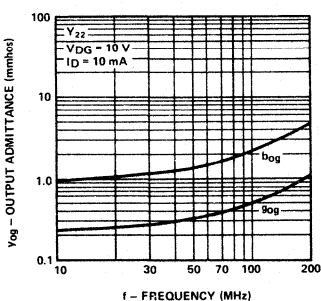
Drain Current & ON Resistance vs Gate-Source Cutoff Voltage



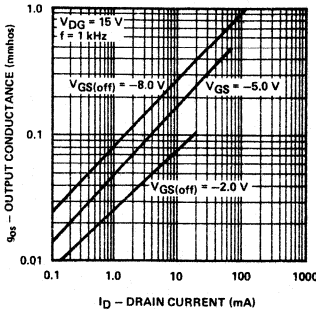
Leakage Current vs Ambient Temperature



Common-Gate Output Admittance vs Frequency



Common-Source Output Conductance vs Drain Current

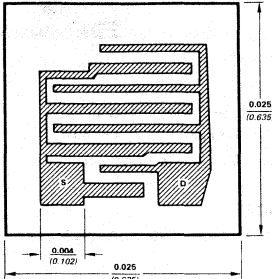


### n-channel JFET current regulator diode designed for . . .

- Current Regulation
- Current Limiting
- Biasing

**BENEFITS:**

- Simple Two Lead Current Source
- Simplifies Floating Current Sources  
No Power Supplies Required
- Low Cost



ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

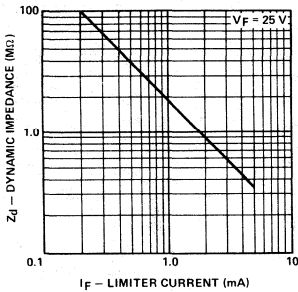
**TYPE**  
Single  
Single

**PACKAGE**  
TO-92  
Chip

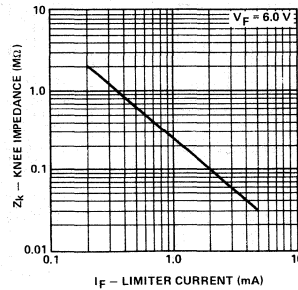
**PRINCIPAL DEVICES**  
J500-505, J506-511  
J500CHP-505CHP, J506CHP-511CHP

### PERFORMANCE CURVES (25°C unless otherwise noted)

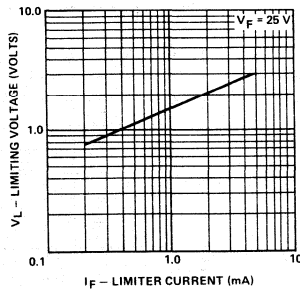
Dynamic Impedance vs  
Limiter Current



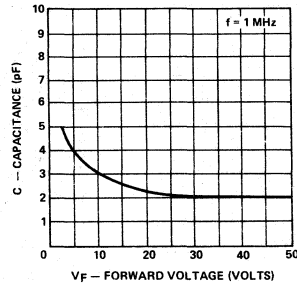
Knee Impedance vs Limiter Current



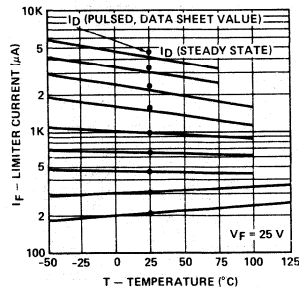
Limiting Voltage at 0.9 ID vs  
Limiter Current

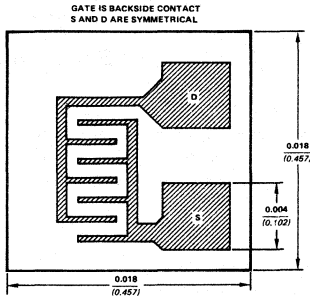


Capacitance vs Forward Voltage



Typical Variation of ID with Temperature  
Steady State and Pulsed Value





ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

## n-channel JFET designed for . . .

- Low and Medium Frequency Single and Differential Amplifiers
- High Input Impedance Amplifiers

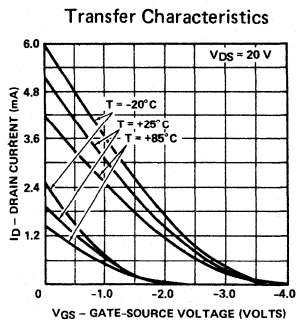
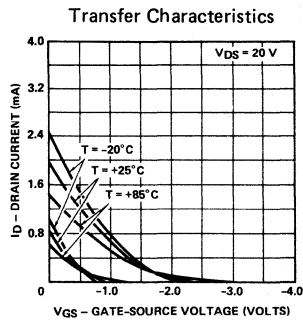
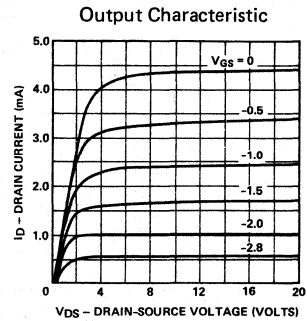
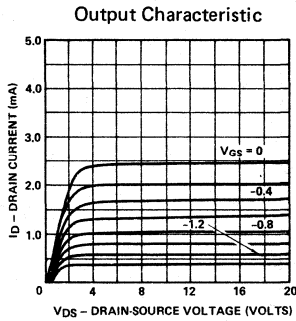
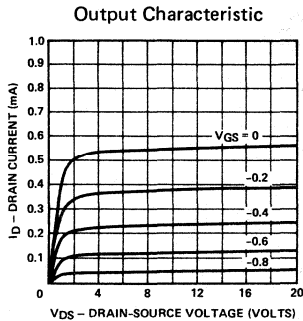


### BENEFITS:

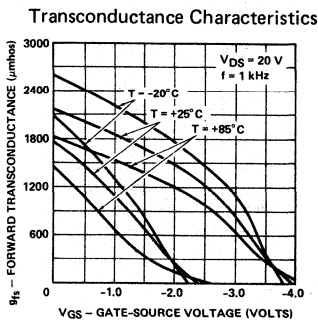
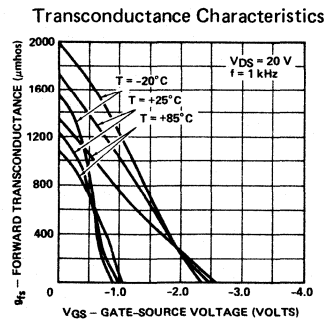
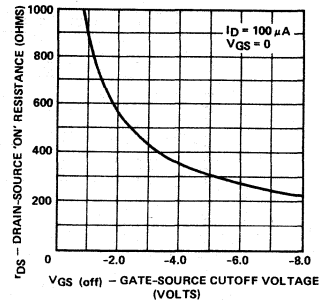
- Wide Dynamic Range  
I<sub>G</sub> Specified @ V<sub>DG</sub> = 20 V
- Low Capacitance C<sub>iss</sub> < 4 pF
- Low Output Conductance

| TYPE   | PACKAGE | PRINCIPAL DEVICES                                     |
|--------|---------|---|
| Dual   | TO-71   | 2N3954, 2N3954A, 2N3955, 2N3955A, 2N3956-8, 2N5452-54 |
| Single | TO-72   | 2N3684-7  |
| Dual   | Chip    | 2N3955CHP, 2N3956CHP-8CHP, 2N5454CHP                  |
| Single | Chip    | 2N3684CHP-7CHP  |

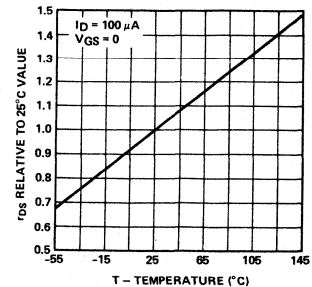
## PERFORMANCE CURVES (25°C unless otherwise noted)



### Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage

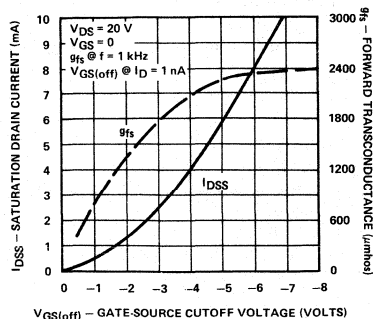


### 'ON' Resistance vs Ambient Temperature

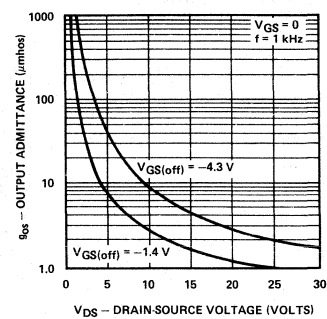


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

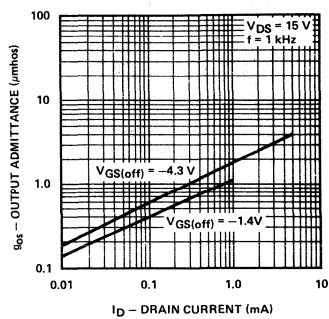
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



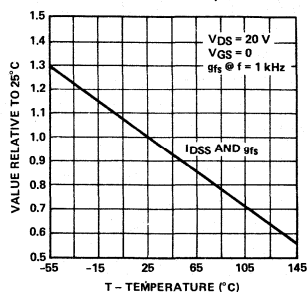
Common-Source Output Conductance vs Drain-Source Voltage



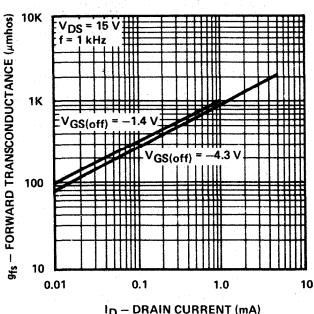
Common-Source Output Conductance vs Drain Current



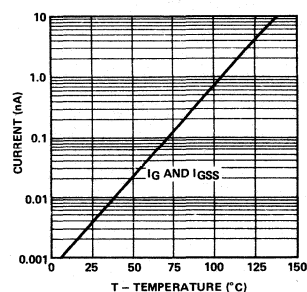
Drain Current and Transconductance vs Ambient Temperature



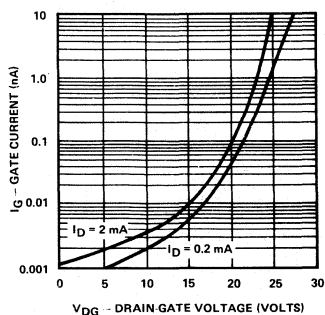
Common-Source Forward Transconductance vs Drain Current



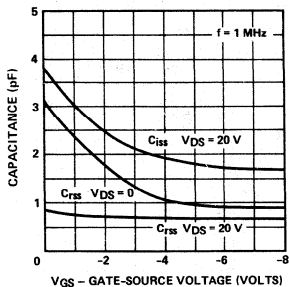
Leakage Currents vs Ambient Temperature



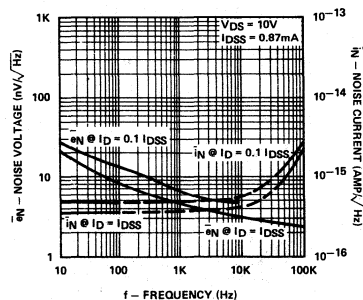
Gate Operating Current vs Drain-Gate Voltage



Common-Source Input Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency

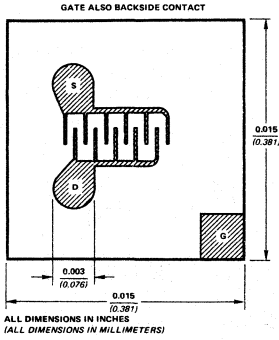


### n-channel JFET designed for . . .

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch

**BENEFITS:**

- Low Noise  
NF = 3 dB Typical @ 400 MHz
- Wideband  
High  $g_{fs}/C_{iss}$  Ratio



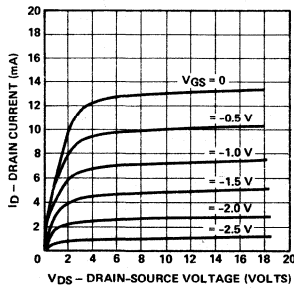
| TYPE   | PACKAGE |
|--------|---------|
| Single | TO-72   |
| Single | TO-92   |

| PRINCIPAL DEVICES   |
|---|
| 2N3966, 2N4416-16A  |
| 2N5484-6, 2N5555, 2N5668-70, MPF102, MPF108, MPF112, PN4416, J304-5, U1837, U1994 |
| KK4416-18, K304-18, KK305-18, K1837-18  |
| All of the above devices  |

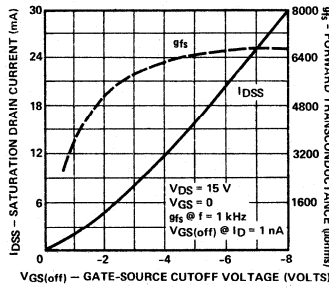
|        |                 |
|--------|-----------------|
| Single | TO-92 Lead-form |
| Single | Chip            |

### PERFORMANCE CURVES (25°C unless otherwise noted)

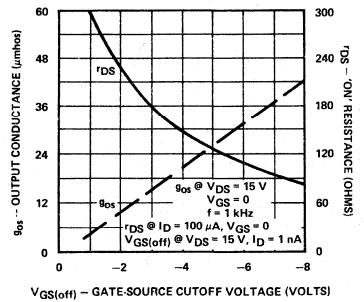
Output Characteristic



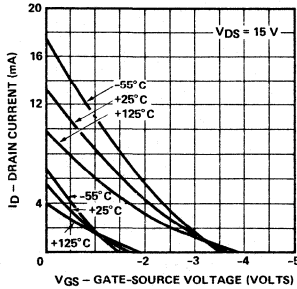
Drain Current & Transconductance vs Gate-Source Voltage



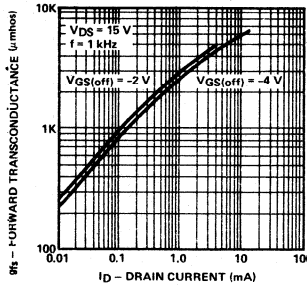
'ON' Resistance & Output Conductance vs Gate-Source Cutoff Voltage



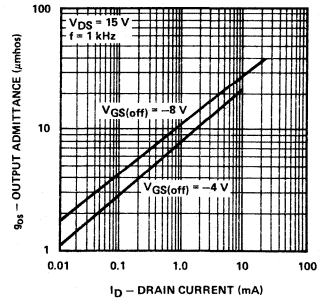
Transfer Characteristics



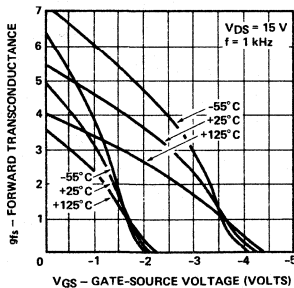
Common-Source Forward Transconductance vs Drain Current



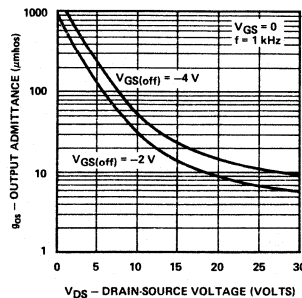
Common-Source Output Conductance vs Drain Current



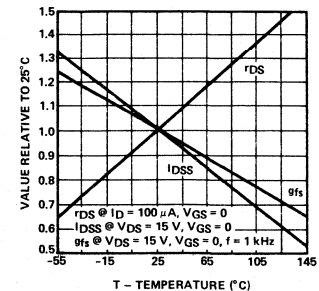
Transconductance Characteristics



Common-Source Output Conductance vs Drain-Source Voltage



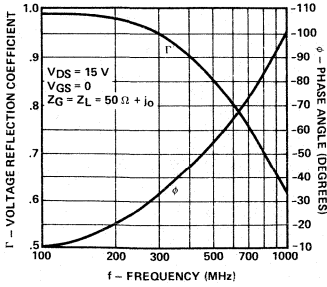
Drain Current, Transconductance and 'ON' Resistance vs Ambient Temperature



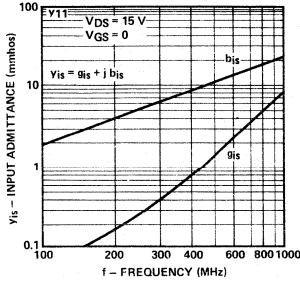


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

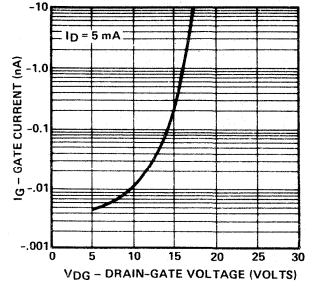
S Parameters S<sub>11</sub> Common-Source vs Frequency



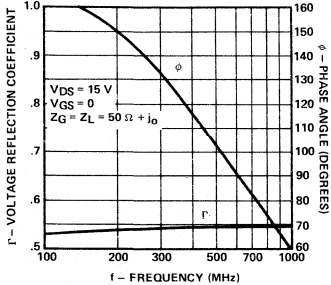
Common-Source Input Admittance vs Frequency



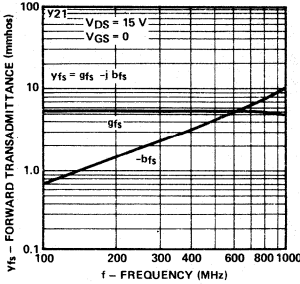
Gate Operating Current vs Drain-Gate Voltage



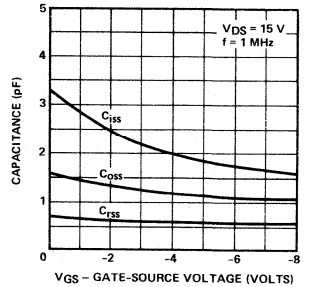
S Parameters S<sub>21</sub> Common-Source vs Frequency



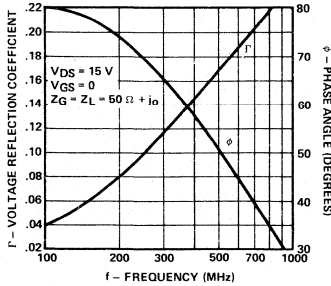
Common-Source Forward Transadmittance vs Frequency



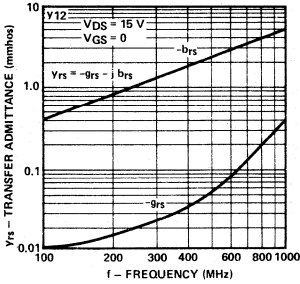
Common-Source Capacitances vs Gate-Source Voltage



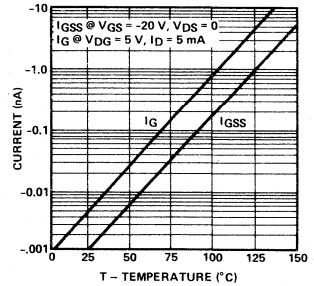
S Parameters S<sub>12</sub> Common-Source vs Frequency



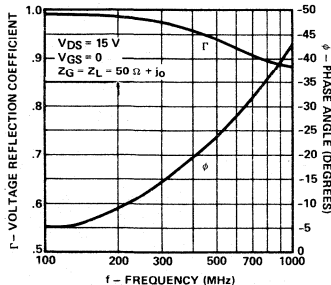
Common-Source Reverse Transfer Admittance vs Frequency



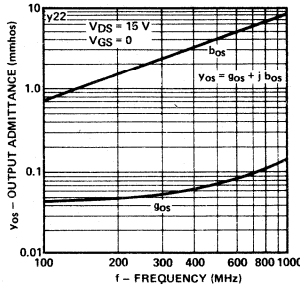
Gate Current vs Ambient Temperature



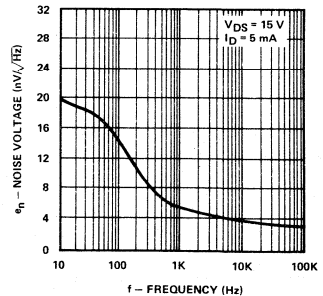
S Parameters S<sub>22</sub> Common-Source vs Frequency

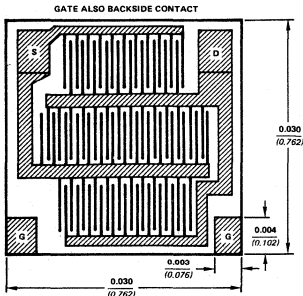


Common-Source Output Admittance vs Frequency



Equivalent Input Noise Voltage vs Frequency





ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

### n-channel JFET designed for . . .

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

| TYPE   | PACKAGE         |
|--------|-----------------|
| Single | TO-39           |
| Single | TO-52           |
| Single | TO-92           |
| Single | TO-92 Lead-form |
| Single | Chip            |



#### BENEFITS:

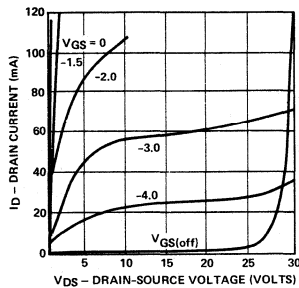
- Low Insertion Loss
- Small Error in Measurement Systems  
 $V_{DS(on)} < 50 \text{ mV}$  (2N5432)
- High Off-Isolation  $I_{D(off)} < 200 \text{ pA}$
- High Speed  $t_{d(on)} < 4 \text{ ns}$
- Low Noise Audio-Freq Amplification  
 $e_N < 2 \text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz

#### PRINCIPAL DEVICES

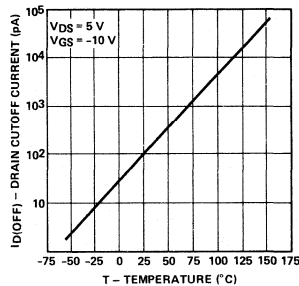
- U320-2
- 2N5432-34
- J108-10
- J108-18 -110-18
- All of the above devices

### PERFORMANCE CURVES (25°C unless otherwise noted)

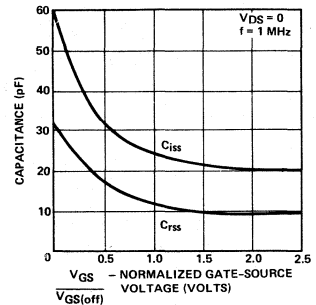
Output Characteristic



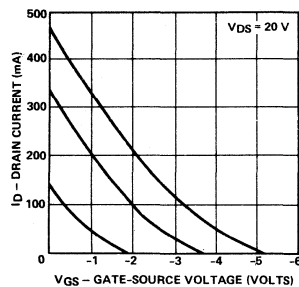
Drain Cutoff Current vs Ambient Temperature



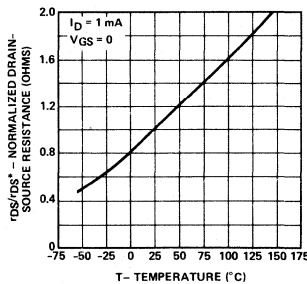
Common-Source Capacitance vs Normalized Gate-Source Voltage



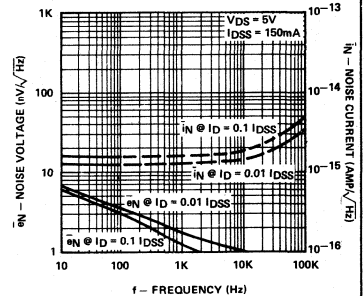
Transfer Characteristics



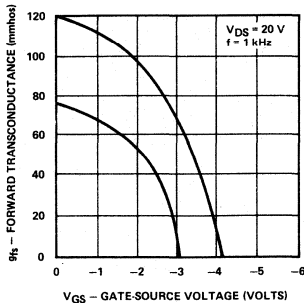
ON Resistance vs Ambient Temperature



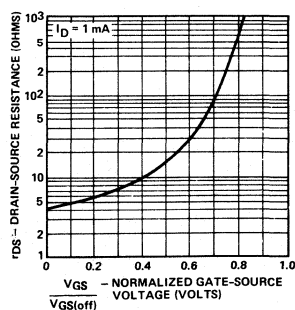
Equivalent Input Noise Voltage and Noise Current vs Frequency



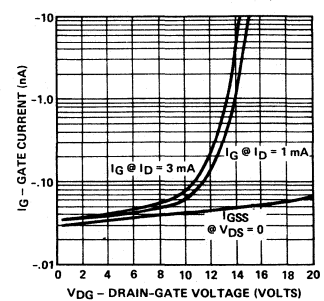
Forward Transconductance vs Drain Current



Resistance vs Normalized Gate-Source Voltage

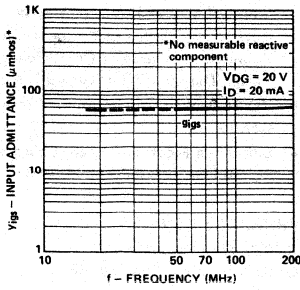


Gate Currents vs Drain-Gate Voltage

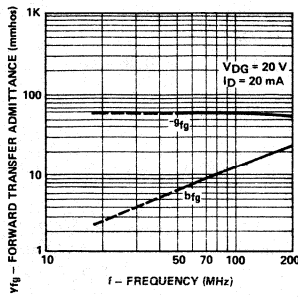


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

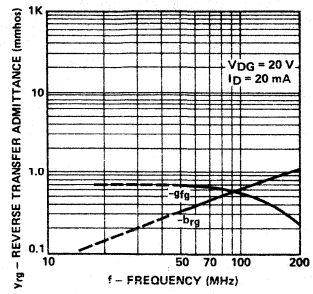
Input Admittance Common Gate vs Frequency



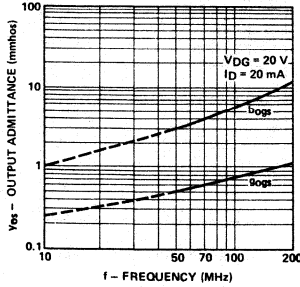
Forward Transfer Admittance Common Gate vs Frequency



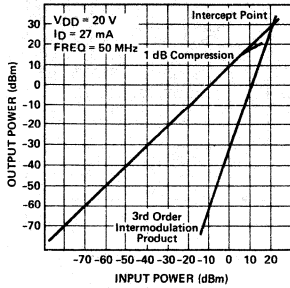
Reverse Transfer Admittance Common Gate vs Frequency



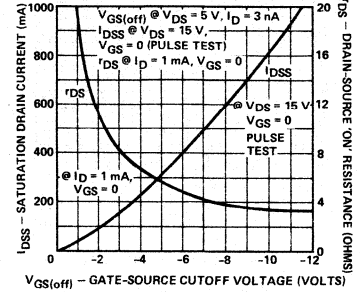
Output Admittance Common Gate vs Frequency

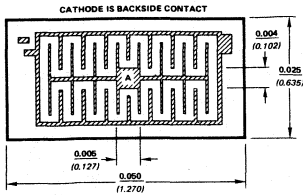


Gain - Intermodulation Characteristics



Drain Current & 'ON' Resistance vs Gate-Source Voltage





ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

## n-channel JFET current regulator diode designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

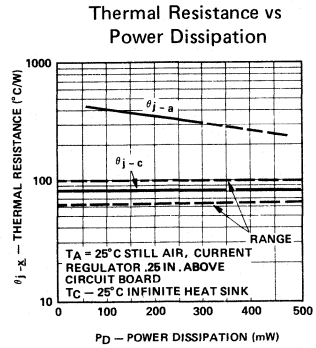
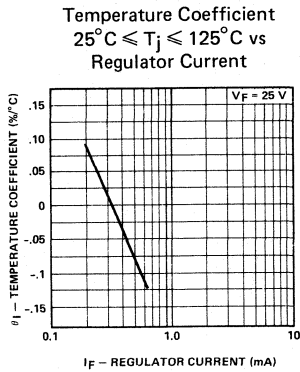
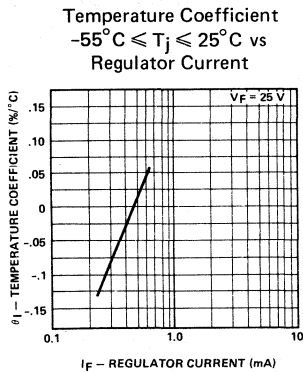
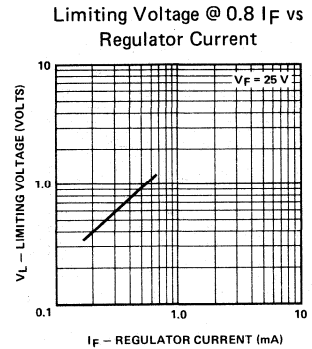
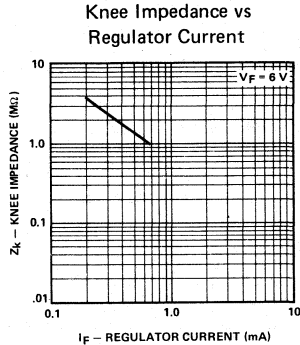
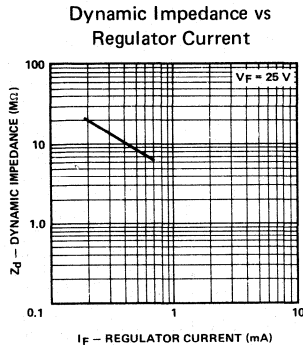
### BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

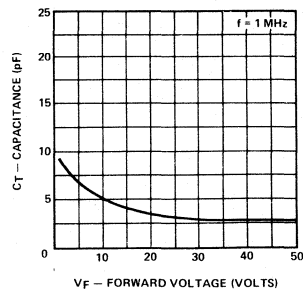
| TYPE   | PACKAGE        |
|--------|----------------|
| Single | TO-18 (2-lead) |
| Single | Chip           |

| PRINCIPAL DEVICES      |
|------------------------|
| CR022 Thru CR062, U508 |
| CR022CHP Thru CR062CHP |

## PERFORMANCE CURVES (25°C unless otherwise noted)



### Capacitance vs Forward Voltage



**NOTE:**  $I_F$ , Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature.  $I_F$  (steady state) =  $I_F \times [1 + \theta_I (T_j - 25^\circ\text{C})]$  where  $\theta_I$  is the temperature coefficient of  $I_F$  and  $T_j$  is the junction temperature.

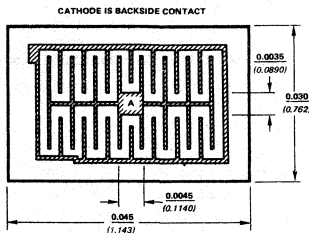
$T_j$  may be found by  $T_j = T_{\text{amb}} + \theta_{j-a}PD = T_{\text{case}} + \theta_{j-c}PD$ .  $T_j$  must not exceed 150°C.  $\frac{1}{\theta_{j-c}}$  or  $\frac{1}{\theta_{j-a}}$  is the derating factor for all devices.

# n-channel JFET current regulator diode designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

### BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required



ALL DIMENSIONS IN INCHES  
ALL DIMENSIONS IN MILLIMETERS

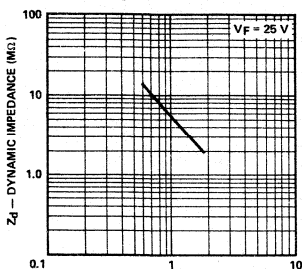
| TYPE   | PACKAGE        |
|--------|----------------|
| Single | TO-18 (2-lead) |
| Single | Chip           |

### PRINCIPAL DEVICES

CR068 Thru CR150  
CR068CHP Thru CR150CHP

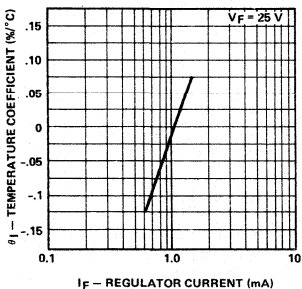
## PERFORMANCE CURVES (25°C unless otherwise noted)

Dynamic Impedance vs  
Regulator Current



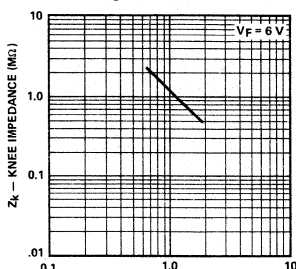
$I_F$  - REGULATOR CURRENT (mA)

Temperature Coefficient  
-55°C ≤ T<sub>j</sub> ≤ 25°C vs  
Regulator Current



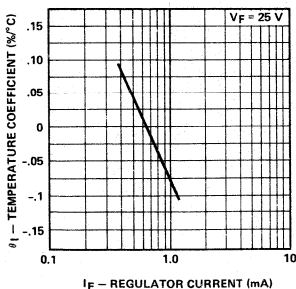
$I_F$  - REGULATOR CURRENT (mA)

Knee Impedance vs  
Regulator Current



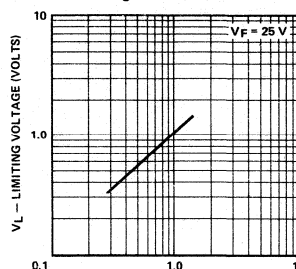
$I_F$  - REGULATOR CURRENT (mA)

Temperature Coefficient  
25°C ≤ T<sub>j</sub> ≤ 125°C vs  
Regulator Current



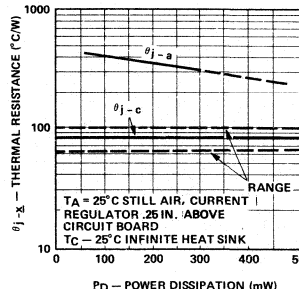
$I_F$  - REGULATOR CURRENT (mA)

Limiting Voltage @ 0.8 I<sub>F</sub> vs  
Regulator Current



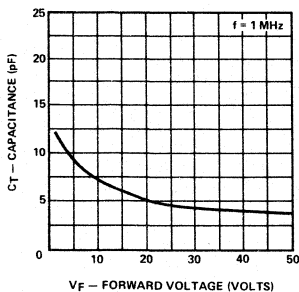
$I_F$  - REGULATOR CURRENT (mA)

Thermal Resistance vs  
Power Dissipation



$P_D$  - POWER DISSIPATION (mW)

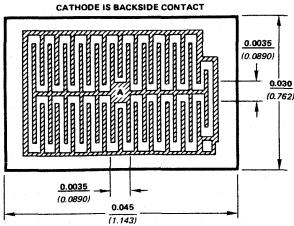
Capacitance vs Forward Voltage



$V_F$  - FORWARD VOLTAGE (VOLTS)

NOTE:  $I_F$ , Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature.  $I_F$  (steady state) =  $I_F \times [1 + \theta_1 (T_j - 25^\circ\text{C})]$  where  $\theta_1$  is the temperature coefficient of  $I_F$  and  $T_j$  is the junction temperature.

$T_j$  may be found by  $T_j = T_{amb} + \theta_{j-a}P_D = T_{case} + \theta_{j-c}P_D$ .  $T_j$  must not exceed 150°C.  $\frac{1}{\theta_{j-c}}$  or  $\frac{1}{\theta_{j-a}}$  is the derating factor for all devices.



ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

## n-channel JFET current regulator diode designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

### BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

### TYPE

Single  
Single

### PACKAGE

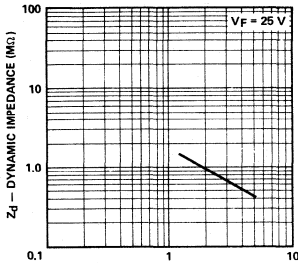
TO-18 (2-lead)  
Chip

### PRINCIPAL DEVICES

CR160 Thru CR470  
CR160CHP Thru CR470CHP

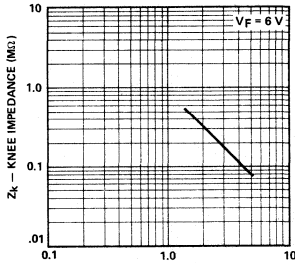
## PERFORMANCE CURVES (25°C unless otherwise noted)

Dynamic Impedance vs  
Regulator Current



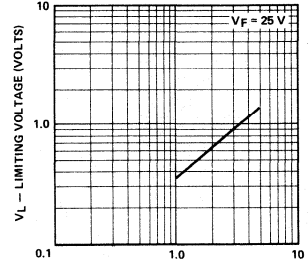
$I_F$  - REGULATOR CURRENT (mA)

Knee Impedance vs  
Regulator Current



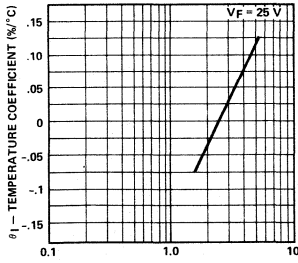
$I_F$  - REGULATOR CURRENT (mA)

Limiting Voltage @ 0.8 If vs  
Regulator Current



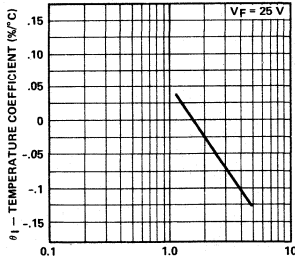
$I_F$  - REGULATOR CURRENT (mA)

Temperature Coefficient  
-55°C ≤ Tj ≤ 25°C vs  
Regulator Current



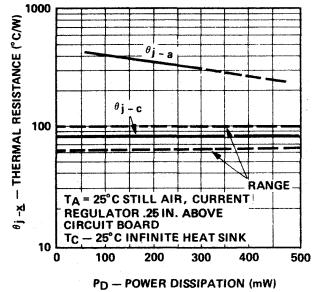
$I_F$  - REGULATOR CURRENT (mA)

Temperature Coefficient  
25°C ≤ Tj ≤ 125°C vs  
Regulator Current

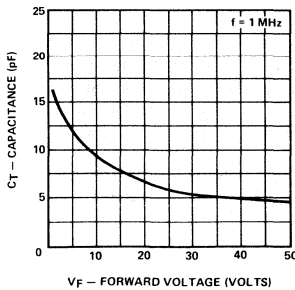


$I_F$  - REGULATOR CURRENT (mA)

Thermal Resistance vs  
Power Dissipation



Capacitance vs Forward Voltage



$V_F$  - FORWARD VOLTAGE (VOLTS)

NOTE:  $I_F$ , Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature.  $I_F$  (steady state) =  $I_F \times [1 + \theta_I (T_j - 25^\circ\text{C})]$  where  $\theta_I$  is the temperature coefficient of  $I_F$  and  $T_j$  is the junction temperature.

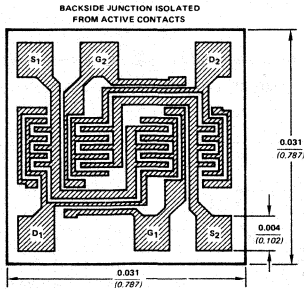
$T_j$  may be found by  $T_j = T_{\text{amb}} + \theta_{j-a} P_D = T_{\text{case}} + \theta_{j-c} P_D$ .  $T_j$  must not exceed 150°C.  $\frac{1}{\theta_{j-c}}$  or  $\frac{1}{\theta_{j-a}}$  is the derating factor for all devices.

**monolithic  
dual n-channel JFET  
designed for . . .**

- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

**BENEFITS:**

- Minimum System Error and Calibration  
5 mV Offset Maximum (2N5196)
- Low Drift With Temperature  
5  $\mu\text{V}/^\circ\text{C}$  Maximum (2N5196)



ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

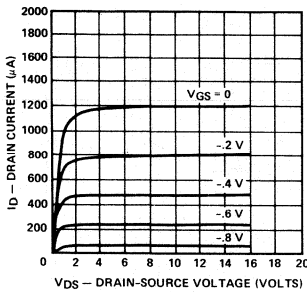
| TYPE | PACKAGE |
|------|---------|
| Dual | TO-71   |
| Dual | Chip    |

**PRINCIPAL DEVICES**

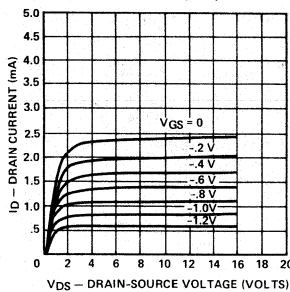
- 2N5196-9, 2N5545-47, U231-35
- 2N5199CHP, U232CHP-35CHP
- 2N5547CHP

**PERFORMANCE CURVES (25°C unless otherwise noted)**

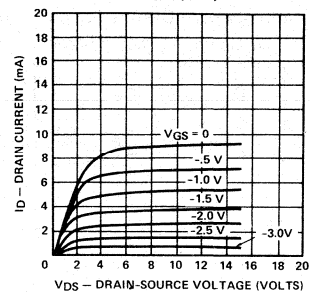
**Output Characteristics  
Low  $V_{GS(off)}$  Unit**



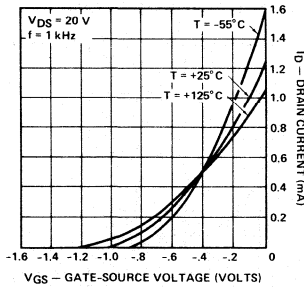
**Output Characteristics  
Medium  $V_{GS(off)}$  Unit**



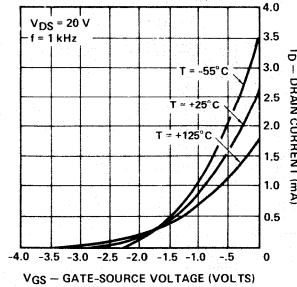
**Output Characteristics  
High  $V_{GS(off)}$  Unit**



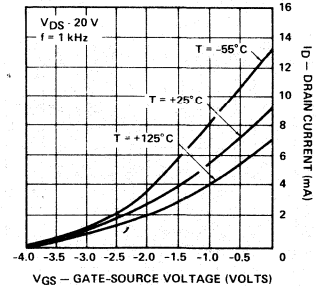
**Transfer Characteristics  
Low  $V_{GS(off)}$**



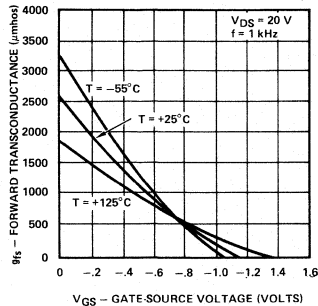
**Transfer Characteristics  
Medium  $V_{GS(off)}$**



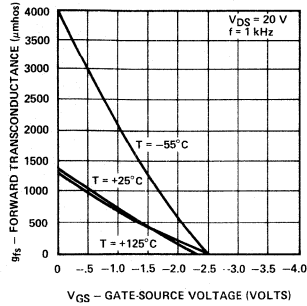
**Transfer Characteristics  
High  $V_{GS(off)}$**



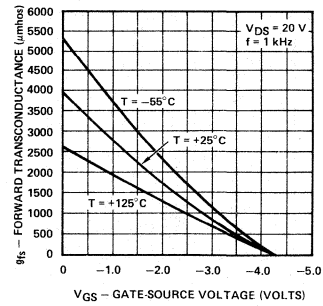
**Transconductance Characteristics  
Low  $V_{GS(off)}$**



**Transconductance Characteristics  
Medium  $V_{GS(off)}$**

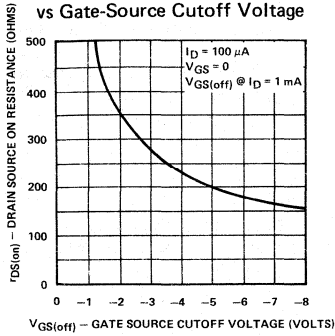


**Transconductance Characteristics  
High  $V_{GS(off)}$**

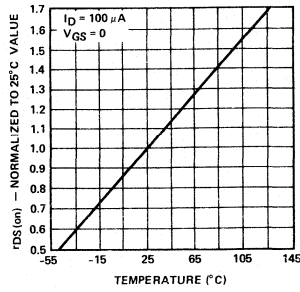


**PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)**

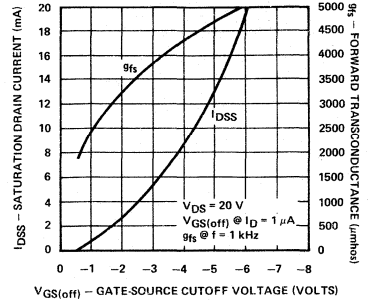
**Static Drain-Source ON Resistance vs Gate-Source Cutoff Voltage**



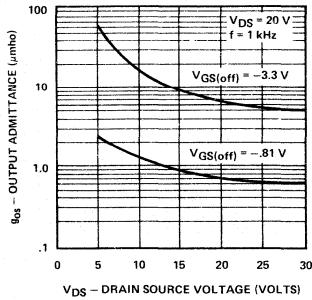
**Normalized ON Resistance vs Ambient Temperature**



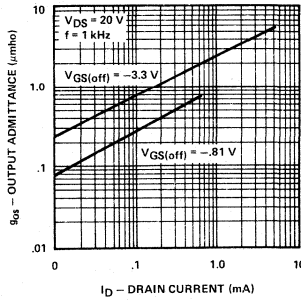
**IDSS and gfs vs Gate-Source Cutoff Voltage**



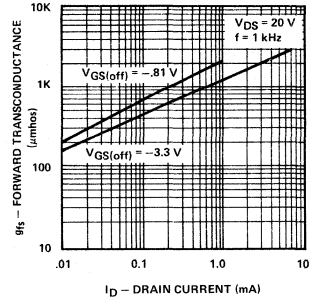
**Common-Source Output Conductance vs Drain-Source Voltage**



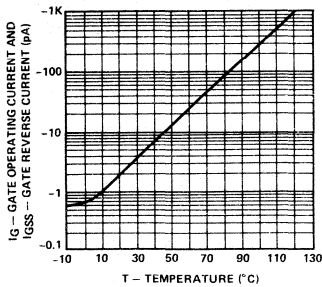
**Common-Source Output Conductance vs Drain Current**



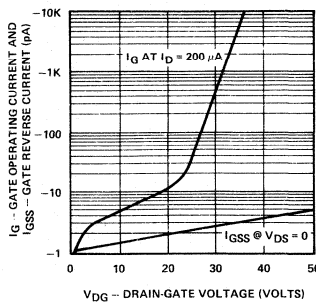
**Forward Transconductance vs Drain Current**



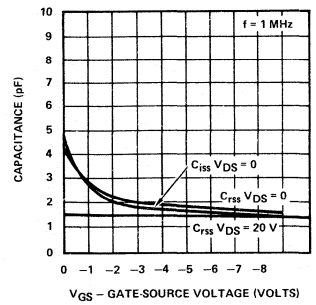
**Gate Leakage Currents vs Ambient Temperature**



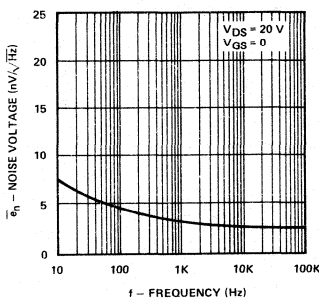
**Gate Leakage Currents vs Drain-Gate Voltage**



**Capacitance vs Gate-Source Voltage**



**Equivalent Input Noise Voltage vs Frequency**



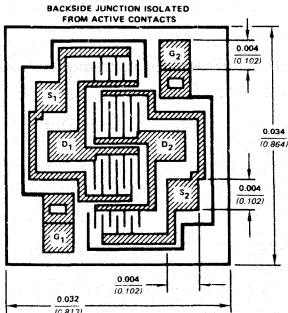


# monolithic dual n-channel JFET designed for . . .

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

**BENEFITS:**

- Minimum System Error and Calibration  
5 mV Offset Maximum (J401)  
95 dB Minimum CMRR
- Low Drift With Temperature  
10  $\mu\text{V}/^\circ\text{C}$  (J401)
- Simplifies Amplifier Design  
Output Conductance < 2  $\mu\text{mho}$
- Low Noise  
 $\bar{e}_n = 6 \text{ nV}/\sqrt{\text{Hz}}$  at 10 Hz Typical



ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

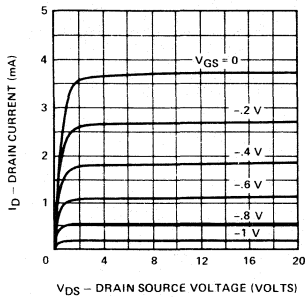
| TYPE | PACKAGE |
|------|---------|
| Dual | TO-71   |
| Dual | Chip    |

**PRINCIPAL DEVICES**

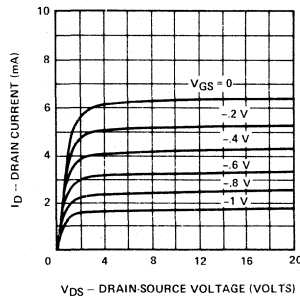
2N3921-2, 2N4084-5, 2N5045-7, U401-6  
2N4085CHP, 2N5046CHP-47CHP,  
U403CHP-06CHP

**PERFORMANCE CURVES (25°C unless otherwise noted)**

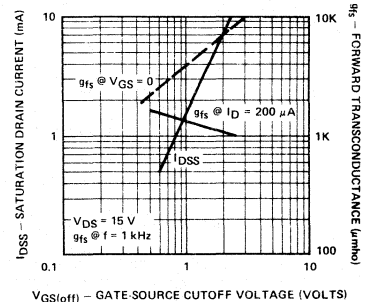
Output Characteristics  
Low  $V_{GS(off)}$  Unit (-1.5 V)



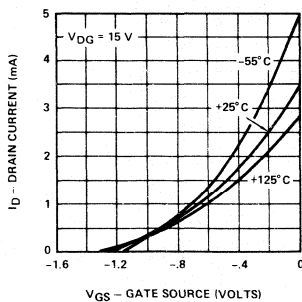
Output Characteristics  
Medium  $V_{GS(off)}$  Unit (-2.2 V)



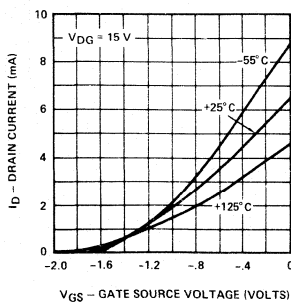
Drain Current and Transconductance vs  
Gate-Source Cutoff Voltage



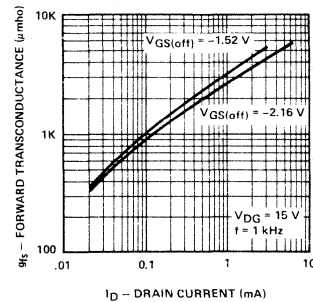
Transfer Characteristics  
Low  $V_{GS(off)}$  Unit (-1.5 V)



Transfer Characteristics  
Medium  $V_{GS(off)}$  Unit (-2.2 V)



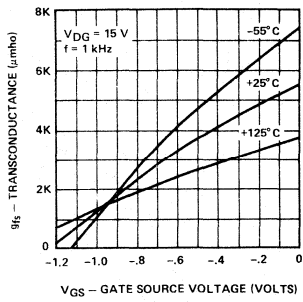
Forward Transconductance  
vs Drain Current



PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

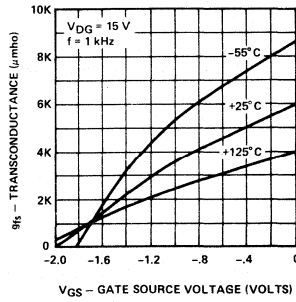
Transconductance vs Gate Source Voltage

Low  $V_{GS(off)}$  Unit (-1.5 V)

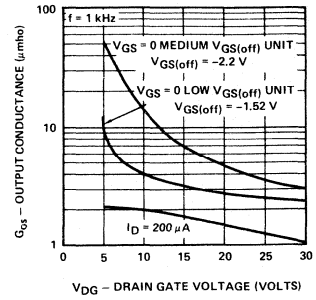


Transconductance vs Gate Source Voltage

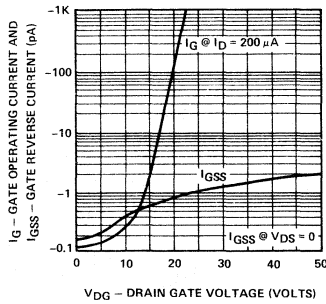
Medium  $V_{GS(off)}$  Unit (-2.2 V)



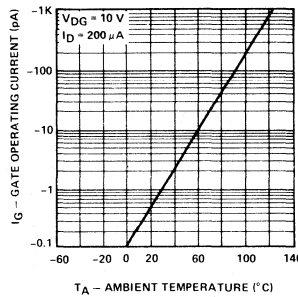
Output Conductance vs Drain Gate Voltage



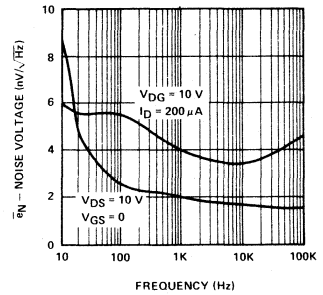
Gate Operating Current vs Drain Gate Voltage



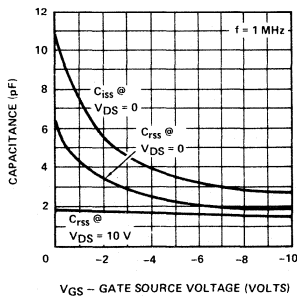
Gate Operating Current vs Ambient Temperature



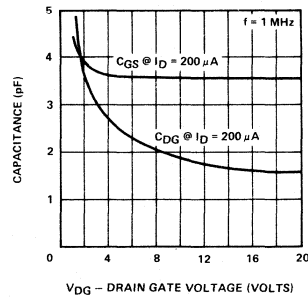
Equivalent Short Circuit Input Noise vs Frequency



Capacitance vs Gate Source Voltage



Capacitance vs Drain to Gate Voltage



### n-channel JFET designed for . . .

- Small Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

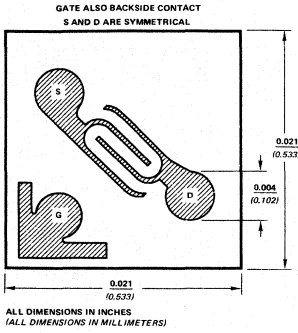
**BENEFITS:**

- Low Noise NF < 1 dB at 1 kHz
- Operation From Low Power Supply Voltages,  $V_{GS(off)} < 1 V$  (2N4338)
- High Off-Isolation As A Switch  $I_{D(off)} < 50 pA$
- High Input Impedance

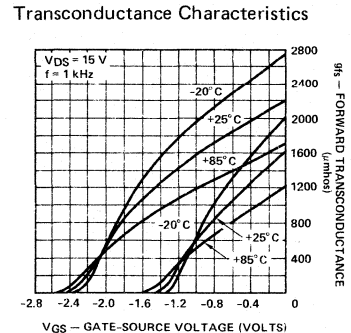
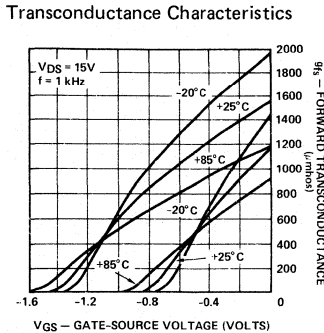
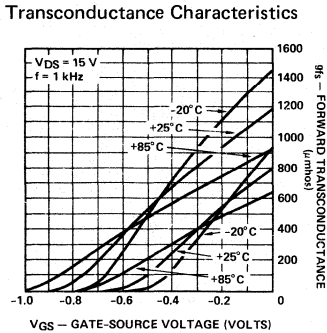
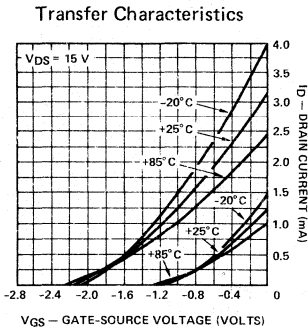
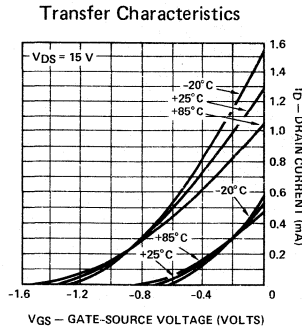
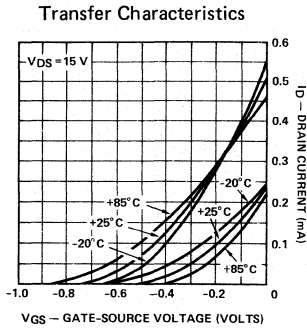
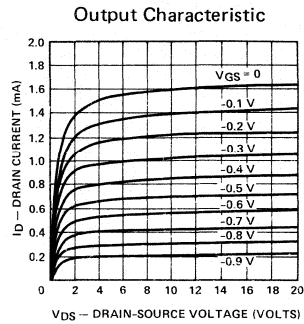
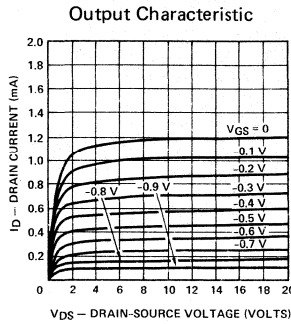
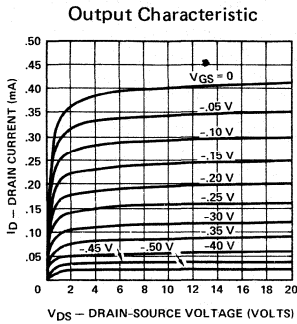
**PRINCIPAL DEVICES**

- 2N3368-70, 2N3436-8, 2N3458-60, 2N4338-41, VCR4N  
2N5196-9, U231-5, 2N5545-47  
J201-203, J204, PN4302-04  
J201-18 - 203-18, J204-18,  
All of the above  
PN4302-18 - 4304-18

| TYPE   | PACKAGE         |
|--------|-----------------|
| Single | TO-18           |
| Dual   | TO-71           |
| Single | TO-92           |
| Single | TO-92 Lead-form |
| Single | Chip            |

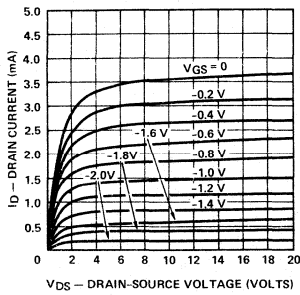


**PERFORMANCE CURVES (25°C unless otherwise noted)**

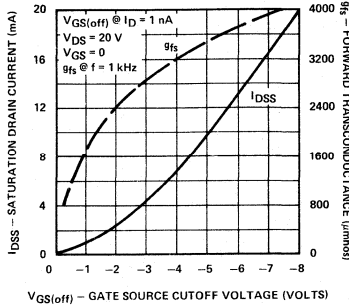


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

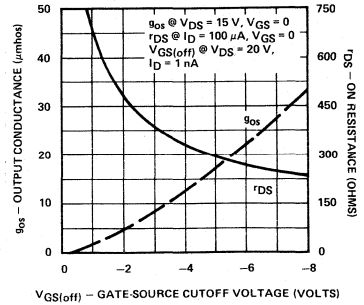
Output Characteristic



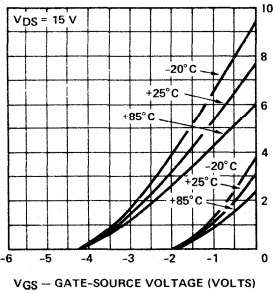
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



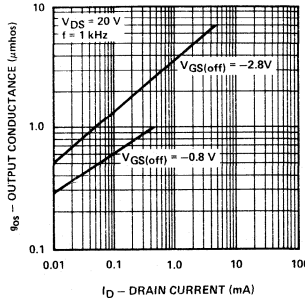
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



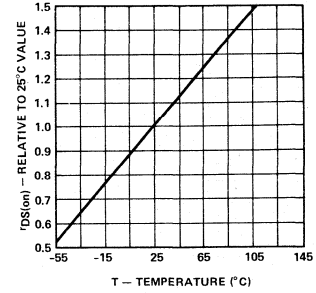
Transfer Characteristics



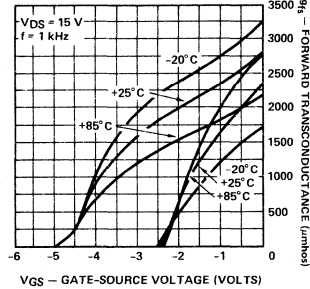
Common-Source Output Conductance vs Drain Current



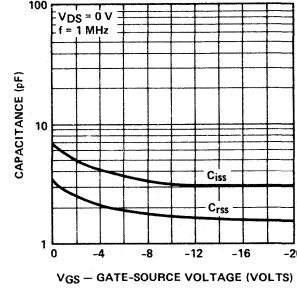
ON Resistance vs Ambient Temperature



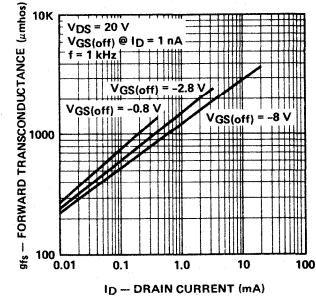
Transconductance Characteristics



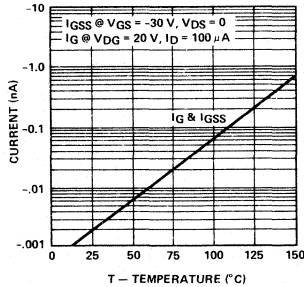
Common-Source Capacitances vs Gate-Source Voltage



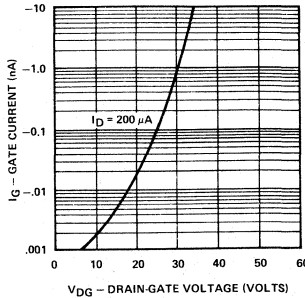
Common-Source Forward Transconductance vs Drain Current



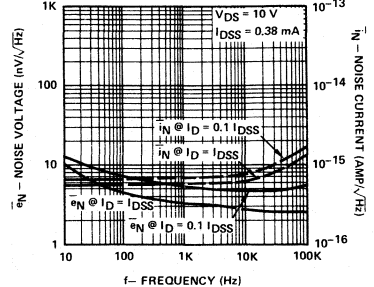
Gate Currents vs Ambient Temperature



Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency



# monolithic dual n-channel JFET designed for . . .

■ General Purpose Differential Amplifiers

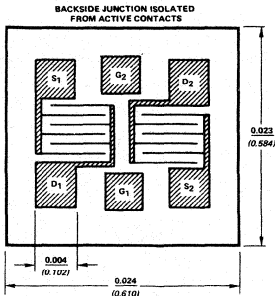
**BENEFITS:**

- Low Cost
- High Input Impedance

| TYPE | PACKAGE |
|------|---------|
| Dual | TO-71   |
| Dual | Chip    |

**PRINCIPAL DEVICES**

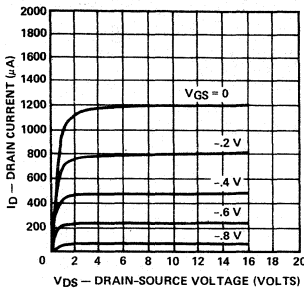
U410-12  
U411CHP, U412CHP



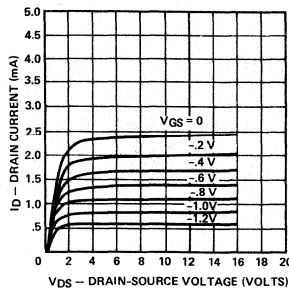
ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

## PERFORMANCE CURVES (25°C unless otherwise noted)

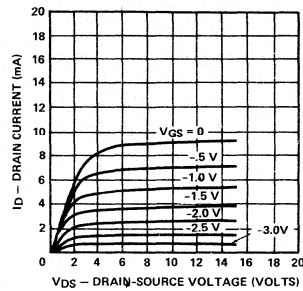
Output Characteristics  
Low  $V_{GS(off)}$  Unit



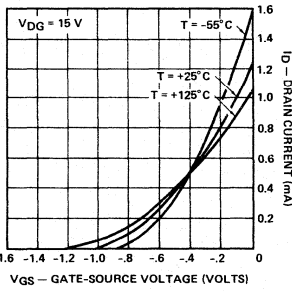
Output Characteristics  
Medium  $V_{GS(off)}$  Unit



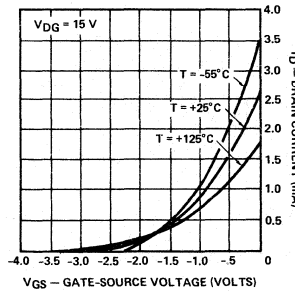
Output Characteristics  
High  $V_{GS(off)}$  Unit



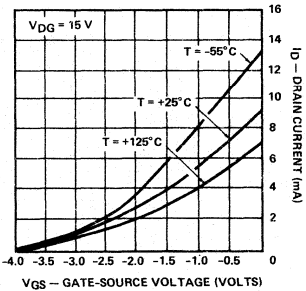
Transfer Characteristics  
Low  $V_{GS(off)}$



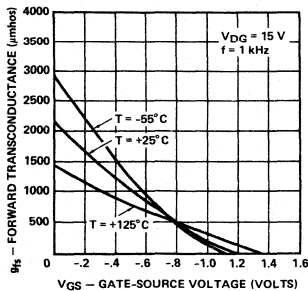
Transfer Characteristics  
Medium  $V_{GS(off)}$



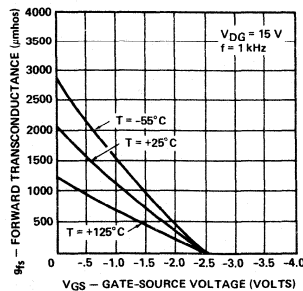
Transfer Characteristics  
High  $V_{GS(off)}$



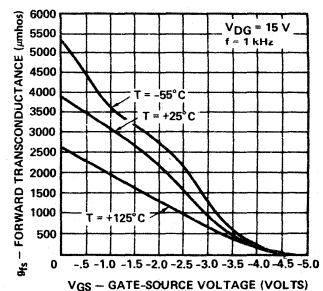
Transconductance Characteristics  
Low  $V_{GS(off)}$



Transconductance Characteristics  
Medium  $V_{GS(off)}$

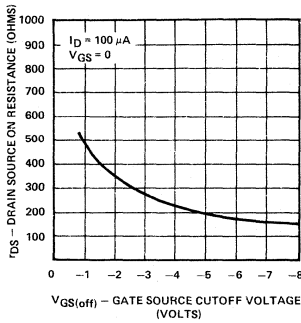


Transconductance Characteristics  
High  $V_{GS(off)}$

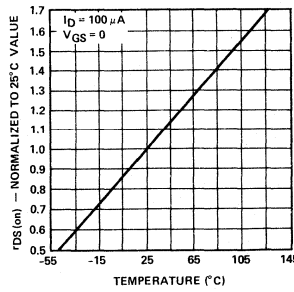


**PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)**

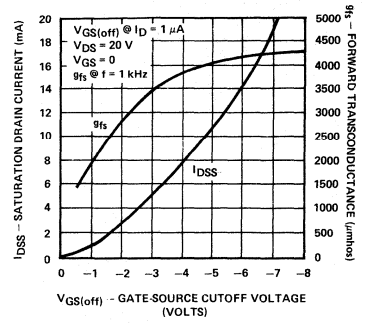
**Static Drain-Source ON Resistance vs Gate-Source Cutoff Voltage**



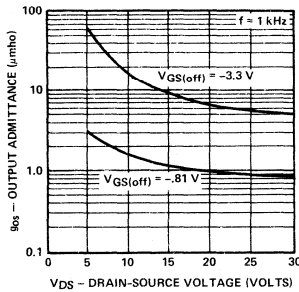
**Normalized ON Resistance vs Ambient Temperature**



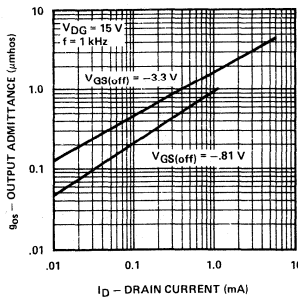
**I<sub>DSS</sub> and g<sub>fs</sub> vs Gate-Source Cutoff Voltage**



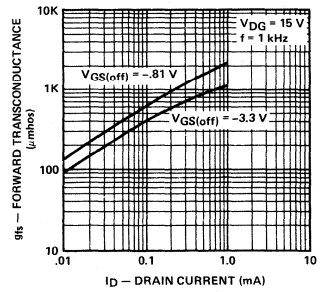
**Common Source Output Admittance vs Drain-Source Voltage**



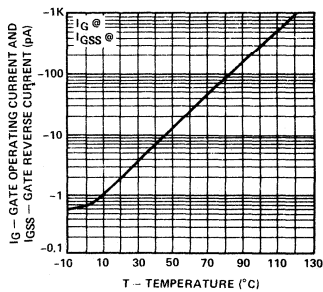
**Common-Source Output Conductance vs Drain Current**



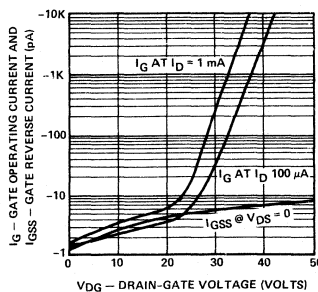
**Common Source Forward Transconductance vs Drain Current**



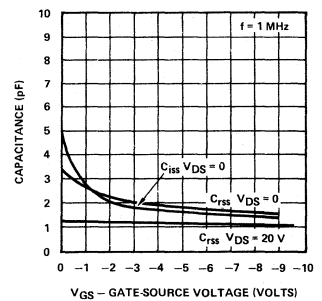
**Leakage Current vs Ambient Temperature**



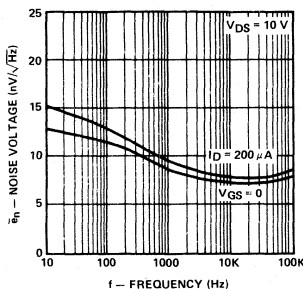
**Gate Operating Current vs Drain-Gate Voltage**



**Capacitance vs Gate-Source Voltage**



**Equivalent Input Noise Voltage vs Frequency**



# monolithic dual n-channel JFETs designed for . . .

- Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

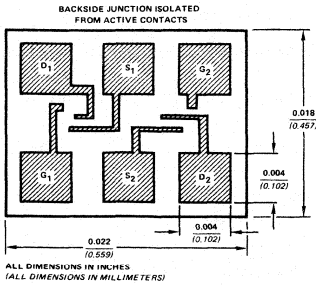
| TYPE | PACKAGE |
|------|---------|
| Dual | TO-78   |
| Dual | Chip    |

### BENEFITS:

- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

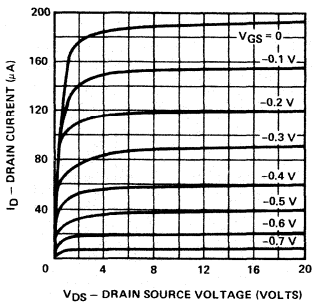
### PRINCIPAL DEVICES

- U421-6
- U422CHP, U423CHP, U425CHP, U426CHP

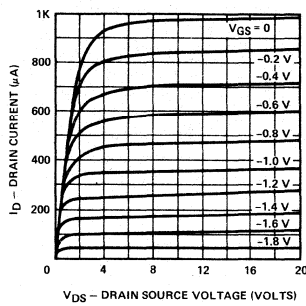


## PERFORMANCE CURVES (25°C unless otherwise noted)

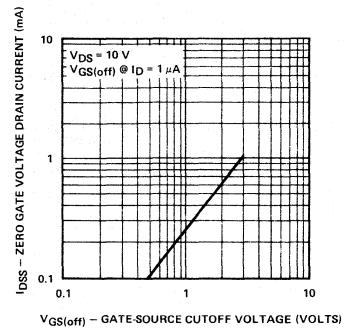
Output Characteristics  
Low  $V_{GS(off)}$  Unit (1.0 V)



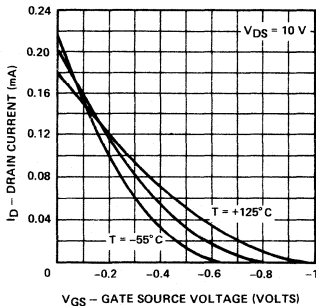
Output Characteristics  
High  $V_{GS(off)}$  Unit (2.5 V)



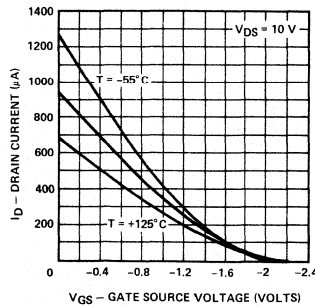
$I_{DSS}$  vs Gate Source Cutoff Voltage



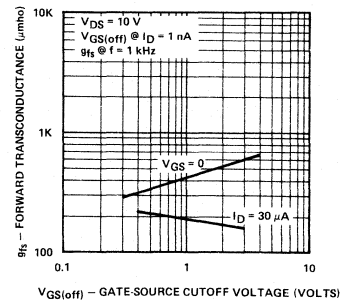
Transfer Characteristics  
Low  $V_{GS(off)}$  Unit (1.0 V)



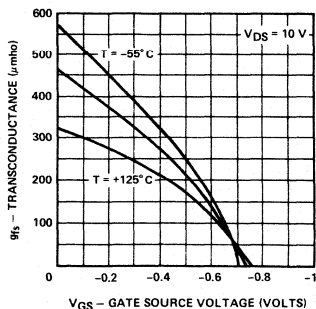
Transfer Characteristics  
High  $V_{GS(off)}$  Unit (2.5 V)



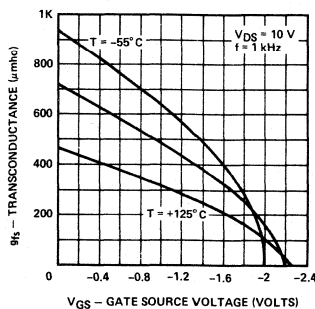
Forward Transconductance vs Gate Source Cutoff Voltage



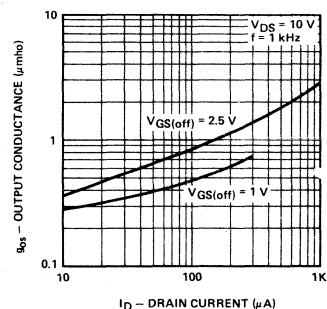
Transconductance vs Gate Source Voltage  
Low  $V_{GS(off)}$  Unit (1.0 V)



Transconductance vs Gate Source Voltage  
High  $V_{GS(off)}$  Unit (2.5 V)

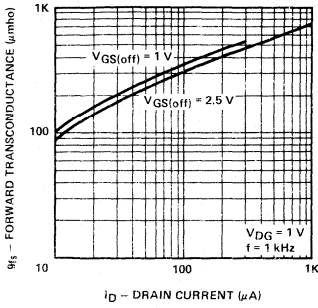


Common-Source Output Conductance vs Drain Current

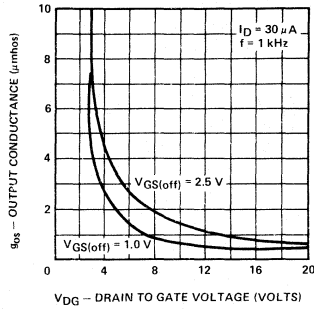


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

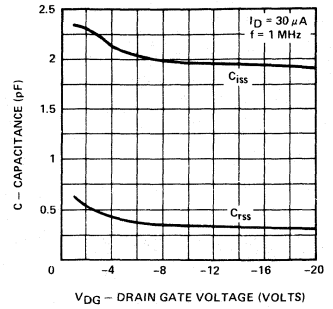
Forward Transconductance vs Drain Current



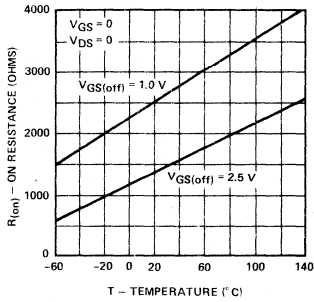
Output Conductance vs Drain to Gate Voltage



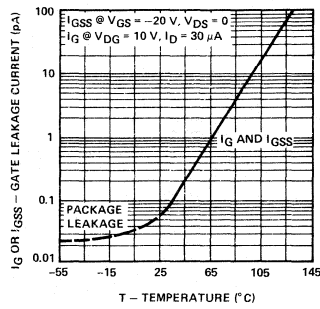
Capacitance vs Drain Gate Voltage



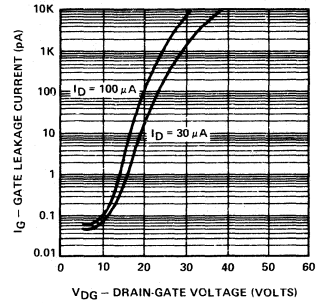
On Resistance vs Ambient Temperature



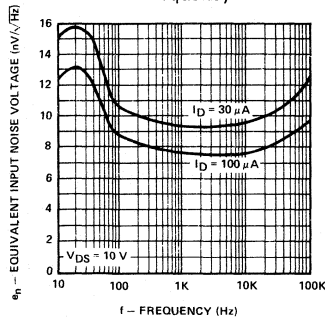
Leakage Current vs Temperature



Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency







### n-channel JFET designed for . . .

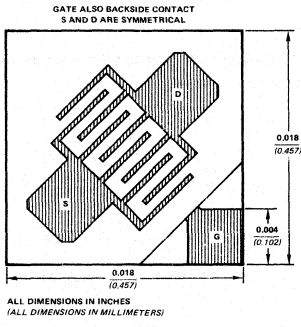
- Small Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers
- Switches

**BENEFITS:**

- Wide Input Dynamic Range  
High  $I_G$  Breakpoint Voltage
- High Gain
- Low Insertion Loss Switches

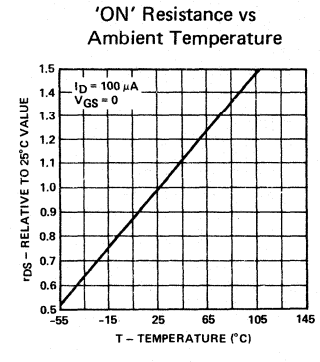
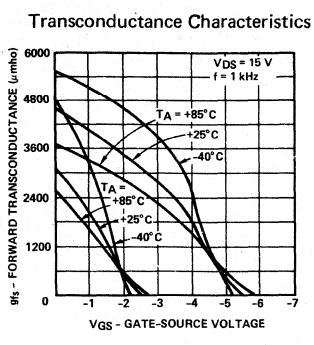
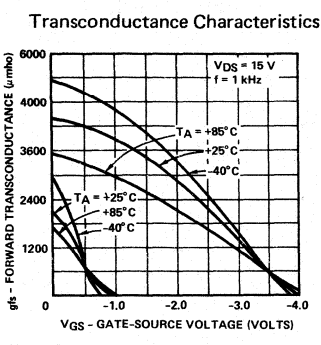
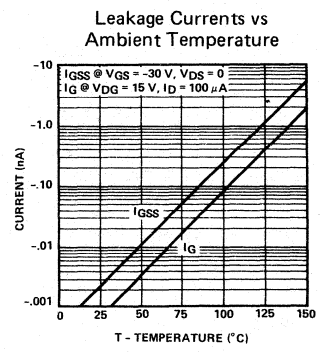
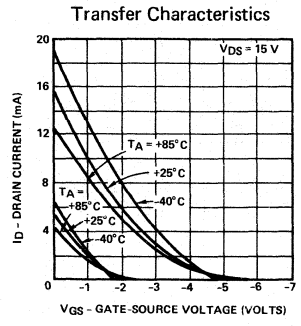
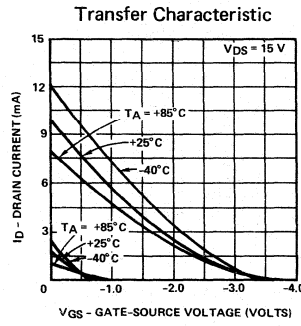
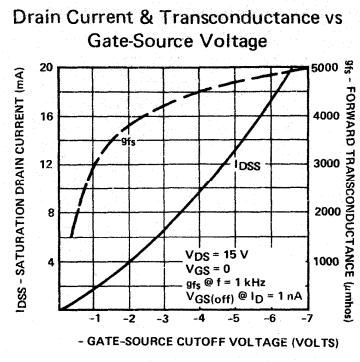
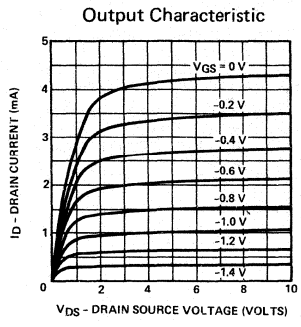
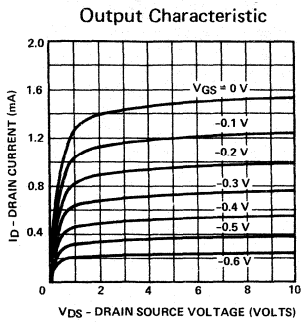
**PRINCIPAL DEVICES**

2N3821-4, 2N4220-2, 2N4220A-22A  
 2N4223-24, 2N5556-58  
 2N3819, 2N5457-9, MPF109, MPF111  
 2N3921-2, 2N4084-5, 2N5045-7, U401-8  
 All of the above except 2N3819



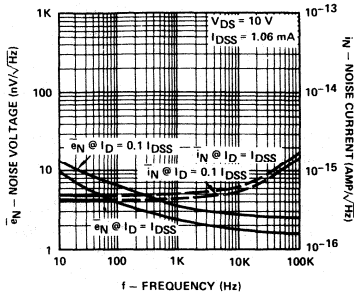
| TYPE   | PACKAGE |
|--------|---------|
| Single | TO-72   |
| Single | TO-92   |
| Dual   | TO-71   |
| Single | Chip    |

**PERFORMANCE CURVES (25°C unless otherwise noted)**

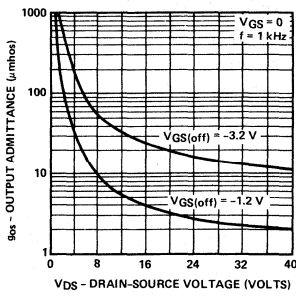


PERFORMANCE CURVES (Con't) (25° C unless otherwise noted)

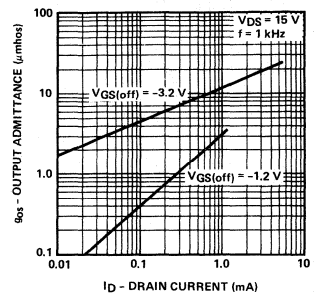
Equivalent Input Noise Voltage and Noise Current vs Frequency



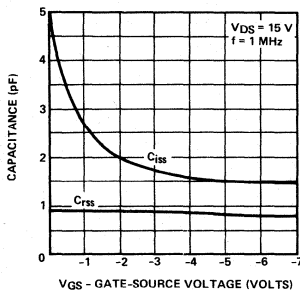
Common-Source Output Admittance vs Drain-Source Voltage



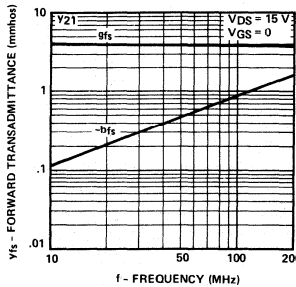
Common-Source Output Admittance vs Drain Current



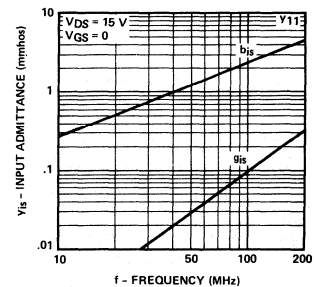
Common-Source Capacitances vs Gate-Source Voltage



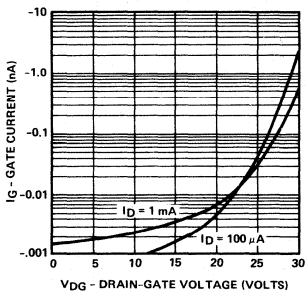
Common-Source Forward Transadmittance vs Frequency



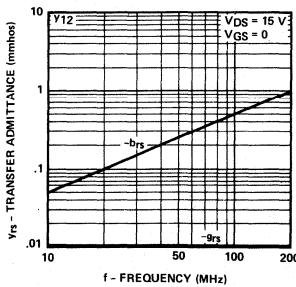
Common-Source Input Admittance vs Frequency



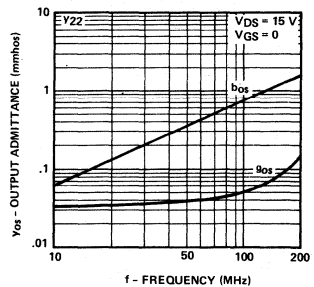
Gate Operating Current vs Drain-Gate Voltage



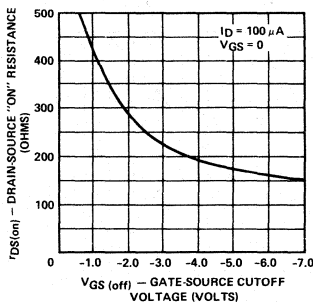
Common-Source Reverse Transfer Admittance vs Frequency



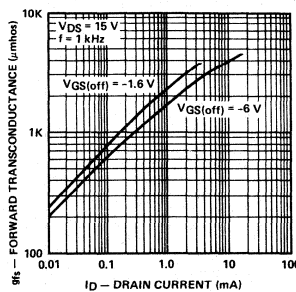
Common-Source Output Admittance vs Frequency



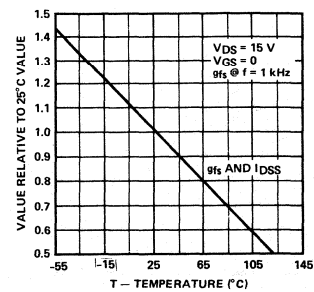
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



Common-Source Forward Transconductance vs Drain Current



Drain Current and Transconductance vs Ambient Temperature





### n-channel JFET designed for . . .

- Low Noise Amplifiers
- Single and Differential Amplifiers

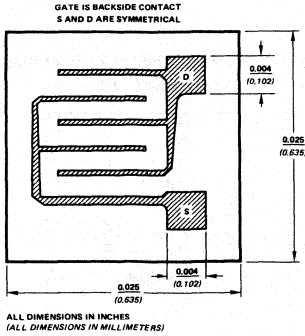
#### BENEFITS:

- Simplifies Amplifier Design
- Low Output Conductance
- Low 1/f Noise

| TYPE   | PACKAGE         |
|--------|-----------------|
| Dual   | TO-71           |
| Single | TO-72           |
| Single | TO-92           |
| Single | TO-92 Lead-form |
| Dual   | Chip            |
| Single | Chip            |

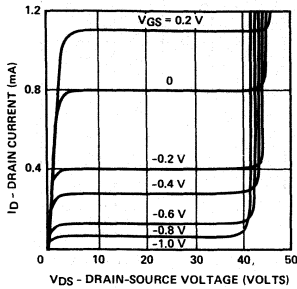
#### PRINCIPAL DEVICES

2N5515-24  
 2N4867-9, 2N4867A-69A  
 J230-32  
 J230-18 - 232-18  
 2N5518CHP-9CHP, 2N5523CHP-4CHP  
 All of the above single devices

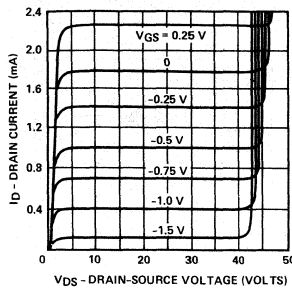


### PERFORMANCE CURVES (25°C unless otherwise noted)

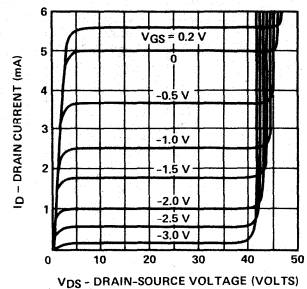
#### Output Characteristics



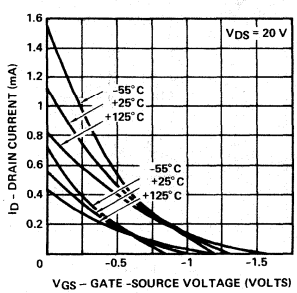
#### Output Characteristics



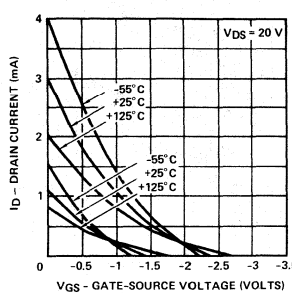
#### Output Characteristics



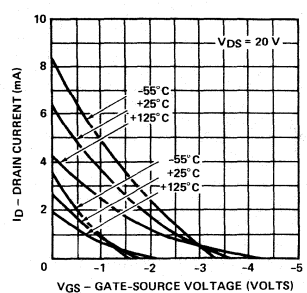
#### Transfer Characteristics



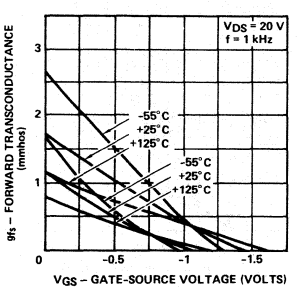
#### Transfer Characteristics



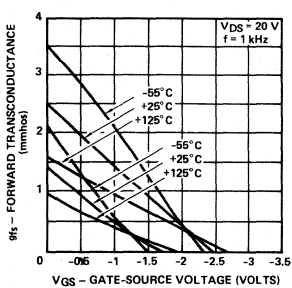
#### Transfer Characteristics



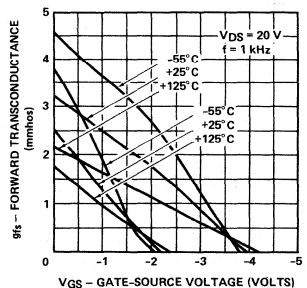
#### Transconductance Characteristics



#### Transconductance Characteristics

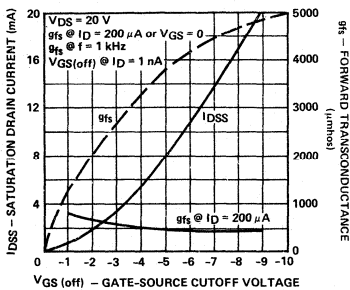


#### Transconductance Characteristics

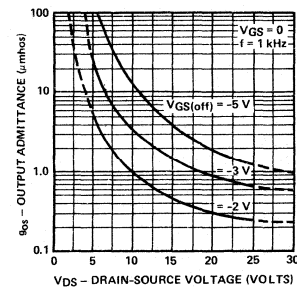


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

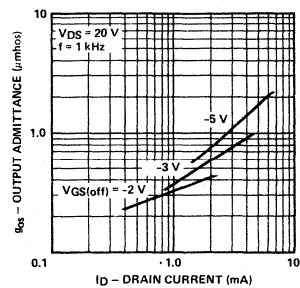
Saturation Drain Current and Forward Transconductance vs. Gate-Source Cutoff Voltage



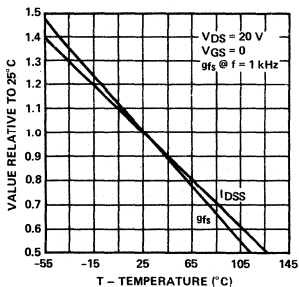
Common-Source Output Conductance vs Drain-Source Voltage



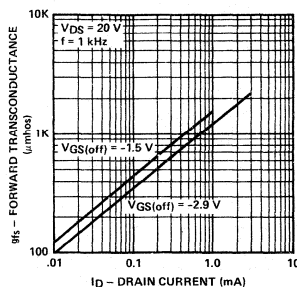
Common-Source Output Conductance vs Drain Current



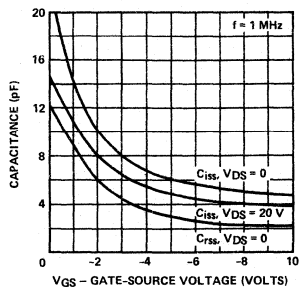
Drain Current & Transconductance vs Ambient Temperature



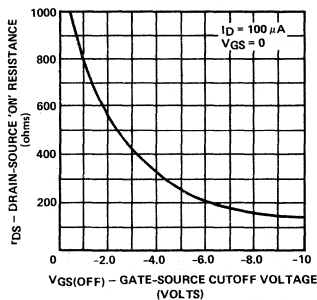
Common-Source Forward Transconductance vs Drain Current



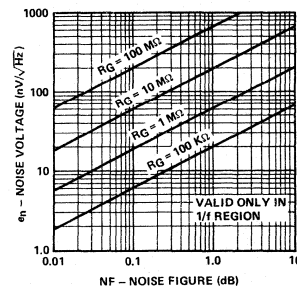
Common-Source Capacitance vs Gate-Source Voltage



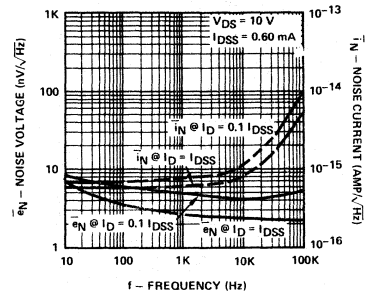
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



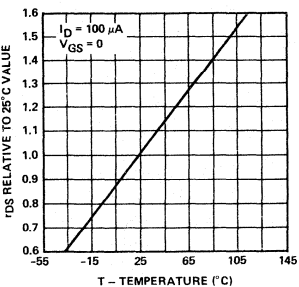
Approximate Noise Figure vs Input Noise Voltage



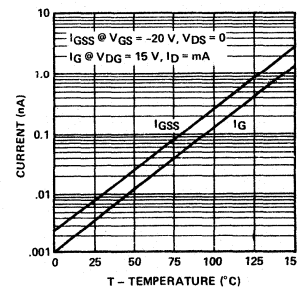
Equivalent Input Noise Voltage and Noise Current vs Frequency



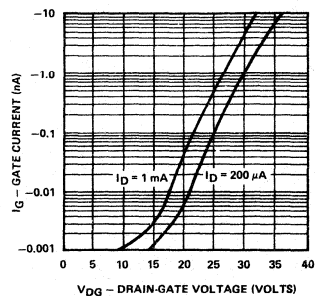
Drain-Source 'ON' Resistance vs Ambient Temperature



Leakage Currents vs Ambient Temperature



Gate Operating Current vs Drain-Gate Voltage



# n-channel JFET designed for . . .

- Ultra-High Input Impedance Amplifiers
- Electrometers
- pH Meters
- Smoke Detectors

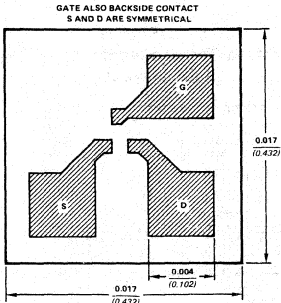
### BENEFITS:

- Low Power  
 $I_{DSS} < 90 \mu A$  (2N4117)
- High Input Impedance  
 $I_G < 1 pA$  (2N5906-09)

| TYPE   | PACKAGE |
|--------|---------|
| Single | TO-72   |
| Dual   | TO-78   |
| Single | Chip    |
| Dual   | Chip    |

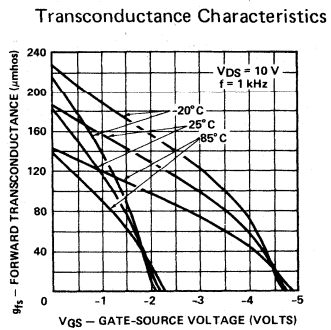
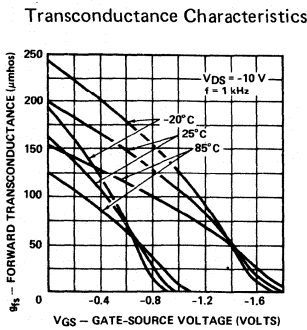
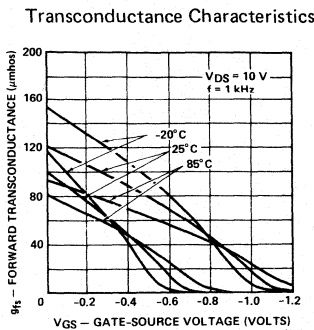
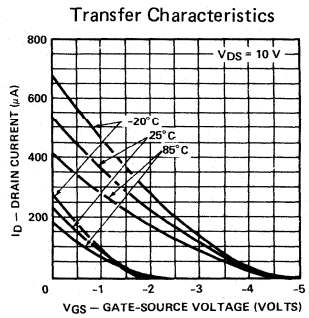
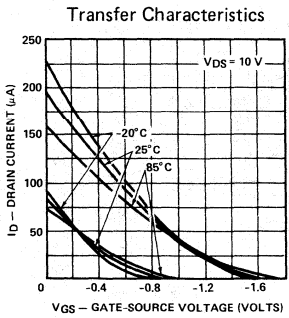
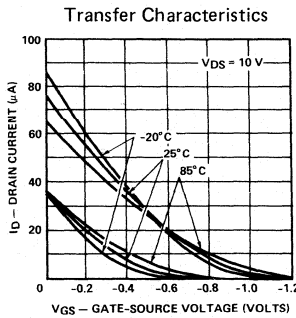
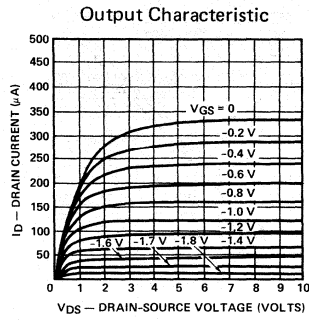
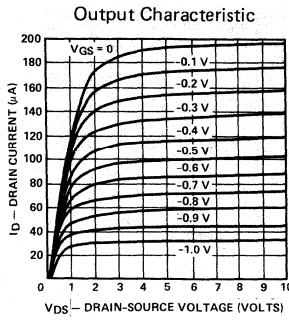
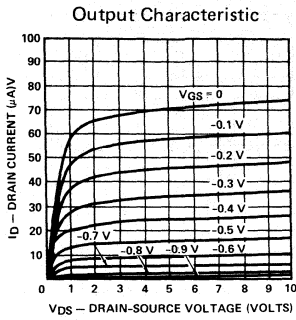
### PRINCIPAL DEVICES

- 2N4117-9, 2N4117A-9A, VCR7N
- 2N5902-9
- 2N4117CHP-9CHP, 2N4117ACHP-9ACHP, VCR7NCHP
- 2N5905CHP, 2N5909CHP



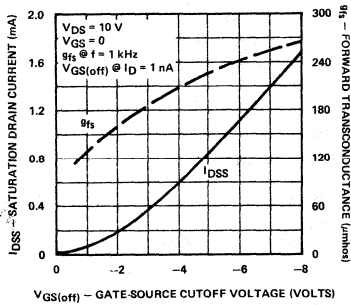
ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

## PERFORMANCE CURVES (25°C unless otherwise noted)

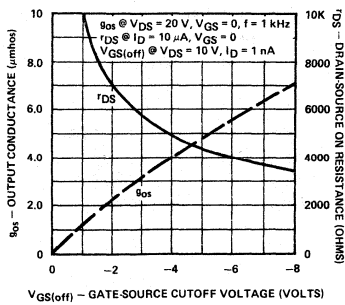


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

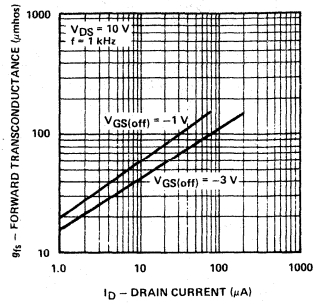
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



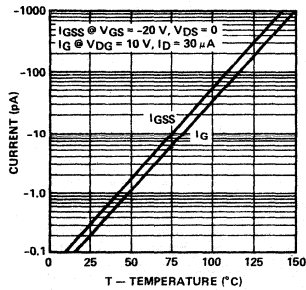
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



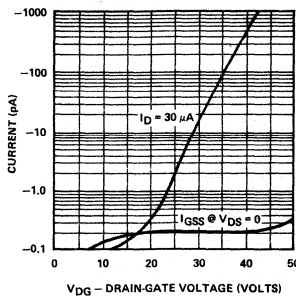
Common-Source Forward Transconductance vs Drain Current



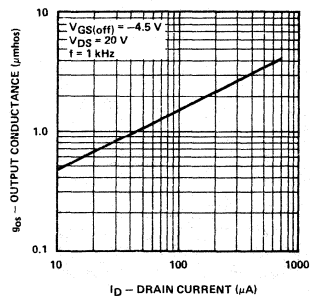
Leakage Currents vs Ambient Temperature



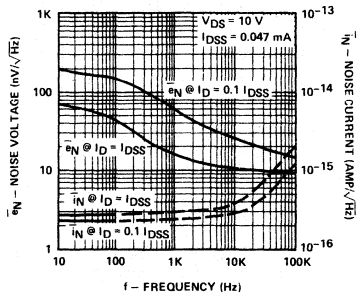
Leakage Currents vs Drain-Gate Voltage



Common-Source Output Conductance vs Drain Current



Equivalent Input Noise Voltage and Noise Current vs Frequency



### n-channel JFET designed for . . .

- Analog Switches
- Commutators
- Choppers

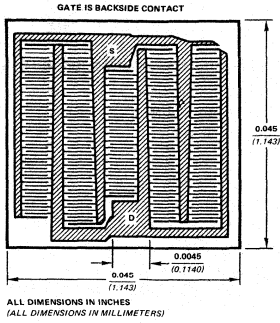
**BENEFITS:**

- Very Low Insertion Loss  
 $R_{DS(on)} < 2.5 \text{ Ohms (U290)}$
- High Off-Isolation

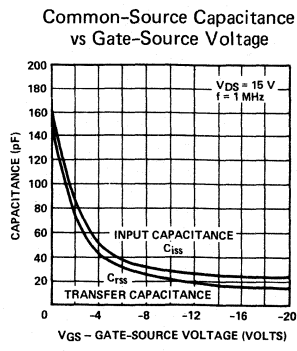
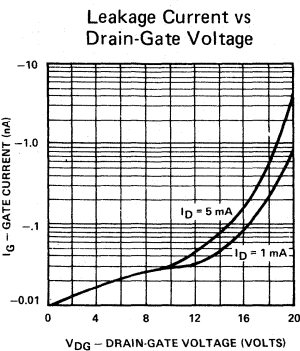
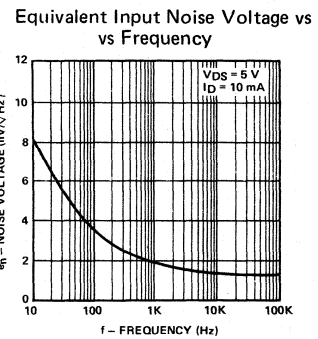
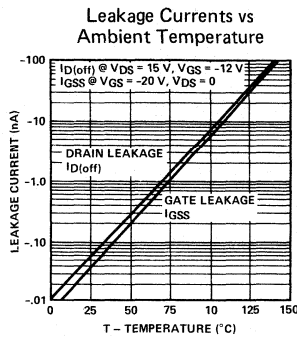
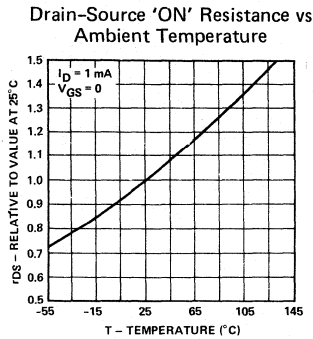
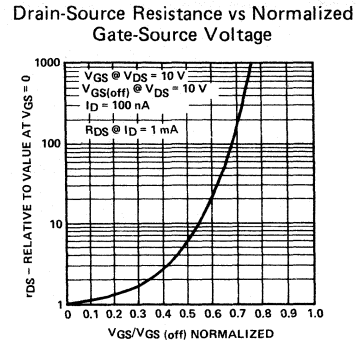
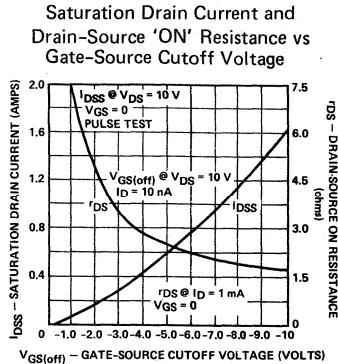
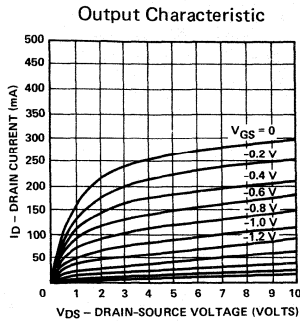
| TYPE   | PACKAGE         |
|--------|-----------------|
| Single | TO-52           |
| Single | TO-92           |
| Single | TO-92 Lead-form |
| Single | Chip            |

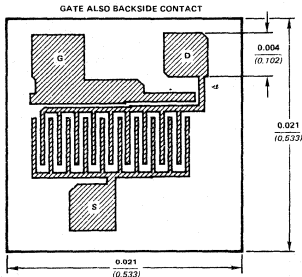
**PRINCIPAL DEVICES**

- U290-1
- J105-7
- J105-18 - 107-18
- U290CHP-1CHP, J105CHP-7CHP



### PERFORMANCE CURVES (25°C unless otherwise noted)





ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

## n-channel JFET designed for . . .

- VHF/UHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers



### BENEFITS

- Industry Standard
- High Power Gain  
16 dB at 100 MHz, Common Gate  
11 dB at 450 MHz, Common Gate
- Low Noise  
3 dB Noise Figure at 450 MHz
- Wide Dynamic Range  
Greater Than 100 dB
- 75 Ohm Input Match Common Gate

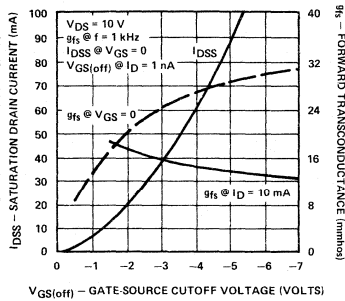
| TYPE   | PACKAGE         |
|--------|-----------------|
| Single | TO-52           |
| Single | TO-72           |
| Single | TO-92           |
| Dual   | TO-99           |
| Single | TO-92 Lead-form |
| Single | Chip            |
| Dual   | Chip            |

### PRINCIPAL DEVICES

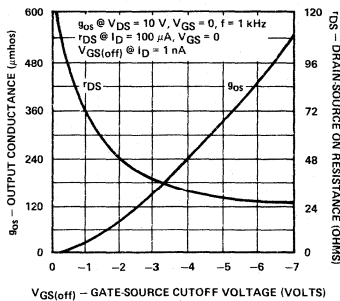
- U308-10
- U311
- J308-10
- U430-1
- K308-18 -310-18
- J308CHP-10CHP,
- U308CHP-10CHP, U311CHP
- U430CHP-1CHP

## PERFORMANCE CURVES (25°C unless otherwise noted)

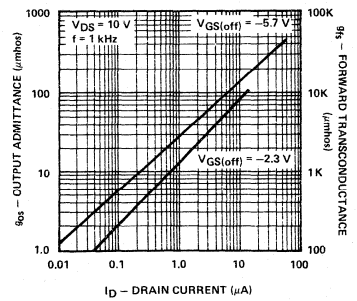
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



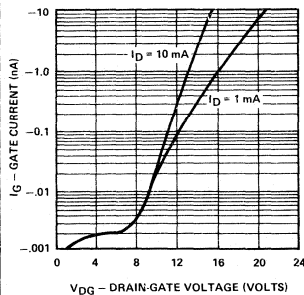
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



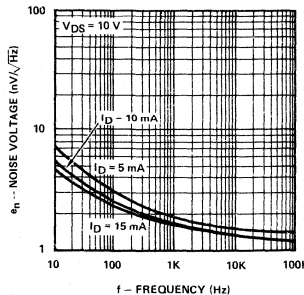
Common-Source Output Conductance vs Drain Current



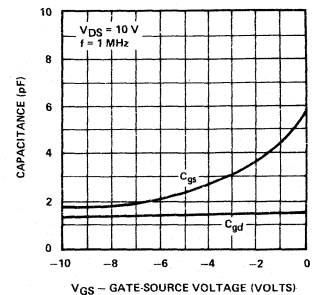
Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency



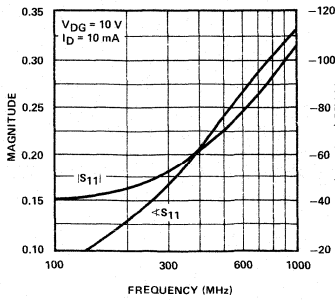
Junction Capacitance vs Gate-Source Voltage



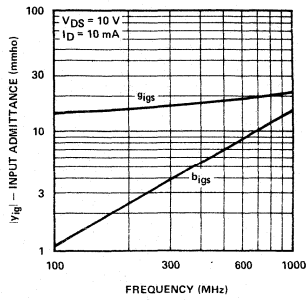


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

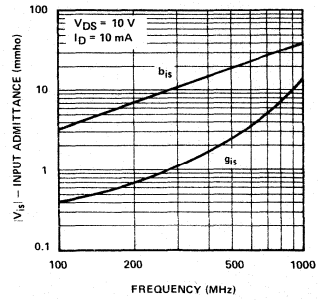
Forward Reflection Coefficient  
Common Gate



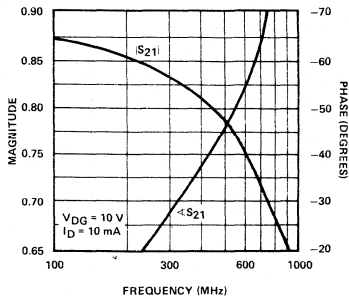
Input Admittance Common Gate



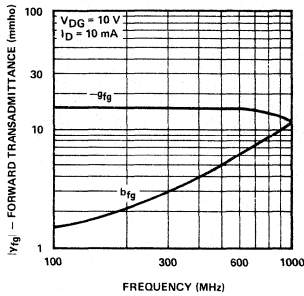
Input Admittance Common Source



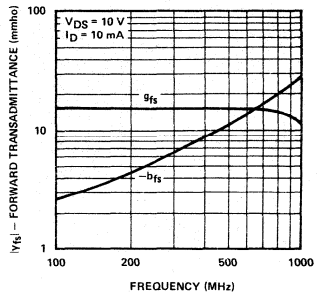
Forward Transmission Coefficient  
Common Gate



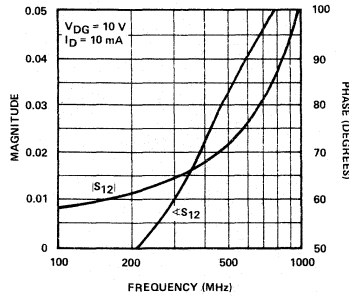
Forward Transfer Admittance  
Common Gate



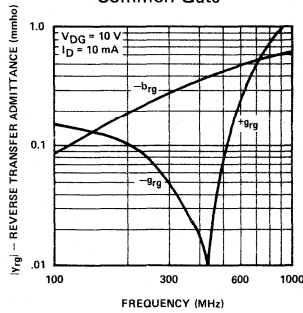
Forward Transfer Admittance  
Common Source



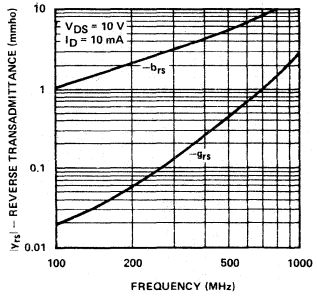
Reverse Transmission Coefficient  
Common Gate



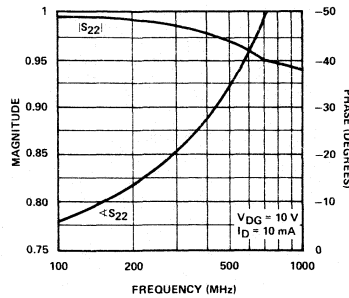
Reverse Transfer Admittance  
Common Gate



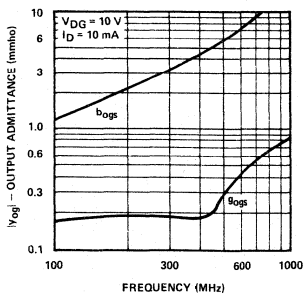
Reverse Transfer Admittance  
Common Source



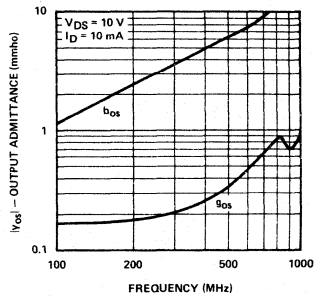
Reverse Reflection Coefficient  
Common Gate

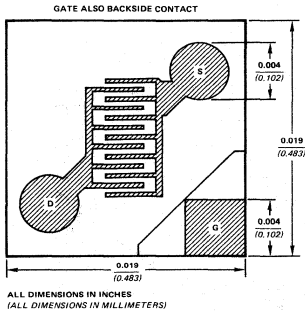


Output Admittance Common Gate



Output Admittance Common Source





### n-channel JFET designed for . . .

- High Frequency Amplifiers
- Mixers
- Oscillators

| TYPE   | PACKAGE |
|--------|---------|
| Single | TO-52   |
| Dual   | TO-78   |
| Dual   | TO-71   |
| Single | Chip    |
| Dual   | Chip    |

#### BENEFITS:

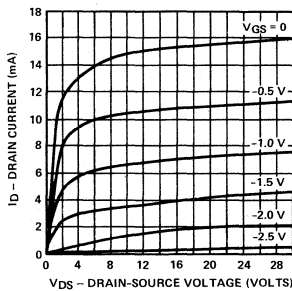
- High Power Gain
- Low Input Capacitance

#### PRINCIPAL DEVICES

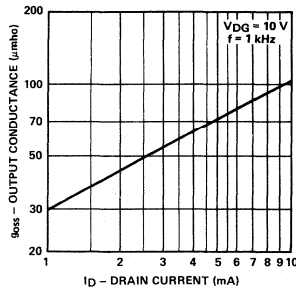
- U312
- 2N5911-12, U257
- U440-41
- U312CHP
- 2N5912CHP, U257CHP

## PERFORMANCE CURVES (25°C unless otherwise noted)

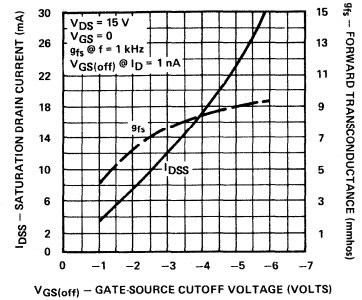
### Output Characteristic



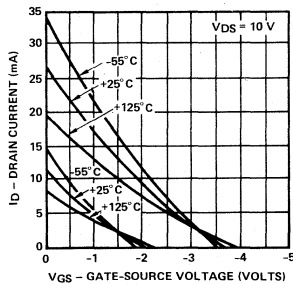
### Common-Source Output Conductance vs Drain Current



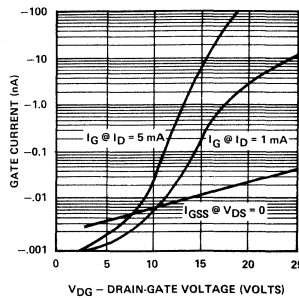
### Saturation Drain Current and Forward Transconductance vs Gate-Source Cutoff Voltage



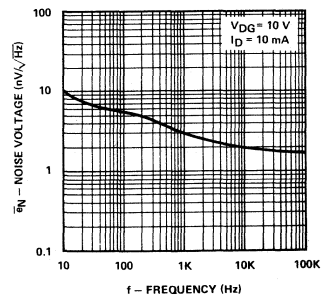
### Transfer Characteristics



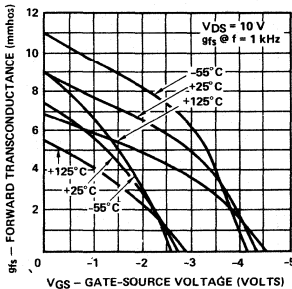
### Leakage Currents vs Drain-Gate Voltage



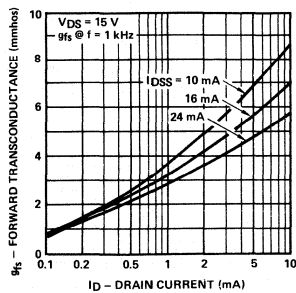
### Equivalent Input Noise Voltage vs Frequency



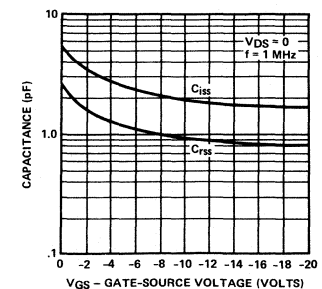
### Transconductance Characteristics



### Forward Transconductance vs Drain Current

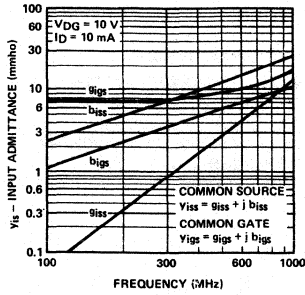


### Common-Source Capacitances vs Gate-Source Voltage

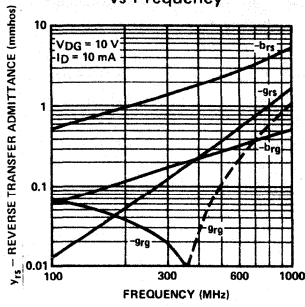


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

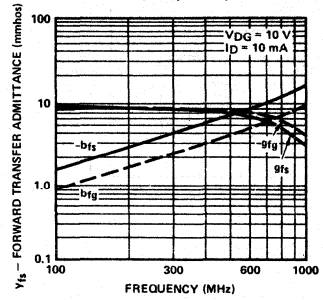
Input Admittance vs Frequency



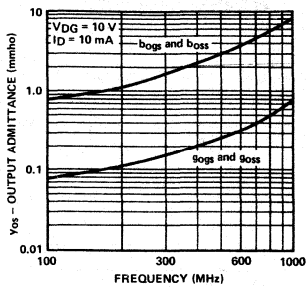
Reverse Transfer Admittance vs Frequency



Forward Transfer Admittance vs Frequency



Output Admittance vs Frequency

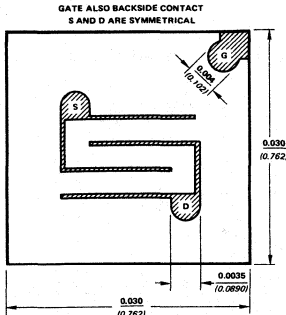


# p-channel JFET designed for ...

- General Purpose Amplifiers and Attenuators

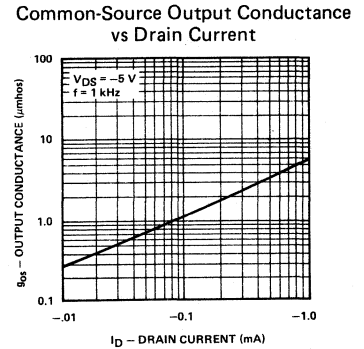
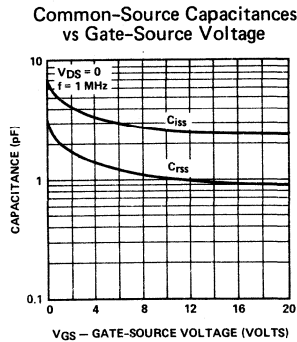
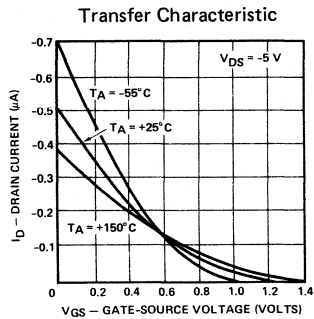
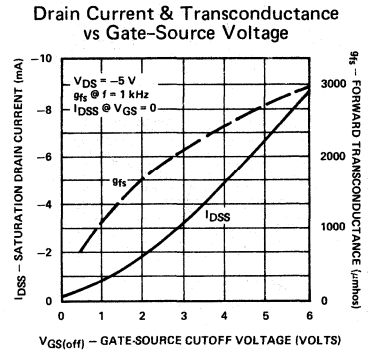
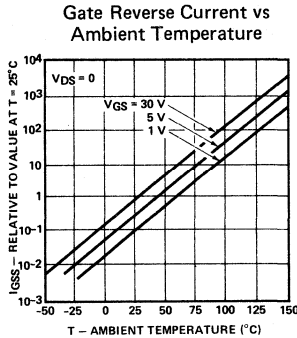
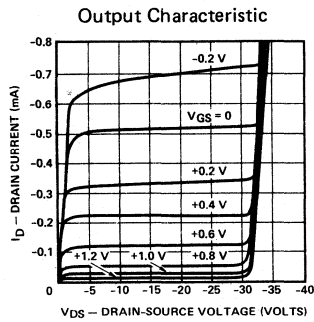
| TYPE   | PACKAGE |
|--------|---------|
| Single | TO-18   |
| Single | TO-72   |
| Single | Chip    |

**PRINCIPAL DEVICES**  
 2N2608, 2N2608JAN, 2N2843  
 2N3329-32, 2N3909, VCR5P  
 2N2608CHP, 2N2843CHP,  
 2N3329CHP-32CHP, 2N3909CHP  
 VCR5PCHP

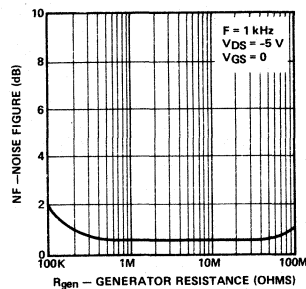


ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

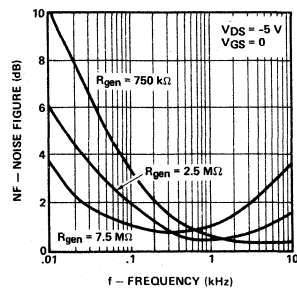
## PERFORMANCE CURVES (25°C unless otherwise noted)



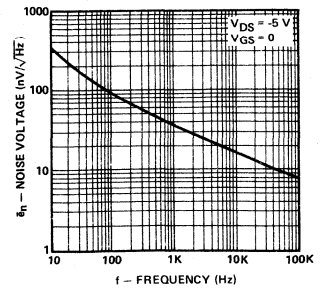
### Noise Figure vs Generator Resistance



### Noise Figure vs Frequency



### Equivalent Input Noise Voltage vs Frequency



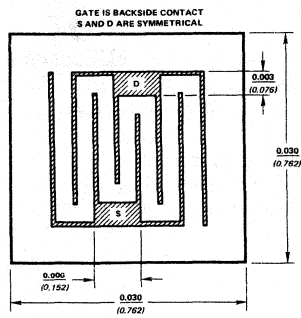


# p-channel JFET designed for . . .

- General Purpose Amplifiers

|             |                |
|-------------|----------------|
| <b>TYPE</b> | <b>PACKAGE</b> |
| Single      | TO-18          |
| Single      | Chip           |

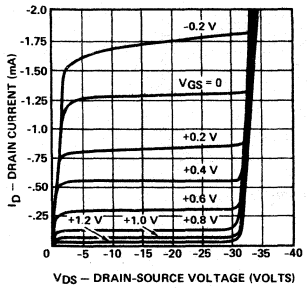
**PRINCIPAL DEVICES**  
2N2609, 2N2609JAN, 2N2844  
2N2609CHP, 2N2844CHP



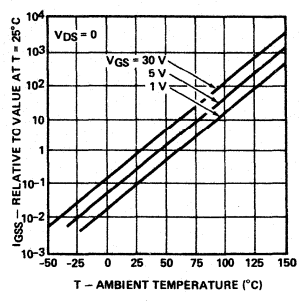
ALL DIMENSIONS IN INCHES  
TALL DIMENSIONS IN MILLIMETERS

## PERFORMANCE CURVES (25°C unless otherwise noted)

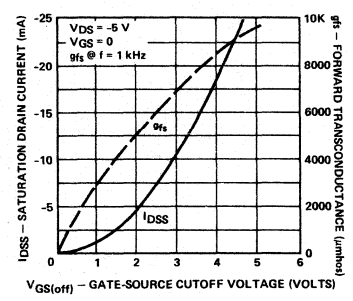
**Output Characteristic**



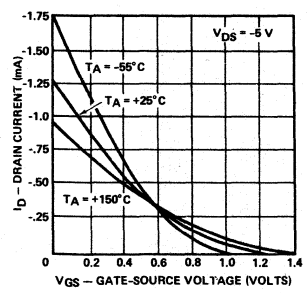
**Gate Reverse Current vs Ambient Temperature**



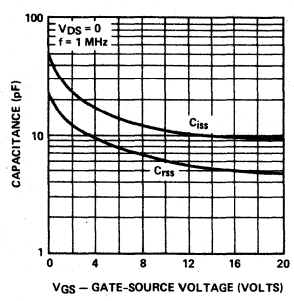
**Drain Current & Transconductance vs Gate-Source Voltage**



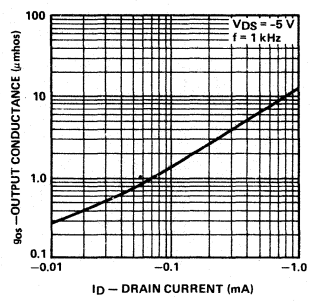
**Transfer Characteristic**



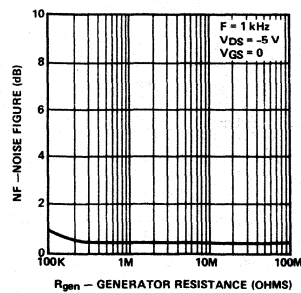
**Common-Source Capacitance vs Gate-Source Voltage**



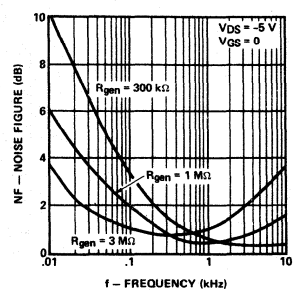
**Common-Source Output Conductance vs Drain Current**



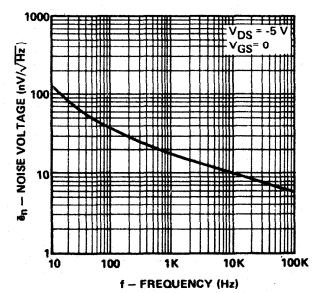
**Noise Figure vs Generator Resistance**

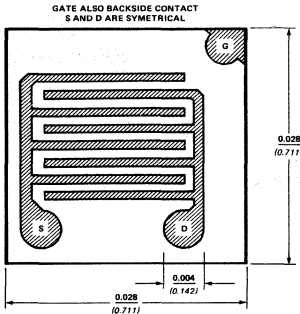


**Noise Figure vs Frequency**



**Equivalent Input Noise Voltage vs Frequency**





ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

**p-channel JFET**  
*designed for ...*

- General Purpose Amplifiers
- Switches

**TYPE**  
Single  
Single

**PACKAGE**  
TO-72  
Chip



**BENEFITS:**

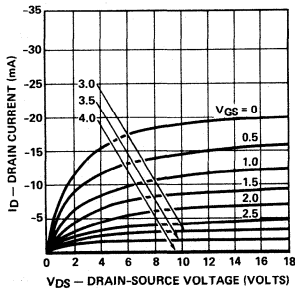
- Wide Range of Transconductance

**PRINCIPAL DEVICES**

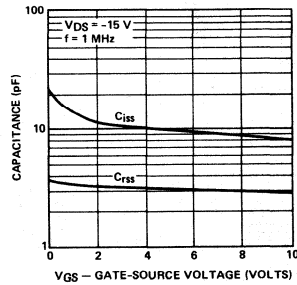
2N3382, 2N3384, 2N3386, VCR3P  
2N3382CHP-86CHP, VCR3PCHP

**PERFORMANCE CURVES (25°C unless otherwise noted)**

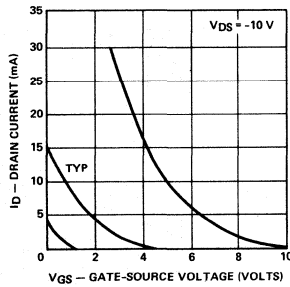
**Output Characteristic**



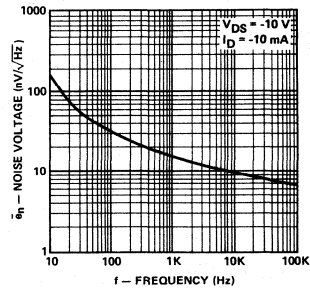
**Common-Source Capacitances vs Gate-Source Voltage**



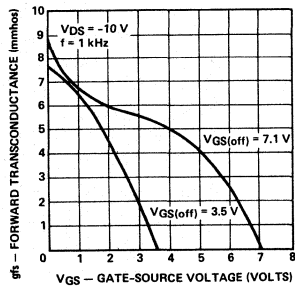
**Transfer Characteristics**



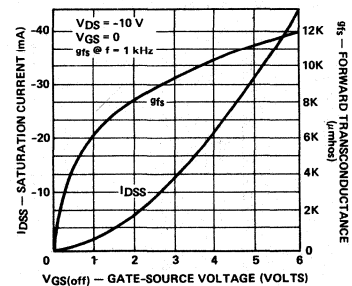
**Equivalent Input Noise Voltage vs Frequency**



**Transconductance Characteristics**



**Drain Current & Transconductance vs Gate-Source Voltage**



### p-channel JFET designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

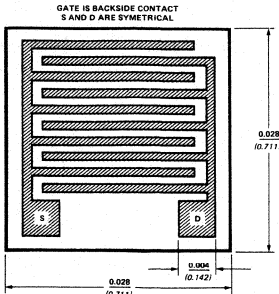
| TYPE   | PACKAGE         |
|--------|-----------------|
| Single | TO-18           |
| Single | TO-92           |
| Single | TO-92 Lead-form |
| Single | Chip            |

#### BENEFITS:

- Low Insertion Loss in Switching Systems  
 $R_{ON} < 75 \Omega$  (2N5114)
- Short Sample and Hold Aperture Time  
 $C_{RSS} < 7 \text{ pF}$
- High Off-Isolation  $I_{D(off)} < 500 \text{ pA}$

#### PRINCIPAL DEVICES

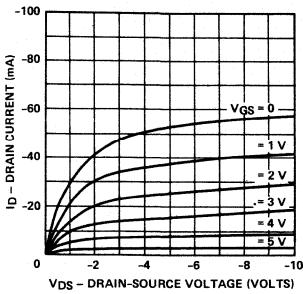
- 2N5018-19, 2N5114-16, U304-6  
 J174-7, J270-1, P1086-87, P1086E  
 J174-18-177-18, J270-18-271-18  
 P1086-18-87-18  
 2N5018CHP-19CHP, 2N5114CHP-16CHP  
 U304CHP-6CHP, P1086CHP-87CHP  
 J270CHP-271CHP



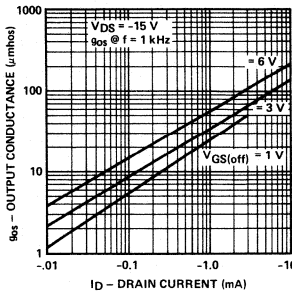
ALL DIMENSIONS IN INCHES  
(ALL DIMENSIONS IN MILLIMETERS)

### PERFORMANCE CURVES (25°C unless otherwise noted)

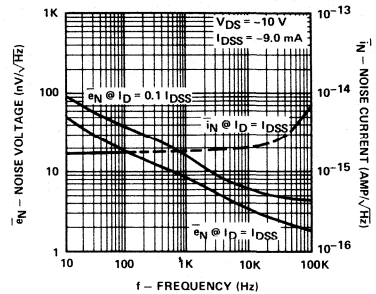
#### Output Characteristic



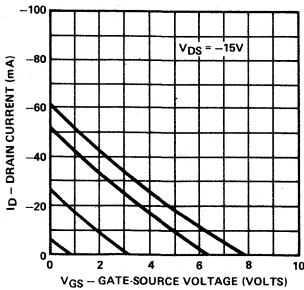
#### Common-Source Output Conductance vs Drain Current



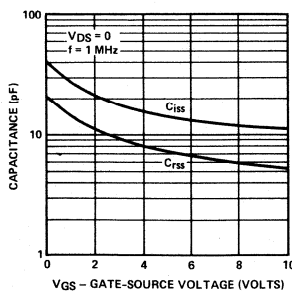
#### Equivalent Input Noise Voltage and Noise Current vs Frequency



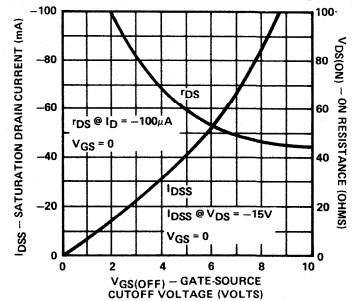
#### Transfer Characteristics



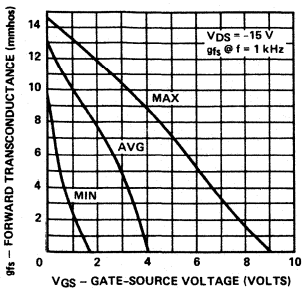
#### Common-Source Capacitance vs Gate-Source Voltage



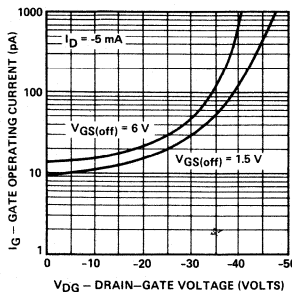
#### Saturation Drain Current and Drain-Source ON Resistance vs. Gate-Source Cutoff Voltage



#### Transconductance Characteristics



#### Gate Operating Current vs Drain-Gate Voltage







# **application notes**

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# APPLICATION NOTE

## An Introduction to FETs

### INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J.E. Lilienfeld's patent of 1925. The theoretical description of a FET made by Shockley in 1952 paved the way for development of a classic electronic device which provides the designer with the means by which he can accomplish nearly every circuit function. The field-effect transistor earlier was known as a "unipolar" transistor, and the term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology and parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

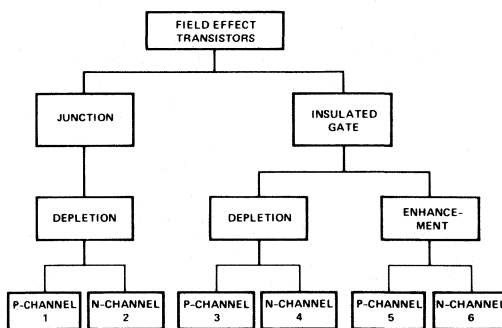
|                   |                 |                           |
|-------------------|-----------------|---------------------------|
| <i>Amplifiers</i> | <i>Switches</i> | <i>Current Limiters</i>   |
| Small Signal      | Chopper-type    | <i>Voltage-Controlled</i> |
| Low Distortion    | Analog Gate     | <i>Resistors</i>          |
| High Gain         | Commutator      | <i>Mixers</i>             |
| Low Noise         |                 | <i>Oscillators</i>        |
| Selective         |                 |                           |
| D.C.              |                 |                           |
| High-Frequency    |                 |                           |

This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics — which are very different from those of bipolar devices — can often make possible the design of technically superior (and sometimes cheaper) circuits. This comment applies not only to networks employing discrete devices and conventional components such as resistors and capacitors, but also extends to both linear and digital integrated circuits.

In fact, FET technology today allows a greater packaging density in large-scale integrated circuits (LSI) than would ever be possible with bipolar devices.

(Although there is no industry-accepted definition of LSI, apparently when the equivalent circuit of an IC contains more than 1,000 active elements (500 gates) or is "very complex", the end product may be called LSI. With a typical LSI chip measuring less than 200 x 200 mils, this is high-density packaging indeed.)

The family tree of FET devices (Figure 1) may be divided into two main branches, junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, *metal-oxide-silicon field-effect transistors*). Junction FETs are inherently depletion-mode devices, and are available in both P- and N-Channel configurations. MOSFETs are available in both enhancement or depletion modes, and exist as both N- and P-Channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

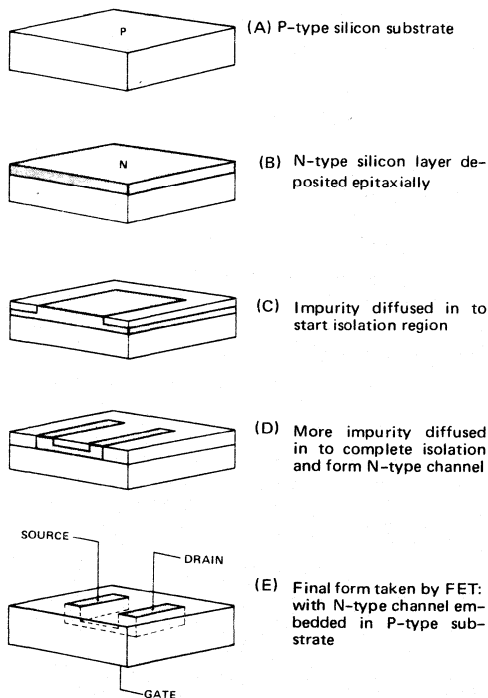


FET Family Tree  
Figure 1

## Junction FETs

In its most elementary version, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a *gate*, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the fundamental difference between FET and bipolar devices: when the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The FET is a high input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, N-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, P-type material will be formed and the channel current will consist of holes. N-Channel devices have greater conductivity than P-Channel types, since electrons have higher mobility than do holes; thus N-Channel FETs tend to be more efficient conductors than their P-Channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, N-type silicon is deposited



Idealized Manufacture of an N-Channel Junction FET

Figure 2

epitaxially (single-crystal condensation surface) onto monocrystalline P-type silicon, so that crystal integrity is maintained. Then a layer of silicon dioxide is grown on the surface of the N-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a P-type annulus has been formed in the layer on N-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of N-type material within the substrate.

In addition to the channel material, a FET contains two ohmic (non-rectifying) contacts, the *source* and the *drain*. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized FET chip, it is immaterial which contact is called the source and which is called the drain; the FET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

(For certain FET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

Figure 2E also shows how the N-Channel is embedded in the P-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the FET functions. If the gate is connected to the source, then the applied voltage ( $V_{DS}$ ) will appear between the gate and the drain. Since the PN junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a *depletion* layer, where almost all the electrons present in the N-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current ( $I_D$ ) which increased  $V_{DS}$  can drive through the channel. This limiting current is known as  $I_{DSS}$  (*Drain-to-Source* current with the gate *Shorted* to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

Figure 3C shows the output characteristics of an N-Channel JFET with the gate short-circuited to the source. The initial rise in  $I_D$  is related to the buildup of the depletion layer as  $V_{DS}$  increases. The curve approaches the level of the limiting current  $I_{DSS}$  when  $I_D$  begins to be *pinched off*. The physical meaning of this term leads to one definition of *pinch-off voltage*,  $V_P$ , which is the value of  $V_{DS}$  at which the maximum  $I_{DSS}$  flows.

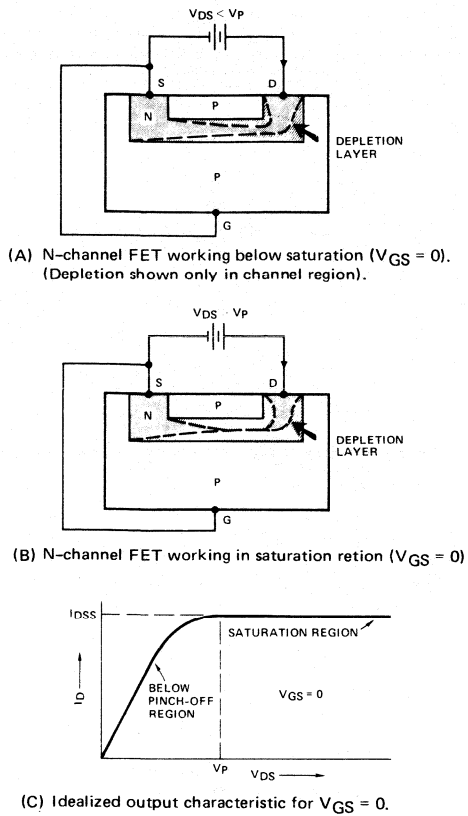
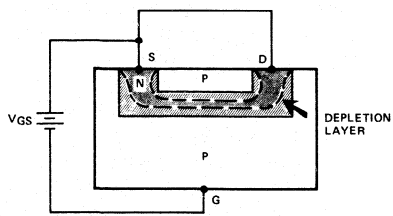


Figure 3

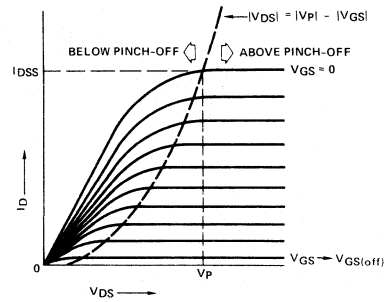
In Figure 4, consider the case where  $V_{DS} = 0$ , and where a negative voltage  $V_{GS}$  is applied to the gate. Again, a depletion layer has built up. If a small value of  $V_{DS}$  were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for  $V_{GS} = 0$ . In fact, at a value of  $|V_{GS}| \geq |V_p|$  the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol  $V_p$  or by  $V_{GS(off)}$ .  $V_p$  has been widely used in the past, but  $V_{GS(off)}$  is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off.  $V_{GS(off)}$  and  $V_p$ , strictly speaking, are equal in magnitude but opposite in polarity.



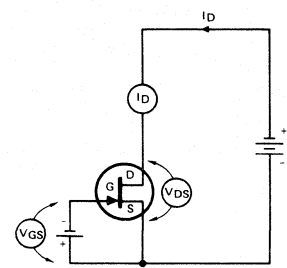
N-channel FET Showing Depletion Due To Gate-Source Voltage ( $V_{DS} = 0$ )  
Figure 4

The mechanisms of Figure 3 and 4 react together to provide a family of output characteristics as shown in Figure 5A. The area below the pinchoff voltage locus is known as the triode or "below pinchoff" region; the area above pinchoff is often referred to as the pentode or saturation region. FET behavior in these regions is comparable to that of a power grid vacuum tube, and for this reason FETs operating in the saturation region may be used as excellent amplifiers. Note that in the "below pinchoff" region both  $V_{GS}$  and  $V_{DS}$  control the channel current, while in the saturation region  $V_{DS}$  has little effect and  $V_{GS}$  essentially controls  $I_D$ .

Figure 5B relates the curves of Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of  $V_{DS}$  and  $V_{GS}$ . Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.



(A) Family of output characteristics for N-channel FET



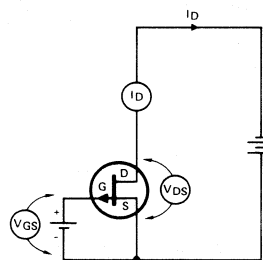
(B) Circuit arrangement for N-channel FET

Figure 5

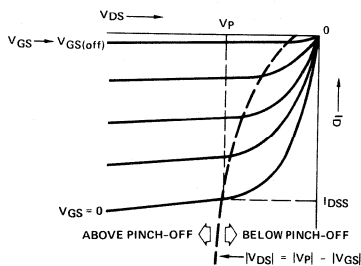
The P-Channel FET works in precisely the same way as does the N-Channel FET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto N-type silicon, and the donor impurity diffused later to form a second N-type region and leave a P-type chan-

nel. In the P-Channel FET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a P-Channel FET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the N-Channel FET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages,  $V_{DS}$  and  $V_{GS}$ . When  $V_{DS}$  is greater than  $V_p$ , the channel current is controlled largely by  $V_{GS}$  alone, because  $V_{GS}$  is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit arrangement for P-channel FET

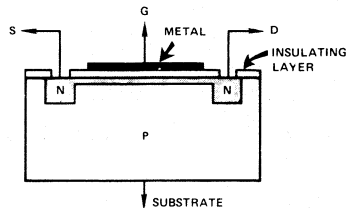


(B) Family of output characteristics for P-channel FET

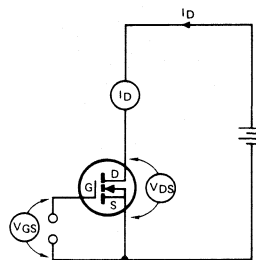
Figure 6

## MOSFETs

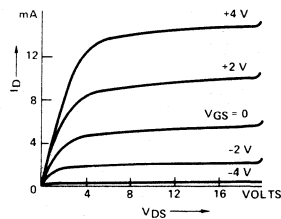
The metal-oxide-silicon FET (MOSFET) depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the P-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate at the interface, spontaneously forming an N-type channel. Thus a conducting path exists between the diffused N-type source and drain regions. Further, the MOSFET will behave



(A) Idealized cross-section through an N-channel depletion-type MOSFET



(B) Circuit arrangement for N-channel depletion MOSFET



(C) Family of output characteristics for the Siliconix 2N3631 N-channel depletion MOSFET

Figure 7

in a manner similar to the N-Channel junction FET when a voltage of the correct polarity is applied to the channel, as in Figure 7B.

Output characteristics of an N-Channel MOSFET are shown in Figure 7C. Because there is no junction involved,  $V_{GS}$  can be reversed without endangering a gate current; the gate may be made either positive or negative with respect to the source. Under these circumstances, still more free electrons will be attracted to the channel region, and  $I_D$  will become greater than  $I_{DSS}$ . This mode of operation is represented by the higher members of the family of output characteristics. Because the application of a negative gate voltage causes the channel to be depleted of free electrons — thus reducing  $I_D$  — the device just described is called a *depletion-mode* MOSFET.

The foregoing has established that the depletion-mode MOSFET is a “normally-ON” device: when  $V_{GS} = 0$ , a conducting path exists between source and drain. In many circuits a “normally-OFF” device would be useful, a condition which leads to the concept of an *enhancement-mode* MOSFET. In the latter device, an increasing voltage applied to the gate will enhance channel conduction, and depletion will never occur,  $I_D$  being zero when  $V_{GS} = 0$ .

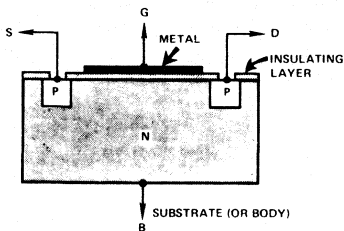
A P-Channel enhancement-mode MOSFET is shown in Figure 8. Here, an acceptor impurity has been diffused into an N-type substrate to form P-type source and drain regions. No conducting channel exists between the source and the drain, because no matter how the drain-source voltage is applied one of the PN junctions will always be reverse-biased. On the other hand, if a negative voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layer of the substrate and produce a P-type channel. A family of output characteristics for a typical MOSFET is shown in Figure 8C. The idealized cross-section illustrated in Figure 8A may be used to show how the characteristics of Figure 8C come about. Refer to Figure 9 for an extension of this phenomenon.

If a constant (negative) gate voltage, ( $V_{GS(K)}$ ) is applied, then an essentially-uniform P-Channel depletion layer will be induced, as in Figure 9A. If a negative drain voltage is applied, then current,  $I_D$ , will flow through the drain. As  $|V_{DS}|$  increases,  $I_D$  also increases. However, the voltage between the drain and the gate decreases, so that the thickness of the channel at the drain end is reduced as in Figure 9B. Therefore, the relationship of  $I_D$  versus  $V_{DS}$  will even-

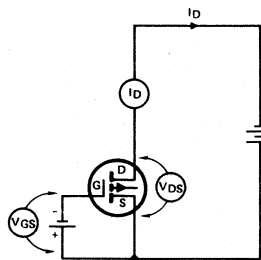
tually reach a limiting value when  $V_{DS} = V_{GS}$ , and the channel becomes pinched off. This condition is shown in Figure 9C.

Different values of  $V_{GS}$  give rise to limiting values of  $I_D$ , so that the characteristic family of output curves which was shown in Figure 8 is realized. Characteristics of depletion-mode MOSFETs also come about for the same reason, except that members of the output characteristics family also exist for  $V_{GS}$  values of zero or reversed polarity. The P-Channel enhancement-mode MOSFET is currently the most popular member of the FET family in current use, and is in fact the basic element in many LSI integrated circuits.

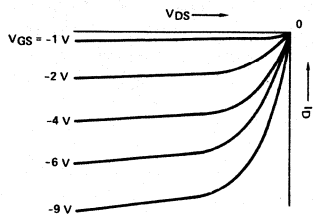
In principle it is possible to manufacture the remaining two members of the MOSFET family, the P-Channel depletion-mode and the N-Channel enhancement-mode devices. Because of the spontaneous formation of an N-Channel at a silicon/silicon-dioxide interface, the fabrication processes involved become quite difficult on a volume production basis. Much work has gone into the development of practical MOSFET processes for these devices, and N-Channel depletion-mode types are now becoming generally available.



(A) Idealized cross-section through a P-channel enhancement MOSFET

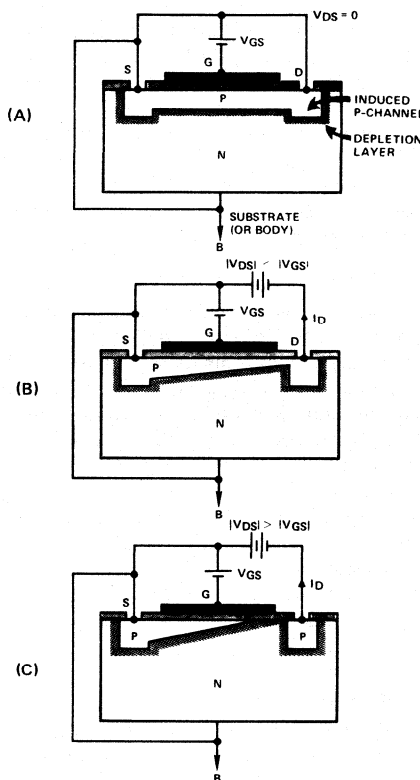


(B) Circuit arrangement for P-channel enhancement MOSFET



(C) Family of output characteristics for a P-channel enhancement MOSFET

Figure 8



Idealized approach of pinch-off, (A)  $V_{DS} = 0$ , (B)  $|V_{DS}| < |V_{GS}|$ , (C)  $|V_{DS}| > |V_{GS}|$

Figure 9

## FET Characteristics

The FET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range ( $> 100$  dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a FET approximates to a square-law response, and the second and higher-order derivatives of  $g_m$  are near zero; thus strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a FET is simply the impedance of a reverse-biased PN junction, which is on the order of  $10^{10}$  to  $10^{12} \Omega$ . In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency; for example, in a 2N4416 FET, the input impedance would be  $22K \Omega$  at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The FET has very high dynamic range, in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

## FET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on FET electrical quantities and parameters – in particular, the most important parameters, and the means by which they can be measured. The following discussion will define specific FET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- $I_{DSS}$  – Drain current with the gate shorted to the source
- $V_{GS(off)}$  – Gate-source cutoff voltage
- $I_{GSS}$  – Gate-to-source current with the drain shorted to the source
- $BV_{GSS}$  – Gate-to-source breakdown voltage with the drain shorted to the source
- $g_{fs}$  – Common-source forward transconductance
- $C_{gs}$  – Gate-source capacitance
- $C_{gd}$  – Gate-drain capacitance

Special attention should be given to the subscript "s" because it has two different meanings and three possible uses. In FET notations, an "s" for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an "s" for the third subscript does not refer to the FET source terminal. It is an abbreviation for "shorted", and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term  $I_{GSS}$  refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the FET, four-pole admittance equations are commonly used to describe electrical characteristics of the FET:

$$I_1 = Y_{11} V_{11} + Y_{21} V_{22} \quad (1)$$

When  $Y_{11}$ ,  $Y_{21}$ ,  $Y_{12}$  and  $Y_{22}$  are defined as the input, reverse transfer, forward transconductance, and output admittances respectively, Equation 1 reduces to

$$i_1 = y_i v_{11} + y_r v_{22} \quad (2)$$

$$i_2 = y_f v_{11} + y_o v_{22}$$

For a three-lead FET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

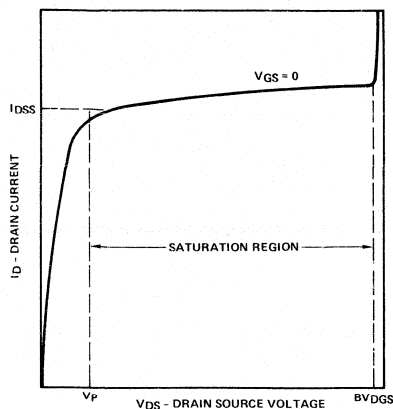
$$\begin{aligned} i_i &= y_{is} v_{gs} + y_{rs} v_{ds} \\ i_o &= y_{fs} v_{gs} + y_{os} v_{ds} \end{aligned} \quad (3)$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.



### $I_{DSS}$ – Drain Current at Zero Gate Voltage ( $I_D$ at $V_{GS} = 0$ )

By itself,  $I_{DSS}$  merely refers to the drain current that will flow for any applied  $V_{DS}$  with the gate shorted to the source. However, when a particular value for  $V_{DS}$  is given, equal to or greater than  $V_P$  (see Figure 10),  $I_{DSS}$  indicates the drain saturation current at zero gate voltage. Some FET data sheets label  $I_{DSS}$  for  $V_{DS}$  greater than  $V_P$  as  $I_{D(on)}$ .



FET Characteristic at  $V_{GS} = 0$   
Figure 10

### $V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by  $R = \rho L/A$ , where

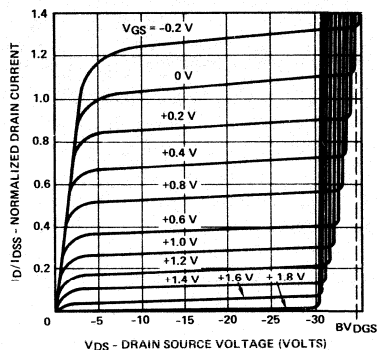
$\rho$  = resistivity

$L$  = length of the channel

$A = W \times T$  = cross-sectional area of channel

In the usual FET structure,  $L$  and  $W$  are fixed by device geometry, while channel thickness  $T$  is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When  $T$  is reduced to zero by any combination of  $V_{GS}$  and  $V_{DS}$ , the depletion layers from the opposite sides come in contact, and the a-c or incremental channel resistance,  $r_{DS}$ , approaches infinity. As earlier noted, this condition is referred to as “pinch-off” or “cutoff” because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in  $V_{DS}$  (up to the junction reverse-bias breakdown) will cause little change in  $I_D$ . Accordingly, the pinch-off region is also referred to as the pentode or “constant-current” region.

In Figure 10, pinch-off occurs with  $V_{GS} = 0$ . In Figure 11,  $V_{GS}$  controls the magnitude of the saturated  $I_D$ , with increases in  $V_{GS}$  resulting in lower values of constant  $I_D$ , and smaller values of  $V_{DS}$  necessary to reach the “knee” of the curve. The current scale in Figure 11 has been normalized to a specific value of  $I_{DSS}$ .



FET  $I_D$  vs  $V_{DS}$  Output Characteristics  
Figure 11

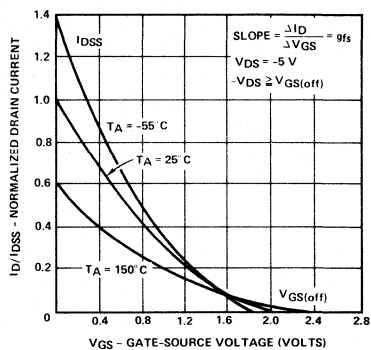
The knee of the curve is important to the circuit designer because he must know what minimum  $V_{DS}$  is needed to reach the pinch-off region with  $V_{GS} = 0$ . When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow;  $V_{DS}$  has no effect until breakdown occurs. The specific amount of  $V_{GS}$  that produces pinch-off is known as the gate-source cutoff voltage,  $V_{GS(off)}$ .

### $V_{GS(off)}$ Test Procedure

Although the magnitude of  $V_{GS(off)}$  is equal to the pinch-off voltage,  $V_P$ , defined by the pinch-off knee in Figure 10, rapid curvature in the area makes it difficult to define any precise point as  $V_P$ . Taking a second derivative of  $V_{DS}/I_D$  would yield a peak corresponding to the inflection point at the knee, which approximates  $V_P$ . However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the  $I_D$  versus  $V_{GS}$  characteristic. This is easier than trying to specify the location of the knee of the  $I_D$  versus  $V_{DS}$  output characteristic.

A typical transfer characteristic  $I_D$  versus  $V_{GS}$  is shown in Figure 12. The curve can be closely approximated by

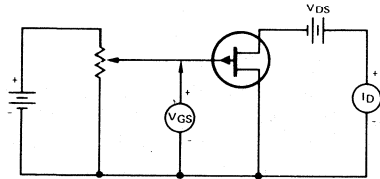
$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 \quad (4)$$



Typical  $I_D$  vs  $V_{GS}$  Transfer Characteristic  
Figure 12

Equation 4 and Figure 12 indicate that at  $V_{GS} = V_{GS(off)}$ ,  $I_D = 0$ . In a practical device, this cannot be true because of leakage currents. If  $I_D$  is reduced to less than 1 percent of  $I_{DSS}$ ,  $V_{GS}$  will be within 10 percent of the  $V_{GS(off)}$  value indicated by Equation 4. If  $I_D$  is reduced to 0.1 percent of  $I_{DSS}$ , the indicated  $V_{GS(off)}$  error will be reduced to about 3 percent. For a true indication of  $V_{GS(off)}$ , and a realistic picture of the parameters of Figure 12, care must be taken that leakage currents do not result in an error in the  $V_{GS(off)}$  reading. Typically, at room temperature, 1 percent of  $I_{DSS}$  is still well above leakage currents but is low enough to give a fairly accurate value of  $V_{GS(off)}$ .

A typical circuit for measuring  $V_{GS(off)}$  is shown in Figure 13. At  $V_{GS} = 0$ , the value of  $I_{DSS}$  can be measured. Then, by increasing  $V_{GS}$  until  $I_D$  is 0.01 percent of  $I_{DSS}$ , the value of  $V_{GS(off)}$  is obtained. From a production standpoint, it is more convenient to specify  $I_D$  at some fixed value (such as 1 nA), rather than as a certain percentage of  $I_{DSS}$ . Thus a pinchoff voltage specification may be given as indicated in Table I.



Circuit for Measuring  $V_{GS(off)}$   
Figure 13

Table I  
Typical Pinch-Off Voltage Specification

| Characteristic   | Min | Max | Units |
|--|-----|-----|-------|
| $V_{GS(off)}$ Gate-source pinch-off voltage of:<br>$V_{DS} = -5 \text{ V}, I_D = -1 \mu\text{A}$ | 1   | 4   | Volts |

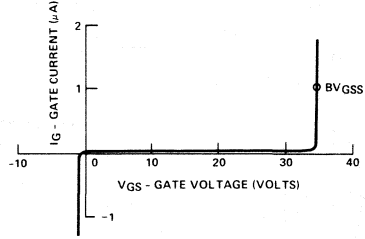
Another method which provides an indirect indication of the maximum value of  $V_{GS(off)}$  is shown in Table II. The characteristic specified is  $I_{D(off)}$ , whereas the parameter of interest is  $V_{GS} = 8$  volts. The specification does say that the maximum  $V_{GS(off)}$  is approximately 8 volts, but no provision is made for stating a *minimum*  $V_{GS(off)}$ , as was done in Table I. Therefore, another test must be made if  $V_{GS(off) (min)}$  is to be specified.

Table II  
Indication of Maximum  $V_p$

| Characteristic                       | Test Conditions                                     | Min | Max | Unit          |
|--------------------------------------|---|-----|-----|---------------|
| $I_{D(off)}$ Pinch-off drain current | $V_{DS} = -12 \text{ V},$<br>$V_{GS} = 8 \text{ V}$ |     | -10 | $\mu\text{A}$ |

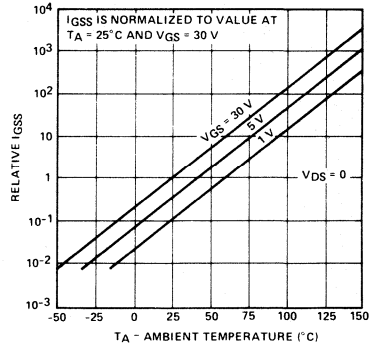
**$I_{GSS}$  – Gate-Source Cutoff Current**

The input gate of a P-Channel FET appears as a simple PN junction; thus the input d-c input characteristic is analogous to a diode V-I curve, as is shown in Figure 14.



P-Channel FET Input Gate Characteristic  
Figure 14

In the normal operating mode, with  $V_{GS}$  positive for a P-Channel device, the gate is reverse-biased to a voltage between zero and  $V_{GS(off)}$ . This results in a d-c gate-source resistance which is typically more than 100M  $\Omega$ . The gate current is both voltage- and temperature-sensitive. Figure 15 shows this relationship for  $I_{GSS}$  versus temperature and  $V_{GS}$ .



$I_{GSS}$  vs Temperature  
Figure 15

If the gate-source junction becomes forward-biased, (negative voltage in a P-Channel device) or if  $V_{GS}$  exceeds the reverse-bias breakdown for the junction, the input resistance will then become very low.

The FET is normally operated with a slight reverse bias applied to the gate-source; hence a good measure of the d-c input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are three common measurements of gate current:  $I_{GDO}$ ,  $I_{GSO}$ , and the combined measurement  $I_{GSS}$ . These measurement circuits are shown in Figure 16.

The question is, should  $I_{GDO}$  and  $I_{GSO}$  be measured separately, or will one measurement of  $I_{GSS}$  suffice? One thing is certain:  $I_{GSO} + I_{GDO} > I_{GSS}$ , because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most FETs, if  $V_G$  is greater than  $V_{GS(off)}$ , the difference between  $(I_{GSO} + I_{GDO})$  and  $I_{GSS}$  is small; therefore, the measurement of  $I_{GSS}$  is a realistic means of controlling both  $I_{GDO}$  and  $I_{GSO}$ .

In a circuit,  $V_{GD}$  may be biased between zero and  $BV_{GDS}$ , while  $V_{GS}$  will be between zero and  $V_{GS(off)}$ ; therefore,  $I_G$  is not necessarily the same as  $I_{GSS}$ .

**BV<sub>GSS</sub> – Gate-Source Breakdown Voltage**

FET input terminals have been previously described as having NP or PN junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

A useful equivalent circuit for a FET is the distributed constant network shown in Figure 17, for a P-Channel FET. If an N-Channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus the gate-drain breakdown rating is most important. However, it is also pos-

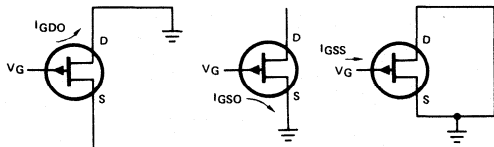
sible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 17, when a high negative voltage is applied from drain to source,  $CR_1$  will break down while  $CR_n$  becomes forward-biased).

Some device manufacturers use a  $BV_{GDO}$  rating, which means they are only checking diode  $CR_1$ . A better method is to use a  $BV_{GSS}$  rating (gate-source breakdown with the drain shorted to the source), because it checks both  $CR_1$  and  $CR_n$ , in addition to exposing the *weakest* breakdown path along the entire gate-channel junction. The  $BV_{GSS}$  test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

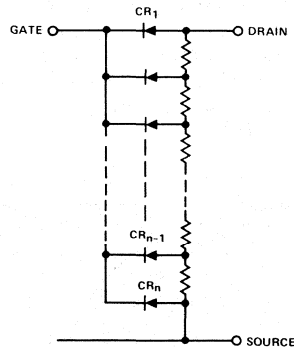
Admittedly, a  $BV_{GSS}$  test will reject some units which might pass a  $BV_{GDO}$  test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

**Test Procedures for BV<sub>GSS</sub>**

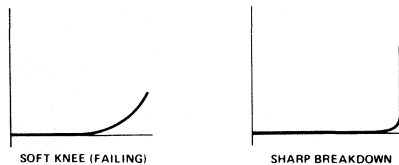
Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 18).



Three Common Measurement of Gate Current  
Figure 16



A Useful FET Equivalent Circuit  
Figure 17



Examples of Soft Knee and Sharp Knee Breakdown  
Figure 18

**$g_{fs}$  – Transconductance**

Transconductance,  $g_{fs}$ , is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} = \text{constant} \quad (5)$$

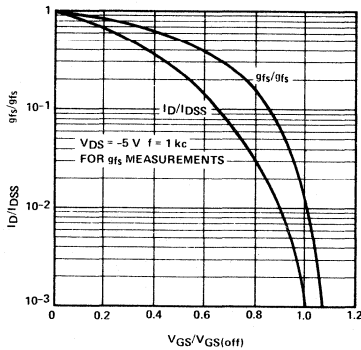
The interrelation of  $g_{fs}$  to the parameters  $I_{DSS}$  and  $V_{GS(OFF)}$  should be noted. Equations 4, 6 and 7 describe the value of  $I_D$  and  $g_{fs}$  in a FET for any value of  $V_{GS}$  between zero and  $V_{GS(OFF)}$ .

$$g_{fs} = g_{fs0} \left( 1 - \frac{V_{GS}}{V_{GS(off)}} \right) \quad (6)$$

$$g_{fs0} = - \frac{2I_{DSS}}{V_{GS(off)}} \quad (7)$$

where  $g_{fs0}$  is the value of  $g_{fs}$  at  $V_{GS} = 0$  and  $I_{DSS}$  is the value of  $I_D$  at  $V_{GS} = 0$ . With these equations, the value of  $g_{fs}$  can be calculated with a fair degree of accuracy (20 percent) if  $I_{DSS}$  and  $V_{GS(off)}$  are known.

Figure 19 shows normalized curves for  $I_D$  and  $g_{fs}$  as functions of  $V_{GS}$  in a P-Channel FET. These curves were obtained from actual measurements on typical diffused channel FETs, such as the 2N2606. The curves agree very well with Equations 4 and 6 until  $V_{GS(off)}$  is approached. For these curves,  $V_{GS(off)}$  was assumed to be the value of  $V_{GS}$  where  $I_D/I_{DSS} = 0.001$ .



**Normalized Curves for  $I_D$  and  $g_{fs}$  as Functions of  $V_{GS}$**   
Figure 19

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_{D/triode} = I_{DSS} \left( \frac{V_{DS}}{V_{GS(off)}} \right)^{1/2} \quad (8)$$

Specifications for  $g_{fs}$  are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the N-Channel 2N3823 and the P-Channel 2N3329. The gate voltage for the 2N3823 is established as zero. This means that  $g_{fs}$  is measured at  $I_D = I_{DSS}$ , as in Table III.

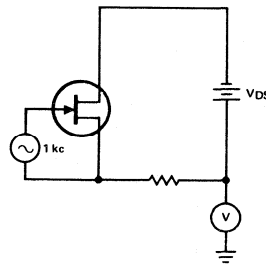
**Table III (2N3823)**

| Characteristic   | Test Conditions  | Min   | Max   | Unit            |
|--|--|-------|-------|-----------------|
| $g_{fs}$ Small-signal common-source forward transconductance | $V_{DS} = 15 \text{ V}$ ,<br>$V_{GS} = 0$ ,<br>$f = 1 \text{ kHz}$ | 3,500 | 6,500 | $\mu\text{mho}$ |

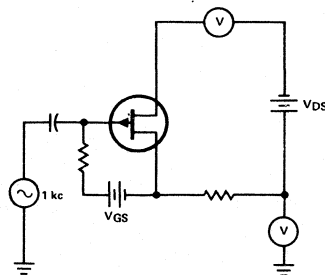
**Table IV (2N3329)**

| Characteristic                                     | Test Conditions  | Min | Max | Unit            |
|--|--|-----|-----|-----------------|
| $Y_{fs}$ Common-source forward transfer admittance | $V_{DS} = -10 \text{ V}$ ,<br>$I_D = -1 \text{ mA}$ ,<br>$f = 1 \text{ kHz}$ |     | 20  | $\mu\text{mho}$ |

The test conditions shown in Table IV specify a certain value for  $I_D$  (-1 mA for the 2N3329). This means that for each unit tested,  $V_{GS}$  is adjusted until  $I_D$  equals the specified value. The conditions specified in Table III simplify testing of the  $g_{fs}$  parameter by eliminating the necessity of adjusting  $V_{GS}$ . Figures 20 and 21 show typical test setups for the two methods.



**Test Circuit for  $g_{fs}$  with  $V_{GS} = 0$**   
Figure 20



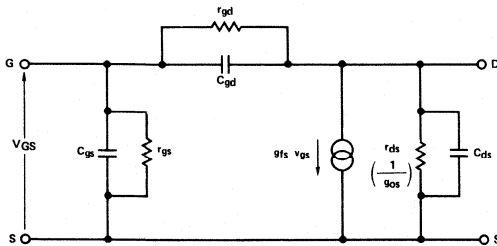
**Test Circuit for  $g_{fs}$  with  $I_D$  Specified**  
Figure 21

**Junction FET Capacitances**

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometric distribution are functions of the applied voltages  $V_{GS}$  and  $V_{DS}$ . Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances,  $C_{gs}$  and  $C_{gd}$ , exist between the gate and the source and drain, respectively. (A much smaller capacitance,  $C_{ds}$ , also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote  $C_{gs}$  and  $C_{gd}$  (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of  $C_{gs}$  and  $C_{gd}$  as the result of changing conditions of  $V_{DS}$ ,  $V_{GS}$  and temperature. If these data are not presented, an estimate of inter-electrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the  $-2.2 \text{ mV}/^\circ\text{C}$  change in junction potential difference.

Assuming that the FET is properly biased — that is, that the d-c conditions are met by the external circuitry — it is possible to construct an incremental equivalent circuit from which the small-signal or a-c performance may be predicted. Such an equivalent circuit is shown in Figure 22.



NOTE:  $C_{gss} = C_{iss} = C_{gs} + C_{gd}$   
 $C_{dss} = C_{oss} = C_{gd} + C_{ds} \cong C_{gd} = C_{rss}$

**Incremental Equivalent Circuit for the Junction FET**  
**Figure 22**

The equivalent capacitance from the gate to the source,  $C_{gs}$ , is shunted by a very large input resistance,  $r_{gs}$ , with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance  $r_{gd}$ . (For most purposes,  $r_{gs}$  and  $r_{gd}$  may be neglected, and the gate impedance of the FET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance  $C_{ds}$  — which stems from the header material — is shunted by the incremental channel resistance,  $r_{ds}$ . This resistance is capable of wide variations, depending on bias conditions. Since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition,  $r_{ds}$  will be on the order of megohms.

The incremental channel current is given by the transconductance,  $g_{fs}$ , multiplied by the incremental gate voltage. For the small signal,  $v_{gs}$ , this is manifested in the equivalent circuit by the current generator  $g_{fs}v_{gs}$ . Notice that the conventional direction of flow of this current is such that  $i_d$  flows into the FET, in a “positive” direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of  $g_{fs}$  and  $r_{ds}$  can be measured as previously mentioned; there remains only the requirement to establish the methods of determining  $C_{gs}$  and  $C_{gd}$ .

First, assume that the FET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to a-c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gs} \text{ (or } C_{iss}) = C_{gs} + C_{gd} \tag{9}$$

Second, assume that the gate and source are short-circuited to a-c in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss} \text{ (or } C_{oss}) \approx C_{gd} \tag{10}$$

The alternative symbols  $C_{iss}$  and  $C_{oss}$  simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for  $C_{gd}$  is  $C_{rss}$ , which refers to the “reverse” capacitance.

In data sheets, it is customary to state  $(= C_{iss}) C_{gss}$  and  $C_{dss} (= C_{oss})$ .  $C_{rss}$  is often given in place of  $C_{oss}$  because if  $C_{ds} \ll C_{oss}$ , which is usually the case, then  $C_{rss} \cong C_{oss}$ . Equations (9) and (10) can be used in those instances where it is necessary to extract  $C_{gs}$  and  $C_{gd}$ , as in

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \tag{11}$$

and

$$C_{gd} = C_{rss} \tag{12}$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the values given in the data sheet for the Siliconix E202 N-channel FET. They are given as

$$C_{iss} \text{ (at } V_{DS} = 20 \text{ V and } f = 1 \text{ MHz)} = 5 \text{ pF max.}$$

and

$$C_{rss} \text{ (at } V_{DS} = 20 \text{ V and } F = 1 \text{ MHz)} = 2 \text{ pF max.}$$

Hence, at a drain-source voltage of 20 V and a frequency of 1 MHz,  $C_{gs} = 5 - 2 = 3 \text{ pF}$  maximum. Even though the FET is physically symmetrical, bias conditions have forced the capacitances to be unequal.



## APPLICATION NOTE

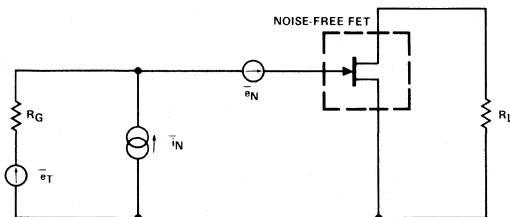
# Audio-Frequency Noise Characteristics of Junction FETs

### INTRODUCTION

The purpose of this application note is to identify and characterize audio frequency noise in junction field-effect transistors. Emphasis is placed on basic device characteristics rather than on end applications, since it is important for the circuit designer to know the salient noise behavior of the FET, and how those characteristics may be specified by production-oriented test parameters.

#### Defining FET Noise Figure

For analysis, it is convenient to represent noise in a FET by assuming that an ideal noise-free device has two external noise sources,  $e_N$  and  $i_N$ . These noise sources are chosen to have the same output as would an actual noisy FET. An equivalent circuit is shown in Figure 1.



Representing Noise in an Ideal FET  
Figure 1

A noise factor (F) is a Figure of Merit of a device with respect to the resistance of a generator. To calculate a noise

factor, a source resistor  $R_G$ , with a thermal noise voltage  $e_T$ , is added to the circuit.

A noise factor (F) may be defined as

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to thermal noise of } R_G}$$

or

$$F = \frac{\text{Noise power output due to } R_G + \text{noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Gain X noise power of FET referred to input}}{\text{Gain X noise power due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power of FET referred to input}}{\text{Noise power due to } R_G}$$

The thermal noise voltage across  $R_G$  is<sup>(1)</sup>

$$e_T = \sqrt{4kTR_GB} \quad (1)$$

where  $k = 1.380 \times 10^{-23}$  Joules/ $^{\circ}$ K (Boltzmann's Constant),  $T =$  temperature in  $^{\circ}$ K, and  $B =$  bandwidth in Hz. Therefore noise power due to  $R_G$  is

$$\frac{e_T^2}{R_G} = \frac{4kTR_GB}{R_G} = 4kTB \quad (2)$$

The noise power of the FET referred to the input is

$$\frac{\bar{e}_N^2}{R_G} + i_N^2 \cdot R_G \quad (3)$$

When expressions for the noise power of both the FET and  $R_G$  are substituted, the noise factor becomes

$$F = 1 + \frac{\bar{e}_N^2 + i_N^2 R_G^2}{4kTR_G B} \quad (4)$$

A noise figure (NF) expressed in dB indicates the presence of added noise power from the FET or another active device. The noise figure is always given with reference to a standard, specifically the generator resistance  $R_G$ :

$$NF = 10 \log_{10} [F] \quad (5)$$

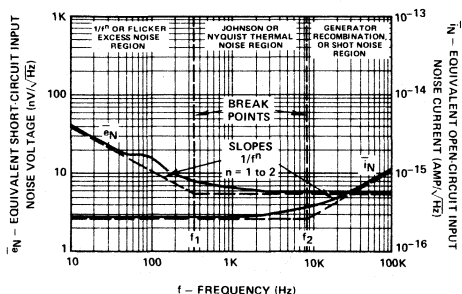
The noise figure of the FET is

$$NF = 10 \log_{10} \left[ 1 + \frac{\bar{e}_N^2 + i_N^2 R_G^2}{4kTR_G B} \right] \text{ dB} \quad (6)$$

When junction FET noise is expressed in terms of the noise figure (NF), an inherent disadvantage arises in that the noise figure value is dependent upon the value of the generator resistance,  $R_G$ . Therefore, the  $\bar{e}_N, i_N$  method remains as the best way to quantitatively express the noise characteristics of the FET itself.

### Describing Junction FET Noise Characteristics

Junction FET  $\bar{e}_N$  and  $i_N$  characteristics are frequency-dependent within the audio noise spectrum, and take a form as shown in Figure 2.



Characteristics of Junction FET Noise  
Figure 2

$\bar{e}_N$ , the equivalent short circuit input noise voltage (with the exception of the  $1/f^n$  region), is defined as<sup>(2)</sup>

$$\bar{e}_N = \sqrt{4kTR_N B} \quad (7)$$

where  $R_N \cong 0.67/g_{fs}$ , the equivalent resistance for noise. The  $\bar{e}_N$ , except in the  $1/f^n$  region, closely approximates the equivalent thermal noise voltage of the channel resistance.

In the so-called  $1/f^n$  region,  $\bar{e}_N$  is expressed as

$$\bar{e}_N = \sqrt{4KR_N B(1 + f_1/f^n)} \quad (8)$$

where  $n$  varies between 1 and 2 and is device- and lot-oriented.

The characteristic bulge in  $\bar{e}_N$  in the  $1/f^n$  region has been observed to some extent in all junction FETs submitted to test. The breakpoint or corner frequency shown as  $f_1$  in Figure 2 is lot- and device design-oriented, and varies from about 100 Hz to 1 kHz.

As indicated in Equations (7) and (8),  $\bar{e}_N$  is inversely proportional to the square root of the transconductance of the FET ( $\bar{e}_N \propto 1/\sqrt{g_{fs}}$ ).  $\bar{e}_N$  can be lowered by a factor of  $1/\sqrt{N}$  if  $N$  devices with matched electrical characteristics are connected parallel. For example, when

$$N = 2 \quad (9)$$

let

$$\bar{e}_{N1} = \bar{e}_{N2} \quad (10)$$

and let

$$g_{fs1} = g_{fs2} \quad (11)$$

Thus,

$$g_{fs \text{ TOTAL}} = 2 g_{fs1} \text{ or } 2 g_{fs2} \quad (12)$$

From Equation (7)

$$\bar{e}_{N1} = \sqrt{4kT(0.67/g_{fs1})B} \quad (13)$$

and

$$\bar{e}_{N \text{ TOTAL}} = \sqrt{4kT(0.67/2g_{fs1})B} \quad (14)$$

Thus,

$$\bar{e}_{N \text{ TOTAL}} = \frac{1}{\sqrt{2}} \bar{e}_{N1} \quad (15)$$

A second way to achieve low  $\bar{e}_N$  is to use a device with a large gate area. Empirically,  $\bar{e}_N$  is inversely proportional to the square of the gate area ( $\bar{e}_N \propto 1/A_G^2$ ), independent of  $g_{fs}$ . This large gate area philosophy has been followed in the



design of the Siliconix 2N4867A FET, and noise performance of the device is discussed later in this Application Note. A major advantage of this type of design is that  $e_N$  is significantly lowered and  $\bar{i}_N$  also remains at a low value.

The equivalent open-circuit input noise current,  $\bar{i}_N$ , with the exception of the shot noise region shown in Figure 2, is due to thermally-generated reverse current in the gate channel junction. It is defined as

$$\bar{i}_N = \sqrt{2qI_G B} \quad (16)$$

where  $q = 1.602 \times 10^{-19}$  coulomb (the magnitude of the electron charge),  $I_G$  is the measured DC operating gate current in amperes, and  $B$  is bandwidth in Hz. The expression is accurate only when the measured gate current is the result of bulk device conductance. It is possible for the measured gate current to be due to conductance stemming from contamination across the leads of the semiconductor package.

At higher frequencies, as in the shot noise region shown in Figure 2,  $\bar{i}_N$  can be approximated as being equal to the Nyquist thermal noise current generated by a resistor:<sup>(3)</sup>

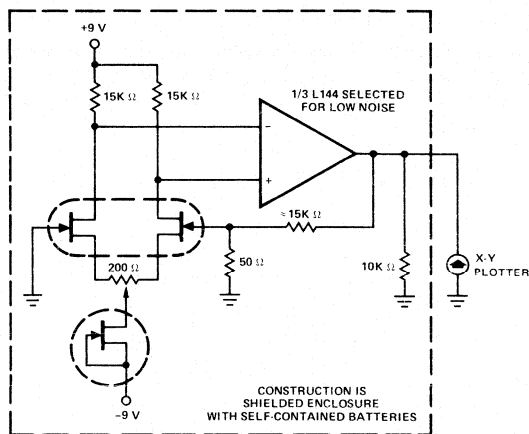
$$\bar{i}_N = \sqrt{\frac{4kTB}{R_p}} \quad (17)$$

where  $R_p$  is the real part of the gate-to-source input impedance. The breakpoint or corner frequency  $f_2$  in Figure 2 is lot- and device design-oriented and can vary from 5 kHz to 50 kHz.

Another form of noise found in junction FETs is known as "popcorn" or burst noise; the term popcorn noise was originated in the hearing aid industry because of noise or level shifts which are present in input stages, and which resemble the sound of corn popping.

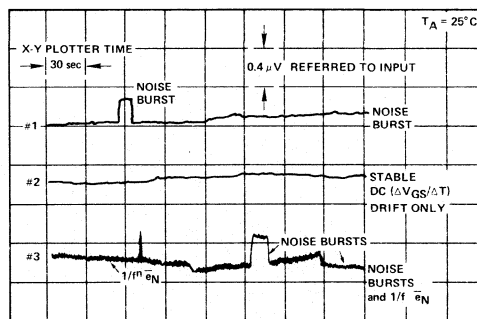
Popcorn noise is a form of random burst input noise current which remains at the same amplitude, and which is confined to frequencies of 10 Hz or lower. The suitability of a FET device is dependent on the amplitude of the burst, its duration, and its repetition rate. The origins of popcorn noise are not completely identified, but are believed to be caused by intermittent contact in aluminum-silicon interfaces and by contamination in the oxidation processes.

A test circuit to measure popcorn noise in differential junction FET amplifiers is shown in Figure 3. In practice, popcorn noise is evaluated on an engineering basis, and not on a production-line basis. No correlation between  $1/f^{1/2}$  noise at 10 Hz and popcorn noise has yet been found in junction FETs. However, if the amplitude of the burst is large and occurs frequently, then  $1/f^{1/2}$  noise voltage ( $e_N$ ) is masked and difficult to evaluate at 10 Hz.



Test Circuit to Measure Popcorn Noise  
Figure 3

The graph in Figure 4 shows "moderate" burst noise observed in a group of junction FET differential amplifiers which were measured in the test circuit.



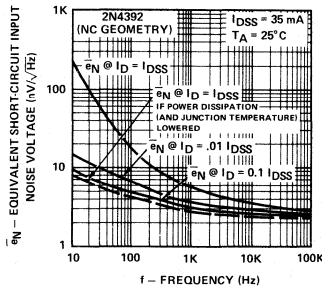
Popcorn Noise in Differential Amplifiers  
Figure 4

### Operating Point Considerations

Unlike bipolar transistors, where  $e_N$  and  $\bar{i}_N$  characteristics vary directly with change in collector current ( $I_C$ ), similar characteristics in junction FETs will vary only slightly as drain current ( $I_D$ ) is varied. This is true so long as the FET is biased so that the drain-source voltage is greater than the pinch-off voltage ( $V_{DS} > V_p$  or  $V_{GS(off)}$ ).

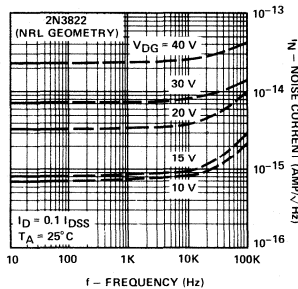
The  $e_N$  in junction FETs will be lowest when the devices are operated at  $V_{GS} = 0$  ( $I_D = I_{DSS}$ ), where transconductance ( $g_{fs}$ ) is at its highest value. This will be true only if device dissipation is maintained very low in relation to the total dissipation capability of the FET.

The curves in Figure 5 illustrate changes in  $\bar{e}_N$  as the operating drain current ( $I_D$ ) is varied. Note that the lowest  $\bar{e}_N$  did not occur at  $V_{GS} = 0$ , because of high power dissipation and a resultant rise in junction temperature at the operating point.



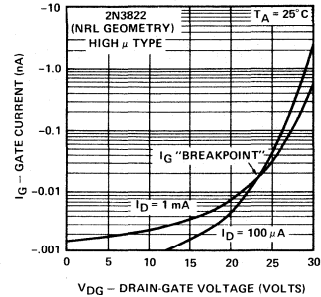
$\bar{e}_N$  Changes vs  $I_D$  Variations  
Figure 5

The optimum (lowest)  $\bar{i}_N$  in depletion-mode junction FETs should occur at  $V_{GS} = 0$  ( $I_D = I_{DSS}$ ). In practice, very little change will be seen in  $\bar{i}_N$  when the operating point is changed, provided that the drain-gate voltage is maintained below the gate current ( $I_G$ ) breakpoint and power dissipation is kept at a low level. The curves in Figure 6 illustrate  $\bar{i}_N$  characteristics as a function of drain-gate voltage at points below, on, and above the  $I_G$  breakpoint voltage.

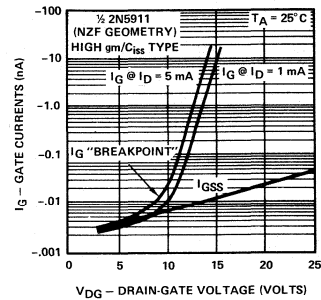


$\bar{i}_N$  Characteristics as Function of Drain-Gate Voltage  
Figure 6

In circuit design, particular attention must be paid to drain-gate voltage ( $V_{DG}$ ) to minimize gate current ( $I_G$ ) under operating conditions. The critical drain-gate voltage ( $I_G$  breakpoint voltage) can be anywhere from 8 to 40 V, depending on device design.<sup>(4)</sup> Gate operating current ( $I_G$ ) should not be considered equal to gate reverse current ( $I_{GSS}$ ) in linear amplifier applications.  $I_{GSS}$  is only an indication of reverse-biased junction leakage under non-operating conditions. The Curves in Figures 7 and 8 show how  $I_G$  breakpoint is related to basic device design. Device designs with a high  $g_{fs}/C_{iss}$  ratio have low breakpoint voltages, typically at  $V_{DG} = 10$  V, whereas high  $\mu$  devices ( $\mu = r_{ds} \cdot g_{fs}$ ) have much higher  $I_G$  breakpoints, typically  $V_{DG} = 20 - 30$  V.



Gate Operating Current vs Drain-Gate Voltage  
Figure 7

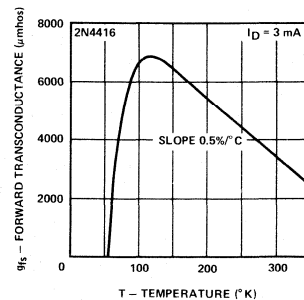


Gate Currents vs Drain-Gate Voltage  
Figure 8

Characteristics of  $\bar{e}_N$  and  $\bar{i}_N$  at Low Temperature

Three equations presented earlier ( (7), (16) and (17) ) show that  $\bar{e}_N$  and  $\bar{i}_N$  are temperature dependent.  $\bar{e}_N$  and  $\bar{i}_N$  are proportional to  $\sqrt{T}$ , and both will be reduced if the temperature is lowered. In Equation (16),  $\bar{i}_N$  is proportional to  $\sqrt{I_G}$ ;  $I_G$  will halve for each temperature drop of 10 to 11°C.  $\bar{e}_N$  is also proportional to  $\sqrt{R_N}$ , where  $R_N \approx 0.67/g_{fs}$ . Thus when  $g_{fs}$  is increased, which is typical of junction FETs operating at low temperature,  $\bar{e}_N$  will also lower.

In Figure 9,  $g_{fs}$  has been plotted vs temperature for a silicon junction FET, and the low temperature limitation caused by a dropoff in  $g_{fs}$  is clearly shown.



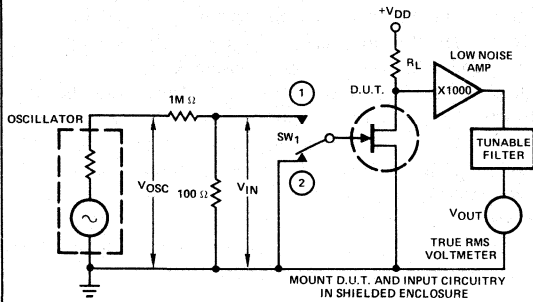
$g_{fs}$  vs Temperature  
Figure 9

In connection with the plot of  $g_{fs}$  vs temperature, note that the relationship can vary from approximately 0.2% to 1% per degree C. The  $g_{fs}$  slope depends upon the basic design of the FET, and upon the proximity of the drain current operating point to  $I_{DZ}$ , the zero temperature coefficient point.

The major application for junction FETs at low temperature is in charge-sensitive amplifiers.<sup>(5)</sup> For best performance in this type of application, a high  $g_{fs}/C_{iss}$  ratio is required. Recommended Siliconix FET types for such applications are the 2N4416 (NH geometry) and the U311 (NZA geometry).

**Test Measurements**

By definition,  $\bar{e}_N$  and  $\bar{i}_N$  are referred to the input of the device under test. To measure  $\bar{e}_N$ , the test circuit shown in Figure 10 will prove useful.



Test Circuit to Measure  $\bar{e}_N$   
Figure 10

The following procedure should be used to make the  $\bar{e}_N$  test:

1. Set tunable filter to required  $f_{low}$  and  $f_{high}$ . Adjust oscillator to mean center frequency ( $f_{mean} = [f_{low} \cdot f_{high}]^{1/2}$ ).
2. Set  $V_{osc}$  to 100 mV with Switch 1 in position ①. Compute  $V_{in1} = 10^{-1} \times \frac{10^2}{10^6} = 10^{-5} V = 10 \mu V$ .
3. Measure  $V_{out1}$ . Compute overall gain as  $A_v = \frac{V_{out1}}{V_{in1}} = \frac{V_{out1}}{10 \mu V}$ .
4. Set Switch 1 to position ② and measure  $V_{out2}$ . Compute  $V_{in2}$ , the equivalent short-circuit input noise voltage ( $\bar{e}_N$ ), using  $A_v$  from Step 3.  $V_{in2} = \frac{V_{out2}}{A_v} = \bar{e}_N$  in volts over bandwidth  $f_{low}$  to  $f_{high}$ .

An alternate method of performing the above test is to use a Quan-Tech Transistor Noise Analyzer consisting of a Model 2173 Control Unit and a Model 2181 Filter. The analyzer has provision for measuring  $\bar{e}_N$  and determining NF with various values of  $R_G$  in FET and bipolar devices with selectable test conditions. The measuring system has a constant gain of 10,000. The analyzer records output noise at selected frequencies between 10 Hz and 100 kHz in the device under test, with the scale shown as the actual output divided by 10,000. This is then the output noise referred to the input. The equivalent bandwidth for testing is 1 Hz.

There are certain instances where the test circuit or the Transistor Noise Analyzer are not adequate to measure  $\bar{e}_N$  at certain frequencies over certain bandwidths in the  $1/f^n$  region. The rms noise over a bandwidth from  $f_{low}$  to  $f_{high}$ , where there is a  $1/f^n$  characteristic over the entire range, can be computed as

$$\bar{e}_N = \left[ \bar{e}_N \text{ known} \right] \cdot \left[ f_{known} \cdot \ln \left( \frac{f_{high}}{f_{low}} \right) \right]^{1/2n} \quad (18)$$

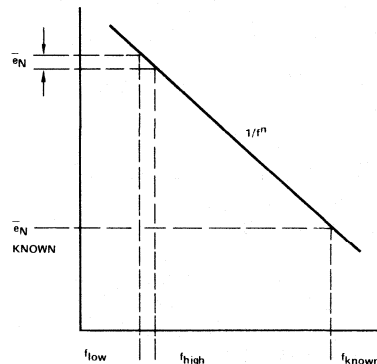
Figure 11 represents this equation graphically. For example,  $\bar{e}_N \text{ known} = 70 \times 10^{-9} V/\sqrt{Hz}$  at 10 Hz. How much noise is in the band from 4.5 to 5.5 Hz? The noise has a  $1/f^1$  characteristic over the entire range. Thus

$$\bar{e}_N = \left[ 70 \times 10^{-9} \right] \cdot \left[ 10 \cdot \ln \left( \frac{5.5}{4.5} \right) \right]^{1/2} \text{ Volts} \quad (19)$$

or

$$\bar{e}_N = 99.16 \times 10^{-9} V/\sqrt{Hz} @ 4.975 \text{ Hz}, \quad (20)$$

4.975 Hz is the mean center frequency where  $f_{mean} = (f_{low} \cdot f_{high})^{1/2}$ .



Computing rms Noise Over a Bandwidth  
Figure 11

$\bar{i}_N$  measurements are difficult to implement at best. At frequencies below  $f_2$  in Figure 2,  $\bar{i}_N$  is assumed to have a constant level or "white" noise characteristic which may be correlated to gate current,  $I_G$ . From Equation (16)  $I_G$  is established as the measured bulk gate current. Because measured gate current ( $I_G$ ) is the result of all conductances at the gate, the resultant gate current and the computed  $\bar{i}_N$  due to bulk material can be assumed to be this value or less.

The total equivalent input noise of the FET can be approximated by<sup>(6)</sup>

$$\bar{e}_{ni}^2 = \bar{e}_T^2 + \bar{e}_N^2 + \bar{i}_N^2 \cdot R_G^2 \quad (21)$$

where  $\bar{e}_T^2$  is the thermal noise of the generator resistance  $R_G$  and  $\bar{e}_{ni}^2$  is the total noise referred to the input. This approximation assumes that the equivalent noise voltage and the current generators vary independently. Equation (21) implies that  $\bar{i}_N^2$  can be calculated if  $\bar{e}_N^2$ ,  $\bar{e}_T^2$  and total noise  $\bar{e}_{ni}^2$  are known. The difficulty here is that in MOS or junction FETs, the  $R_G$  must be very large to detect the anticipated small value of  $\bar{i}_N$ . However, when  $R_G$  is very large  $\bar{e}_T^2$  is much greater than  $\bar{i}_N^2 \cdot R_G^2$ . For example, over a 1 Hz bandwidth at 25°C, if  $R_G$  is equal to 100 MΩ, then

$$\begin{aligned} \bar{e}_T^2 &= 4kTR_G = 4 \times 1.38 \times 10^{-23} \times 2.95 \times 10^2 \times 10^8 = \\ &1.63 \times 10^{-12} \text{ V}/\sqrt{\text{Hz}}. \end{aligned} \quad (22)$$

Anticipated  $\bar{i}_N$  is

$$\bar{i}_N \approx 10^{-15} \text{ Amperes}/\sqrt{\text{Hz}} \quad (23)$$

and

$$\bar{i}_N^2 = 10^{-30} \text{ Amperes}/\sqrt{\text{Hz}}. \quad (24)$$

Thus

$$\bar{i}_N^2 \cdot R_G^2 = 10^{-30} \cdot 10^{16} = 10^{-14} \text{ V}/\sqrt{\text{Hz}}. \quad (25)$$

Therefore,  $\bar{i}_N^2 \cdot R_G^2$  is much less than  $\bar{e}_T^2$ , which renders this method of finding  $\bar{i}_N$  impractical for most common MOS FETs or junction FETs.

An improved method of measuring  $\bar{i}_N$  is to substitute a low-loss mica capacitor for resistor  $R_G$ . The mica capacitor by definition does not have equivalent thermal noise voltage, and thus Equation (21) becomes

$$\bar{e}_{ni}^2 = \bar{e}_N^2 + \bar{i}_N^2 \cdot X_C^2 \quad (26)$$

(where  $X_C$  = capacitive reactance)

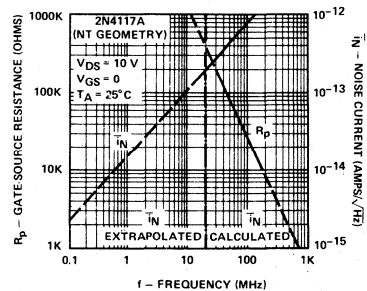
or

$$\bar{i}_N = \frac{(\bar{e}_{ni}^2 - \bar{e}_N^2)^{1/2}}{X_C} \quad (27)$$

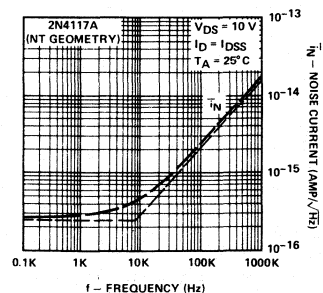
When a 10 pF mica capacitor was used in the evaluation circuit (up to a frequency of 100 Hz) a correlation of from 80 to 90% was obtained when compared to  $\bar{i}_N^2$  computed from measured gate current readings.

At frequencies above 100 Hz direct computation of  $\bar{i}_N$  via the capacitor method becomes unwieldy because of the rapid decrease in capacitor reactance at these frequencies.

In calculating  $\bar{i}_N$  at higher frequencies, an alternate method is to measure ( $R_p$ ) the real part of the gate-source impedance of the FET.<sup>(7)</sup> When  $R_p$  is measured at various frequencies, the equivalent short-circuit input noise current ( $\bar{i}_N$ ) can be computed as a function of frequency (See Equation (17)). A convenient instrument to measure  $R_p$  is the Hewlett-Packard Type 250A Rx meter or equivalent. The Type 250A Rx meter can measure  $R_p$  accurately up to 200K ohms. As is shown in Figure 12, this establishes the low frequency limit of 20 MHz for  $\bar{i}_N$  computed via direct measurement of  $R_p$  for the Siliconix FET Type 2N4117A. For frequencies between 100 Hz and 20 MHz,  $\bar{i}_N$  must be extrapolated, as is shown in Figures 12 and 13. For FET types with lower  $R_p$  (such as the Siliconix 2N4393)  $\bar{i}_N$  can be computed down to 2 MHz, and hence extrapolated  $\bar{i}_N$  between 100 Hz and 100 kHz is more accurate.

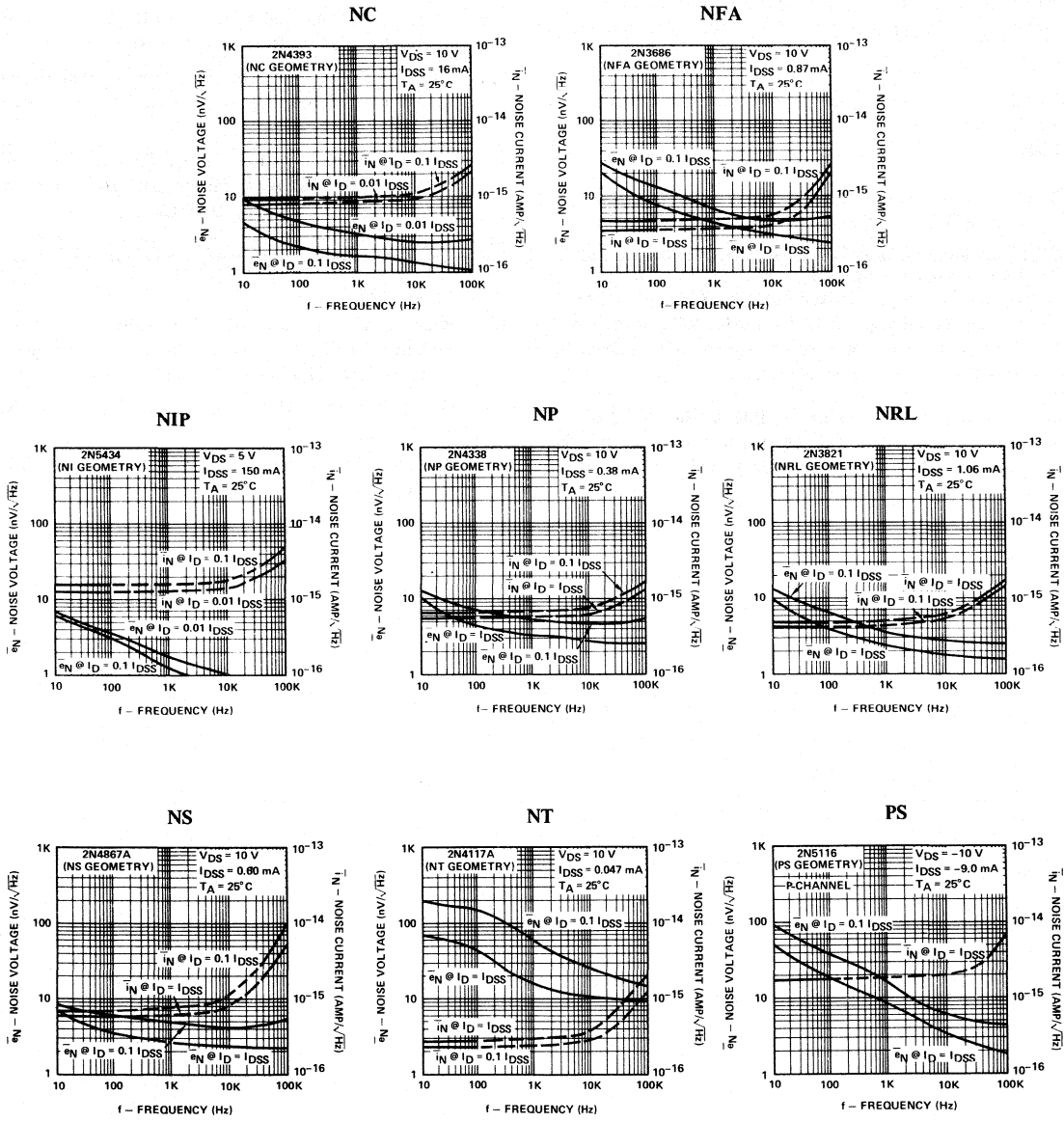


Low Frequency Limit for Calculated  $\bar{i}_N$   
Figure 12



Extrapolated  $\bar{i}_N$  vs Frequency  
Figure 13

The following are representative  $e_N$ ,  $i_N$  curves for Siliconix J-FET products. Of particular importance is the geometry which by its design governs the basic noise characteristics of product types derived from it.



FET Noise Characteristics by Geometry  
Figure 14

## CONCLUSION

Contemporary junction FETs have noise voltages ( $\bar{e}_N$ ) equal to those found in low-noise bipolar transistors. Each type of device has a different operating mechanism: the FET is voltage-actuated, while the bipolar transistor is current-actuated. Hence, FETs have an inherently lower noise current ( $\bar{i}_N$ ) and are preferred over bipolar devices in most audio-frequency applications where low-noise performance is a design requirement.

When bias points are properly selected, as described in this Application Note, the excellent low-noise characteristics of high  $g_{fs}$  junction FETs can be realized.

The curves shown in Figure 14 are representative of  $\bar{e}_N$  and  $\bar{i}_N$  performance of Siliconix junction FETs. Of particular importance in these curves is the process geometry by which the basic design of the FET governs the noise characteristics of product types derived from it. Readers are invited to refer to the Siliconix FET catalog for full geometry performance data, and for specific part numbers stemming from the generic process geometries.

In the measurement section of this Application Note, it was shown that direct  $\bar{e}_N$  measurements can readily be made.  $\bar{i}_N$  can be guaranteed at frequencies below 100 Hz by measuring the DC operating gate current ( $I_G$ ). When  $I_G$  is

known,  $\bar{i}_N$  can be extrapolated from frequencies below 100 Hz to predict noise performance at frequencies to 100 kHz.

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# APPLICATION NOTE

## FETs for Video Amplifiers

### INTRODUCTION

The field-effect transistor lends itself well to video amplifier applications. Gain bandwidth products in excess of 250 MHz may be easily achieved using simple one or two transistor circuits. DC input resistances in the tens of megohms range may also be easily achieved while input capacitances may be significantly reduced to less than 1 pF by well known circuit techniques. Video amplifiers have applications in communications and pulse amplifying circuits and normally operate up to 100 MHz.

### Behavior of FET Input Resistance

A prime FET parameter, input impedance, has a large effect in determining the frequency response of a FET video amplifier. It is not a simple RC network but one in which the real and imaginary parts are a function of frequency.

The voltage generator source resistance  $R_g$  and the FET input impedance  $Z_{in}$  form a frequency sensitive attenuation network. The larger the  $R_g$ , the worse will be the frequency response, and vice versa. Examining this in greater detail, consider the input equivalent circuit of a FET connected in the common source configuration,

where

- $R_{gs}$  and  $R_{gd}$  = bulk series gate resistance
- $C_{gs}$  and  $C_{gd}$  = bulk series gate capacitance
- $G_{oss}$  = output conductance

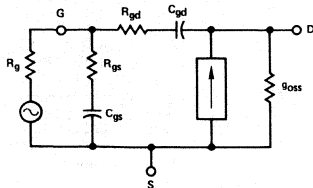


Figure 1

For this analysis the gate source leakage resistance has been ignored due to its high value. Redrawing the input equivalent circuit as a simple parallel RC combination results in

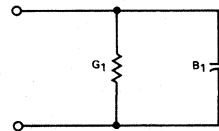


Figure 2

where

$$G_1 = \text{Re } |Y_{in}| = \frac{\omega^2 [T_1 C_1 (1 + \omega^2 T_2^2) + T_2 C_2 (1 + \omega^2 T_1^2)]}{1 - (\omega^2 T_1 T_2)^2 + \omega^2 (T_1^2 + T_2^2)} \quad (1)$$

and

$$B_1 = \text{Im } |Y_{in}| = \frac{\omega [C_1 (1 + \omega^2 T_2^2) + C_2 (1 + \omega^2 T_1^2)]}{1 - (\omega^2 T_1 T_2)^2 + \omega^2 (T_1^2 + T_2^2)} \quad (2)$$

where

$$\begin{aligned} T_1 &= C_{gd} R_{gd} \\ T_2 &= C_{gs} R_{gs} \end{aligned} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4) while the input reactance is inversely proportional to the frequency (see Figure 3).

In common-source circuits,  $1/G_1$  will typically fall to  $< 2K$  ohms at 100 MHz while  $C_1$  remains substantially constant at least up to 1000 MHz. Figures 3 and 4 below exhibit these relationships.

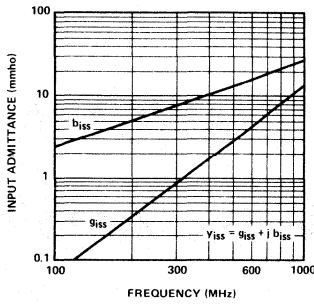


Figure 3

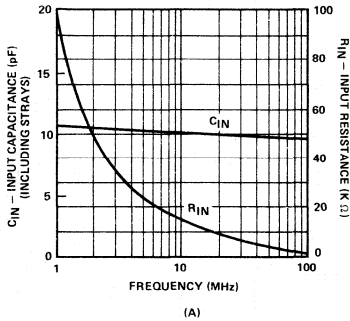
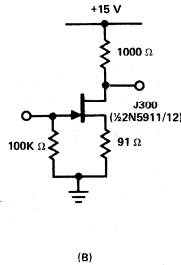


Figure 4



(B)

To maintain low input capacitance, and thus a high input impedance over a wide frequency range, feedback may be applied to most circuits. Such techniques are explored in "FET and Bipolar Cascade" section (page 5). The effect of  $R_g$  on the frequency response is shown in Figures 6, 9, 11, 13 where various amplifier configurations are investigated.

**Circuits to Consider**

Five video amplifier circuits are considered. They are:

- Common-Source Configuration
- Shunt-Peaked Common-Source Configuration
- Source Follower
- Cascode Amplifier
- FET and Bipolar Cascade

**Common-Source Circuit<sup>1</sup>**

The circuit of Figure 5 features high input impedance and high voltage gain. The drain resistor is set at 560 ohms to maintain good bandwidth which, with 50-ohm generator impedance, is determined primarily by the drain load components. These are:

$$R_D = 560 \Omega \quad (4)$$

$$C_T = C_{gd} + C_D + C_S \quad (5)$$

$C_{gd} = 2.0$  pF,  $C_D$  the VTVM probe,  $2.0$  pF, and  $C_S$  is circuit stray capacitance of  $3$  pF.

$$C_T = 2 + 2 + 3 = 7 \text{ pF} \quad (6)$$

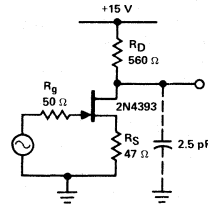


Figure 5

The 3-dB frequency  $\omega_3$  is given by:

$$\omega_3 = \frac{1}{C_T R_D} \quad (7)$$

$$= \frac{1}{7 \times 10^{-12} \times 560} \quad (8)$$

$$\omega_3 = 255 \times 10^6 \quad (9)$$

$$f_3 = 39 \text{ MHz} \quad (10)$$

The low frequency voltage gain for this configuration is given by:

$$A_V = \frac{g_{fs} R_D}{1 + g_{fs} R_S} \quad (11)$$

$$A_V = 4.9 \quad (12)$$

where

$g_{fs} = 15$  mmho when  $I_D = 12$  mA, the quiescent current

$$R_D = 560 \Omega \quad (13)$$

$$R_S = 47 \Omega \quad (14)$$

**Measured Performance**

Figure 6 shows the frequency response of the circuit. The low-frequency gain was measured at 4.5 and the 3-dB bandwidth at 44 MHz giving a gain bandwidth product of 197 MHz. This compares with a calculated gain bandwidth of 191 MHz.

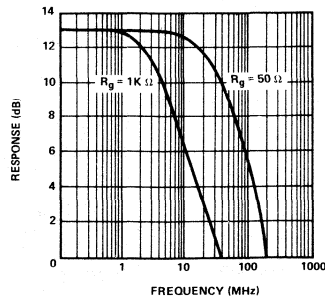


Figure 6



**Effect of Increasing Generator Impedance**

If the generator resistance  $R_g$  is increased to 1K ohm, the input time constant of the FET is increased. The bandwidth of the amplifier is now determined primarily by the input time constant which consists of generator impedance ( $R_g = 1K$  ohm) shunted by  $C_{in}$  ( see Figure 7).

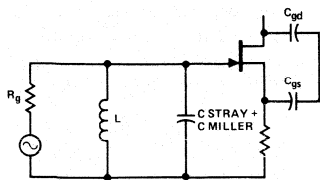


Figure 7

where

$$C_{in} = \left(1 + \frac{g_{fs}R_D}{1 + g_{fs}R_S}\right) C_{gd} + \left(1 - \frac{g_{fs}R_S}{1 + g_{fs}R_S}\right) C_{gs} + \text{Strays}$$

$$= (5.9 \times 3.5) + (0.6 \times 10) + 3. \quad (15)$$

$$C_{in} = 30 \text{ pF} \quad (16)$$

where

$$C_{gd} = 3.5 \text{ pF} \quad (17)$$

$$C_{gs} = 10 \text{ pF} \quad (18)$$

The corresponding 3-dB frequency is given by:

$$\omega_3 = \frac{1}{C_{in}R_g} \quad (19)$$

$$= \frac{1}{30 \times 10^{-12} \times 10^3} = \frac{10^9}{30} \quad (20)$$

$$f_3 = 5.3 \text{ MHz} \quad (21)$$

which agrees closely with the measured bandwidth as shown in Figure 6.

**Shunt-Peaked Common-Source Circuit**

The frequency response of the resistance-loaded common-source circuit may be significantly extended by shunt peaking at the gate and/or drain. Consider first the gate circuit. Here an inductor may be connected in shunt with the gate and set to such a value that it forms a tuned circuit with the FET input capacitance. The frequency of resonance is determined by:

$$f_0 = \frac{1}{2\pi\sqrt{LC_{in}}} \quad (22)$$

where

$$C_{in} = C_{iss} + C_{Stray} + C_{Miller} \quad (23)$$

The response of an input signal of frequency  $f_0$  will then be boosted to an extent depending on the loaded Q of the tuned circuit; the loaded Q in turn is dependent on the unloaded Q of inductor L,  $R_g$  and the FET input resistance.

Next consider shunt peaking in the drain circuit. In Figure 8 the inductor L is set to such a value that a low Q tuned circuit is formed; the resonating capacitance C is the parallel combination of  $C_{gd}$  plus stray and load capacitances. For a flat response, the LC circuit is tuned to the 3-dB frequency of the resistance loaded circuit of Figure 5. (See Appendix.)

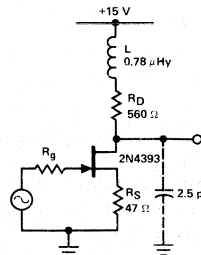


Figure 8

The required value of L is:

$$L = \frac{R_D^2 C}{2}, \text{ and for the circuit in Figure 8.} \quad (24)$$

$$= 0.78 \mu\text{H} \quad (25)$$

where

$$R_D = 560 \Omega \quad (26)$$

$$C = C_{gd} + C_{Stray} + C_{VTVM \text{ PROBE}} \quad (27)$$

$$C = 1.2 + 1.3 + 2.5 = 5 \text{ pF} \quad (28)$$

Due to the low circuit Q (about 5), the value of L is not critical.

The 3-dB bandwidth shown in Figure 9 now extends to 67 MHz giving a gain bandwidth product of:

$$67 \times 4.2 = 281 \text{ MHz} \quad (29)$$

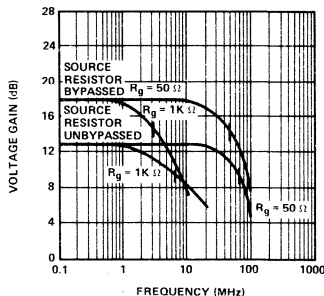


Figure 9

When  $R_S$  is bypassed by a 0.1 capacitor, the low frequency voltage gain is given simply by:

$$A_V = g_{fs} R_D \quad (30)$$

$$= 15 \times 10^{-3} \times 560 \quad (31)$$

$$= 8.4 \text{ (18.5 dB)} \quad (32)$$

The gain bandwidth product tends to remain constant whether  $R_S$  is bypassed or not and this effect is shown in Figure 9.

### Source-Follower Circuit<sup>2</sup>

A J300 is used in the FET source-follower circuit, Figure 10, because of its low input capacitance and high  $g_{fs}$  which remains high at the frequency range of interest. A source follower exhibits a high input impedance and low output impedance. The real part of the output impedance is the reciprocal of  $g_{fs}$  which is independent of frequency up to about 600 MHz. The input capacitance is  $C_{gd} + C_{gs}(1 - A_V)$  which, in this case, is approximately 1.5 pF maximum. The input capacitance is also independent of frequency and independent of load when the load is larger than the output resistance  $R_O$ .

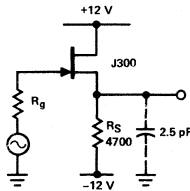


Figure 10

The frequency response is dependent mainly on the generator internal impedance. For example, when  $R_g$  is increased to 1K ohm the bandwidth falls to 80 MHz. In this particular circuit, the low-frequency voltage gain is 0.94.

The input resistance is proportional to  $1/f^2$  as explained in the section, "Behavior of Input Resistance," and at some high frequency will go negative, particularly if the source resistor is large. For example, with the circuit in Figure 10, the input resistance is high at 10 MHz but in the negative resistance region at 100 MHz. However, when  $R_S$  is 1000 ohms, the input resistance is real at this frequency.

The voltage gain of a source follower is given by:

$$A_V = \frac{g_{fs} R_S}{1 + g_{fs} R_S} \quad (33)$$

Thus  $A_V$  is almost independent of  $R_S$  when  $R_S$  is large. Using typical values for the J300 (or  $\frac{1}{2}$  2N5912) in Figure 10, the drain current is 3 mA,  $g_{fs}$  is 5 mmho and  $R_S$  4700 ohms,

$$A_V = 0.96$$

which is near the measured value of 0.94. Measured performance is shown in Figure 11. The output resistance of this source follower is given by:

$$R_O = \frac{1}{g_{fs}} = \frac{1}{5 \times 10^{-3}} = 200 \Omega \quad (34)$$

and in this circuit,  $R_O$  was measured at 165 ohms. The source follower is a useful versatile circuit which may be used as an impedance converter, level shifter, buffer stage, or as an input circuit to an op amp or feedback amplifier.

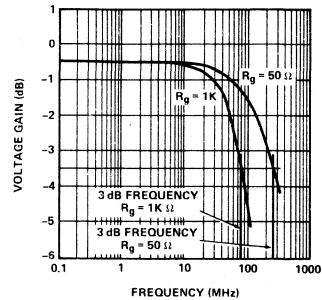


Figure 11

### Cascode Circuit

The cascode circuit has applications as a buffer amplifier for use with high stability oscillators or in low level power amplifiers<sup>2</sup> mainly due to its low reverse transfer characteristics. The advantages and considerations of this configuration, Figure 12, are similar to those listed for the common-source circuit. An extra advantage exists in the cascode circuit, namely the low input capacitance:

$$C_{in} = C_{gs} + (1 - A_V) C_{dg} \quad (35)$$

$$C_{in} = C_{iss} + C_{gd} \quad (36)$$

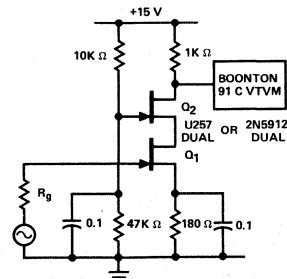


Figure 12

where  $A_V$  is the voltage gain from  $Q_1$  gate to  $Q_1$  drain which is essentially unity.  $C_{iss}$  for the U257 dual FET is 5 pF and  $C_{dg}$  is 1 pF, therefore

$$C_{in} = 5 + 1 = 6 \text{ pF, excluding strays of 4 pF}$$

Thus Miller effect is minimized and a good gain bandwidth product is achieved.

Figure 13 shows cascode frequency response. The voltage gain at low frequency is 15 dB ( $\times 5.6$ ) and the bandwidth is 24.5 MHz with a generator impedance of 50 ohms. Gain bandwidth product is 137 MHz.

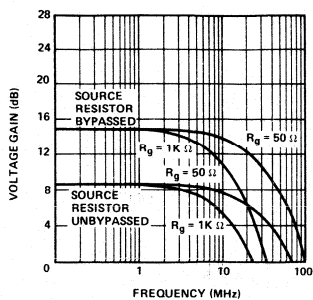


Figure 13

### FET and Bipolar Cascade

The FET and bipolar transistor combination of Figure 14 makes a good video amplifier because the FET input provides the voltage gain thus obtaining a superior gain bandwidth product. The feedback capacitor a-c couples the emitter to the drain. The a-c voltage at the gate is nearly equal to that at the source. This source voltage is d-c coupled to the base.

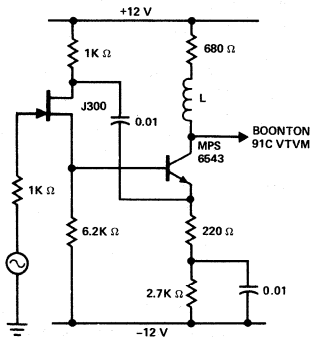


Figure 14

This produces an a-c voltage at the emitter whose amplitude is almost equal to that at the base. Thus at the FET,  $v_g \cong v_s \cong v_d$  and all three signals are in phase. In this way Miller effect capacitance is largely eliminated.

The frequency response of this circuit is controlled by the output time constant if  $f_t$  of the transistor is much greater than the amplifier bandwidth. In the circuit shown the a-c load is 2.5 pF.

### CONCLUSION

The input resistance of a FET is inversely proportional to the frequency squared, while the input capacitance remains constant to at least 1000 MHz.

Several video amplifier configurations are considered. The common-source circuit is considered first: in the example, the low frequency gain is 4.5 and the 30-dB bandwidth 44 MHz (gain bandwidth 197 MHz). By shunt peaking in the drain circuit, gain bandwidth is increased to 260 MHz. The simple source-follower circuit gives a gain near unity with GBW almost 300 MHz and an output resistance of  $1/g_{fs}$ . The cascode circuit features a low input capacitance and GBW of 137 MHz. The circuit featuring the best gain bandwidth is the FET and bipolar combination. A gain of 11 dB and bandwidth of 90 MHz is achieved.

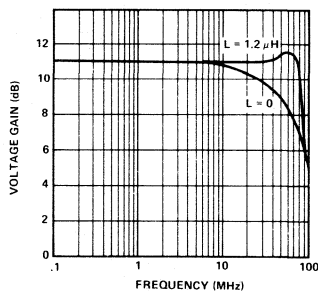


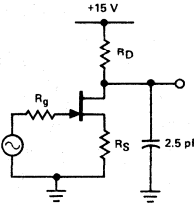
Figure 15

APPENDIX

Selection of Video Amplifier Designs with Performance Summary

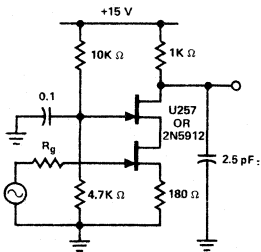
Note. All output voltages measured with Boonton 91C VTVM.

Common Source Stage



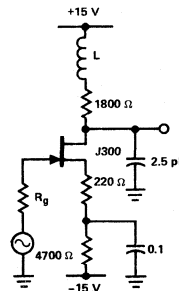
| Device | R <sub>g</sub><br>Ω | R <sub>S</sub><br>Bypassed | R <sub>S</sub><br>Ω | R <sub>D</sub><br>Ω | Gain | dB   | C <sub>in</sub><br>pF | BW<br>MHz | GBW<br>MHz |
|--------|---------------------|----------------------------|---------------------|---------------------|------|------|-----------------------|-----------|------------|
| 2N4393 | 50                  |                            | 47                  | 560                 | 4.5  | 13.0 | 44                    | 197       |            |
|        | 50                  | x                          | 47                  | 560                 | 7.5  | 17.5 | 40                    | 300       |            |
|        | 1K                  |                            | 47                  | 560                 | 4.5  | 13.0 | 5.0                   | 22        |            |
|        | 1K                  | x                          | 47                  | 560                 | 7.5  | 17.5 | 3.5                   | 26        |            |
| J300   | 50                  |                            | 91                  | 1K                  | 3.8  | 11.6 | 11.0                  | 27.5      | 103        |
|        | 50                  | x                          | 91                  | 1K                  | 6.3  | 16.0 | 14.5                  | 30.0      | 189        |
| 2N5912 | 1K                  |                            | 91                  | 1K                  | 3.8  | 11.6 | 11.0                  | 9.5       | 36         |
|        | 1K                  | x                          | 91                  | 1K                  | 6.3  | 16.0 | 14.5                  | 6.5       | 41         |
| 2N4416 | 50                  |                            | 120                 | 1.5K                | 3.9  | 11.8 | 11.5                  | 25        | 98         |
|        | 50                  | x                          | 120                 | 1.5K                | 6.2  | 15.8 | 13                    | 19        | 118        |
|        | 1K                  |                            | 120                 | 1.5K                | 3.9  | 11.8 | 11.5                  | 8         | 31         |
|        | 1K                  | x                          | 120                 | 1.5K                | 6.2  | 15.8 | 13                    | 7         | 44         |

Cascode



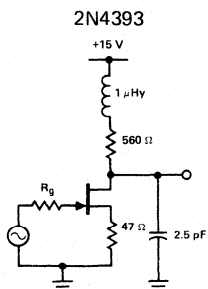
| R <sub>g</sub><br>Ω | R <sub>S</sub><br>Bypassed | Gain | dB  | C <sub>in</sub><br>pF | BW<br>MHz | GBW<br>MHz |
|---------------------|----------------------------|------|-----|-----------------------|-----------|------------|
| 50                  |                            | 2.7  | 8.5 | 9                     | 27        | 73         |
| 50                  | x                          | 5.6  | 15  | 11.5                  | 27        | 151        |
| 1K                  |                            | 2.7  | 8.5 | 9                     | 9.5       | 73         |
| 1K                  | x                          | 5.6  | 15  | 11.5                  | 9.0       | 51         |

Common-Source Circuit

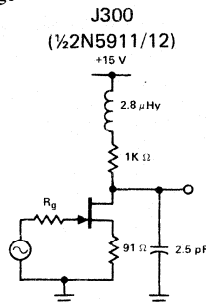


| R <sub>g</sub><br>Ω | L<br>μH | Gain | dB | C <sub>in</sub><br>pF | BW<br>MHz | GBW<br>MHz |
|---------------------|---------|------|----|-----------------------|-----------|------------|
| 50                  | 0       | 3.5  | 11 | 2                     | 20        | 70         |
| 1K                  | 0       | 3.5  | 11 | 2                     | 11        | 38.5       |
| 50                  | 8       | 3.5  | 11 | 2                     | 37        | 130        |
| 1K                  | 15      | 3.5  | 11 | 2                     | 17        | 60         |

Shunt-Peaked Common-Source Stage

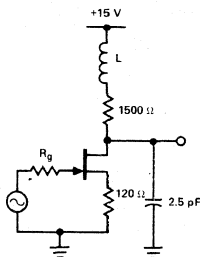


| $R_g$<br>$\Omega$ | $R_S$<br>Bypassed | Gain | dB   | BW<br>MHz | GBW<br>MHz |
|-------------------|-------------------|------|------|-----------|------------|
| 50                |                   | 4.2  | 12.5 | 66        | 277        |
| 50                | x                 | 7.5  | 17.5 | 54        | 405        |
| 1K                |                   | 4.2  | 12.5 | 6.0       | 25         |
| 1K                | x                 | 7.5  | 17.5 | 3.5       | 26         |



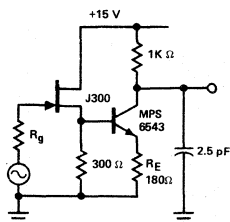
| $R_g$<br>$\Omega$ | $R_S$<br>Bypassed | Gain | dB   | BW<br>MHz | GBW<br>MHz |
|-------------------|-------------------|------|------|-----------|------------|
| 50                |                   | 3.9  | 11.8 | 67        | 262        |
| 50                | x                 | 6.3  | 16.0 | 67        | 421        |

2N4416

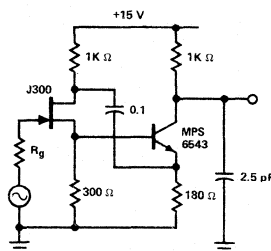


| $R_g$<br>$\Omega$ | L<br>$\mu H$ | $R_S$<br>Bypassed | Gain | dB   | BW<br>MHz | GBW<br>MHz |
|-------------------|--------------|-------------------|------|------|-----------|------------|
| 50                | 4            |                   | 3.9  | 11.8 | 45        | 175        |
| 50                | 4            | x                 | 6.2  | 15.8 | 40        | 248        |
| 50                | 5            | x                 | 6.2  | 15.8 | 45        | 279        |

Common-Drain Common-Emitter Stage

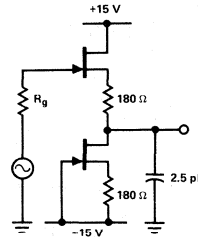
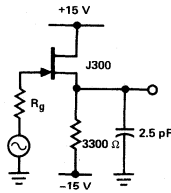


| $R_g$<br>$\Omega$ | $R_E$<br>Bypassed<br>(0.1 $\mu F$ ) | Gain | dB  | $C_{in}$<br>pF | BW<br>MHz | GBW<br>MHz |
|-------------------|-------------------------------------|------|-----|----------------|-----------|------------|
| 50                |                                     | 3    | 9.5 | 2.0            | 39        | 117        |
| 50                | x                                   | 25   | 28  | 2.0            | 21        | 525        |
| 1K                |                                     | 3    | 9.5 | 2.0            | 13        | 39         |
| 1K                | x                                   | 25   | 28  | 2.0            | 11        | 275        |



| $R_g$<br>$\Omega$ | Gain | dB | $C_{in}$<br>pF | BW<br>MHz | GBW<br>MHz |
|-------------------|------|----|----------------|-----------|------------|
| 50                | 5.6  | 15 | 1.0            | 32        | 179        |
| 1K                | 5.6  | 15 | 1.0            | 15        | 84         |

Source-Follower Circuit



| R <sub>g</sub><br>Ω | Gain | C <sub>in</sub><br>Stray pF | Total pF | R <sub>o</sub><br>Ω | BW<br>MHz | GBW<br>MHz |
|---------------------|------|-----------------------------|----------|---------------------|-----------|------------|
| 50                  | 0.92 | 2.2                         | 2.7      | 165                 | 350       | 326        |
| 1K                  | 0.92 | 2.2                         | 2.7      | 165                 | 55        | 50         |

Note. R<sub>o</sub> = output resistance of the source follower.

| Dual FET | R <sub>g</sub><br>Ω | Offset (Max)<br>(Input to Output) mV | Gain | BW<br>MHz | GBW<br>MHz |
|----------|---------------------|--------------------------------------|------|-----------|------------|
| U257     | 50                  | 100                                  | 0.98 | 70        | 69         |
| 2N5912   | 1K                  | 100                                  | 0.98 | 15        | 14.7       |
| U232     | 50                  | 10                                   | 0.98 | 85        | 83         |
|          | 1K                  | 10                                   | 0.98 | 13        | 12.7       |

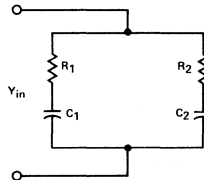
Derivation of Input Admittance Terms

where

$$R_1 = R_{gs} \quad C_1 = C_{gs} \quad (1)$$

$$R_2 = R_{gd} \quad C_2 = C_{gd} \quad (2)$$

$$s = j\omega$$



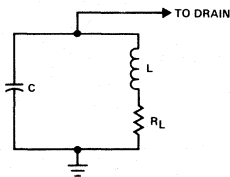
$$Y_{in} = \frac{sC_1}{R_1 C_1 s + 1} + \frac{sC_2}{R_2 C_2 s + 1} \quad (3)$$

$$= \frac{-\omega^2 C_1 C_2 (R_1 + R_2) + s(C_1 + C_2)}{(1 - \omega^2 R_1 R_2 C_1 C_2) + s(C_1 R_1 + C_2 R_2)} \quad (4)$$

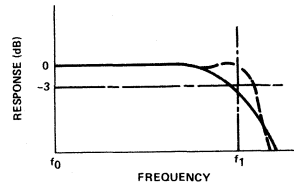
Derivation of Shunt Peaking Formula

The equivalent circuit of the drain load is shown in the Fig-ure below. The total impedance seen by the drain is given by:

$$Z = \left[ \frac{R_L^2 + \omega^2 L^2}{(1 - \omega^2 LC)^2 + \omega^2 C^2 R_L^2} \right]^{1/2} \quad (5)$$



The response below shows the "normal" 3-dB frequency without peaking - f<sub>1</sub>. It is now required to raise the response at f<sub>1</sub> by 3 dB to achieve a maximally flat response. Therefore, under these conditions the total impedance seen by the drain at f<sub>1</sub> must equal the impedance seen by the drain at f<sub>0</sub>. Also at f<sub>1</sub>, X<sub>C</sub> = R<sub>L</sub>. Substituting for X<sub>C</sub> in Equation 5:



$$R_L^2 = \frac{R_L^2 + \omega^2 L^2}{\left(1 - \frac{\omega L}{R_L} + 1\right)} \quad (6)$$

$$R_L^2 - 2\omega L R_L + \omega^2 L^2 + R_L^2 = R_L^2 + \omega^2 L^2 \quad (7)$$

$$R_L^2 = 2\omega L R_L \quad (8)$$

$$R_L = 2\omega L \quad (9)$$

$$L = \frac{R_L}{4\pi f_1} \quad (10)$$

and

$$f_1 = \frac{1}{2\pi R_L C} \therefore L = \frac{R_L^2 C}{2} \quad (11)$$

REFERENCES

1. Sherwin, J.S., "Liberate Your FET Amplifier," Electronic Design, May 1970.
2. Siliconix Application Tip, "FET Cascode Circuits Reduce Feedback Capacitance," August 1970.

# APPLICATION NOTE

## FETs in Balanced Mixers

Ed Oxner

### INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

#### Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

#### Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than

Table I

| Characteristic      | MIXER TYPE               |                 |                 |
|---------------------|--------------------------|-----------------|-----------------|
|                     | Single-Ended             | Single Balanced | Double Balanced |
| Bandwidth           | Several decades possible | Decade          | Decade          |
| Relative IM Density | 1.0                      | 0.5             | 0.25            |
| Interport Isolation | Little                   | 10-20 dB        | >30 dB          |
| Relative L.O. Power | 0 dB                     | +3 dB           | +6 dB           |

Table II

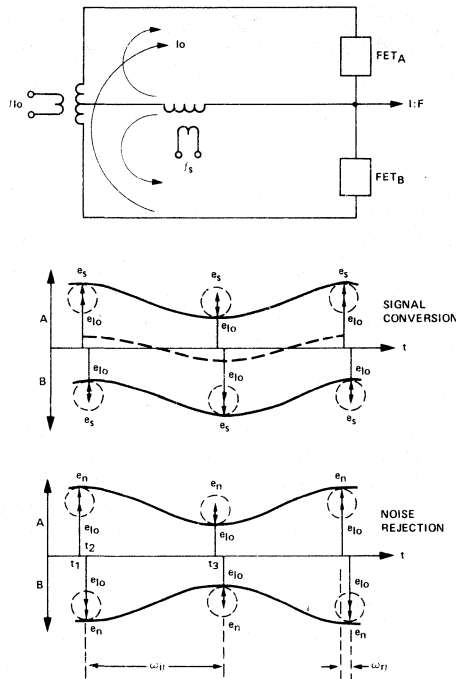
| DEVICE             | ADVANTAGES   | DISADVANTAGES  |
|--------------------|--|--|
| Bipolar Transistor | Low Noise Figure<br>High Gain<br>Low D.C. Power  | High IM<br>Easy Overload<br>Subject to Burnout   |
| Diode              | Low Noise Figure<br>High Power Handling<br>High Burn-out Level   | High L.O. Drive<br>Interface to I.F.<br>Conversion Loss                                      |
| JFET               | Low Noise Figure<br>Conversion Gain<br>Excellent IM products<br>Square Law Characteristic<br>Excellent Overload<br>High Burn-out Level | Optimum Conversion Gain not possible at Optimum Square Law Response Level<br>High L.O. Power |
| Dual-Gate MOS FET  | Low IM Distortion<br>AGC<br>Square Law Characteristic  | High Noise Figure<br>Poor Burnout Level<br>Unstable  |

those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

### First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).



Signal and Noise Vectors

Figure 1

Energy conversion into the intermediate frequency (IF) passband is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate ( $\omega_{ift}$ ); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time ( $t_1$ ) the noise component ( $e_n$ ) is "in phase" with the local oscillator vector ( $e_{10}$ ) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time  $t_2$ , the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving

ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced  $180^\circ$  ( $\omega_{ift}$ ) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise.<sup>(1)</sup>

The analysis of the conversion of the signal to the IF passband is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time  $t_2$ , the signal vector ( $e_s$ ) is "out of phase" with the local oscillator vector,  $e_{10}$ . The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a *prototype* balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

- (1) Intermodulation and Cross-Modulation
- (2) Conversion Gain
- (3) Noise Figure
- (4) Selecting the Proper FET
- (5) Local Oscillator Injection
- (6) Designing the Input Transformer
- (7) Designing the IF Network

### Intermodulation and Cross-Modulation

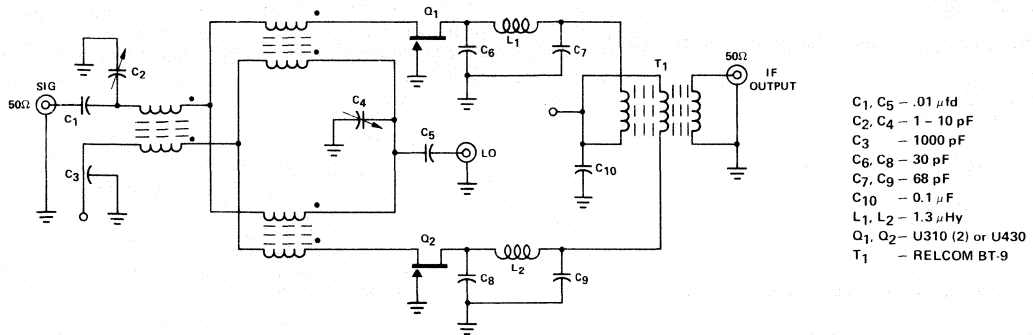
A basic aim in mixer design is to avoid the effects of intermodulation product distortion and crossmodulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both crossmodulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest.<sup>(2)</sup>

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an N-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance,  $g_c$ , is achieved at about 80% of the FET gate cutoff voltage,  $V_{GS(off)}$ , and amounts to about 25% of the forward transconductance,  $g_{fs}$ , of the FET when used as an amplifier.





**Prototype Active Balanced Mixer**  
Figure 2

- C<sub>1</sub>, C<sub>5</sub> - .01 μfd
- C<sub>2</sub>, C<sub>4</sub> - 1 - 10 pF
- C<sub>3</sub> - 1000 pF
- C<sub>6</sub>, C<sub>8</sub> - 30 pF
- C<sub>7</sub>, C<sub>9</sub> - 68 pF
- C<sub>10</sub> - 0.1 μF
- L<sub>1</sub>, L<sub>2</sub> - 1.3 μHy
- Q<sub>1</sub>, Q<sub>2</sub> - U310 (2) or U430
- T<sub>1</sub> - RELCOM BT-9

Since conversion gain (or loss) must be considered, it is common to equate voltage gain  $A_V$ , as:

$$A_V = g_c R_L \tag{1}$$

where  $g_c$  is the conversion transconductance and  $R_L$  is the FET drain load.

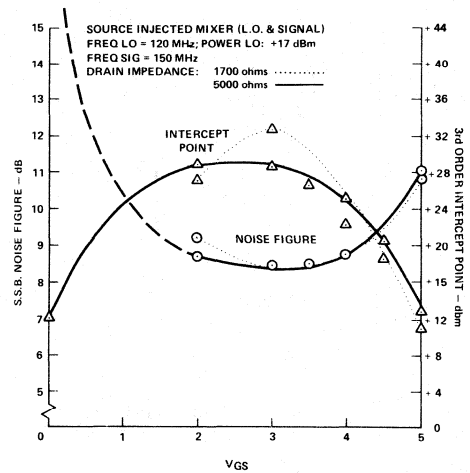
An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion - particularly intermodulation product distortion.

Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

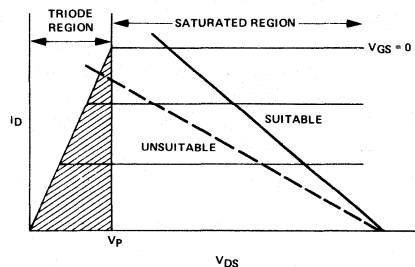
The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted crossmodulation signals.<sup>(3)</sup> A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 18 through 20.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-source voltage can cause a change in parasitic capacitance,  $C_{RSS}$ , and give rise to harmonics.<sup>(4)</sup> A FET tends to be voltage-dependent when the drain voltage falls appreciably below 6 volts. If the source voltage (from the power supply) is also low and the drain

load impedance is high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.



**Comparison of Mixer IM Characteristics**  
Figure 3



**Plotting Drain Load Lines**  
Figure 4

**Conversion Gain**

In a FET, forward transconductance is defined as(5)

$$g_{fs} = \frac{dI_D}{dV_{gs}} \quad (2)$$

and conversion transconductance is defined as(6)

$$g_c = \frac{dI_D(\omega_i)}{dV_{gs}(\omega_r)} \quad (3)$$

where  $\omega_i$  = the intermediate frequency and  $\omega_r$  = the signal frequency.

The effects of time-varying local oscillator voltage,  $V_2$ , and the much smaller signal voltage,  $V_1$ , must be considered:

$$v_{gs} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \quad (4)$$

For square law operation(7)

$$V_2 + V_{GS} \leq V_{GS(off)} \quad (5)$$

Drain current is approximately defined by (8)

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2 \quad (6)$$

or (9)

$$I_D \approx \frac{g_{fso} V_{GS(off)}}{2} \left[ 1 - \frac{v_{gs}}{V_{GS(off)}} \right]^2 \quad (7)$$

or

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \left[ V_{GS(off)} - v_{gs} \right]^2 \quad (8)$$

then (10)

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \text{ (complex Taylor expansion)} \quad (9)$$

which can be reduced to

$$I_D(IF) \approx \frac{g_{fso}}{2V_{GS(off)}} V_1 V_2 \cos(\omega_1 - \omega_2)t \quad (10)$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2V_{GS(off)}} |V_2| \quad (11)$$

Equation 11 suggests that  $g_c$  increases without limit as  $V_2$  increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of  $V_2$  should not exceed  $V_{GS(off)}$ .

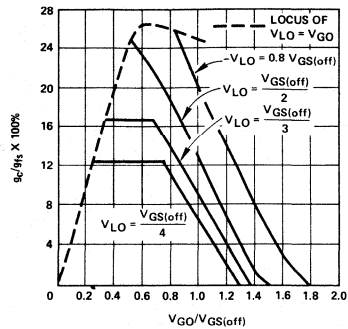
Thus

$$2 V_2 \text{ peak} \leq V_{GS(off)} \quad (12)$$

or

$$V_2 \text{ peak} \leq \frac{V_{GS(off)}}{2} \quad (13)$$

Figure 5 shows plots of normalized conversion transconductance,  $g_c/g_{fs}$  versus normalized quiescent bias,  $V_{GS}/V_{GS(off)}$ , for different oscillator injections.



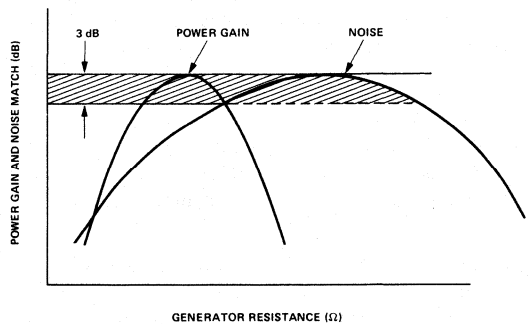
**Normalized  $g_c/g_{fs}$  vs.  $V_{GS}/V_{GS(off)}$**   
 (from "FET RF Mixer Design Technique", S.P. Kwok,  
 WESCON Convention Record (1970) 8/1, p.2.)

**Figure 5**

**Noise Figure**

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance,  $R_g$ .<sup>(11)</sup> A change of a decade in  $R_g$  can produce a noise figure variation of as much as 3 dB.

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance,  $g_{igs}$ , which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.



**Power Gain and Noise Matching**  
**Figure 6**

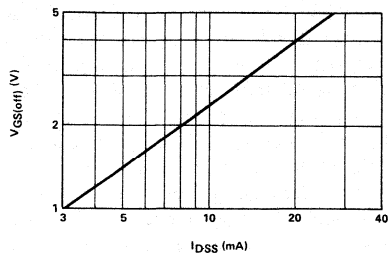
### How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance,  $g_c$ , which in turn is directly related to such FET parameters are zero-bias saturation current,  $I_{DSS}$ , and the gate cutoff voltage,  $V_{GS(off)}$ :

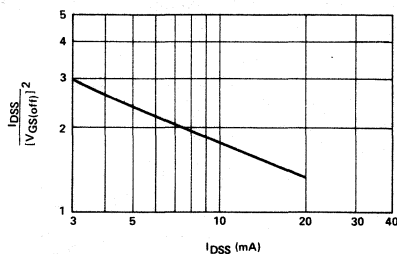
$$g_c = \frac{I_{DSS}}{V_{GS(off)}^2} |V_2| \quad (14)$$

$$\approx \frac{g_{fso}}{2V_{GS(off)}} \quad (15)$$

Equation 15 appears to indicate that FETs with high  $I_{DSS}$  are to be preferred. However,  $I_{DSS}$  and  $V_{GS(off)}$  are related, and Figures 7A and 7B show that devices from a family selected for high  $I_{DSS}$  do not provide high conversion transconductance, but actually produce a lower value of  $g_c$ .



a.



b.

Relationship of  $I_{DSS}$  and  $V_{GS(off)}$

Figure 7

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage,  $V_{GS(off)}$ , for good conversion transconductance, and zero-bias saturation current,  $I_{DSS}$ , for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 20,000  $\mu\text{mhos}$  max at  $V_{DS} = 10 \text{ V}$ ,  $I_D = 10 \text{ mA}$ , and  $f = 1 \text{ kHz}$ .

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach — the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember,

however, that conversion transconductance,  $g_c$ , can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a number of possible alternatives to the U310.

Table III

| Typical Characteristic | DEVICE TYPE |        |         |        |
|------------------------|-------------|--------|---------|--------|
|                        | U310*       | 2N5912 | 2N4416* | 2N3823 |
| $g_m$                  | 14K         | 6K     | 5K      | 3.5K   |
| $I_{DSS}$              | 40 mA       | 15 mA  | 10 mA   | 10 mA  |

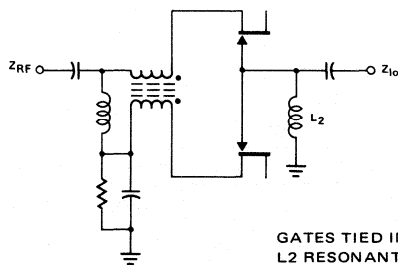
\*Similar devices are also available in plastic packages:

- U310 (J310)
- 2N5397 (K300-18)
- 2N4416 (2N5486, K304-18)

### Local Oscillator Injection

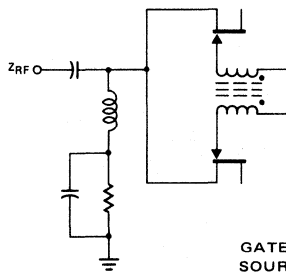
Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5.  $V_{LO}$  is expressed in terms of peak-to-peak voltage, while  $V_{GS(off)}$  is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing. Two circuits to obtain direct gate coupling are suggested in Figure 8.



GATES TIED IN PARALLEL  
L2 RESONANCES WITH  $C_g$

a.



GATES DRIVEN PUSH-PULL  
SOURCES TIED TOGETHER

b.

Alternate Forms of L.O. Injection

Figure 8

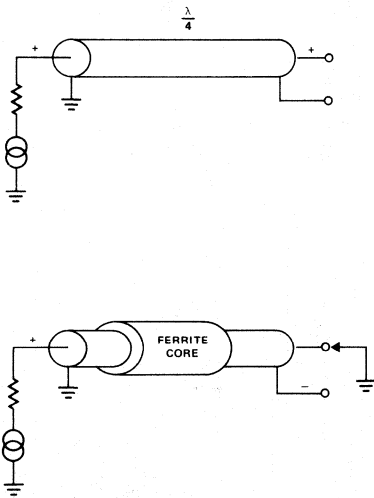
The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer, best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-ohm load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

**Designing the Input Transformer**

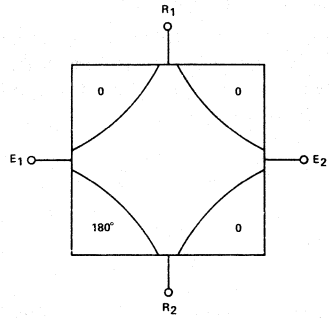
Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

- (1) Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B
- (2) Offer a match between either input to a symmetrical balanced load
- (3) Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)
- (4) Maintain a differential phase of 180° across the symmetrical balanced loads
- (5) Introduce the least possible amount of loss



**Hybrid Input Coupling Transformer**

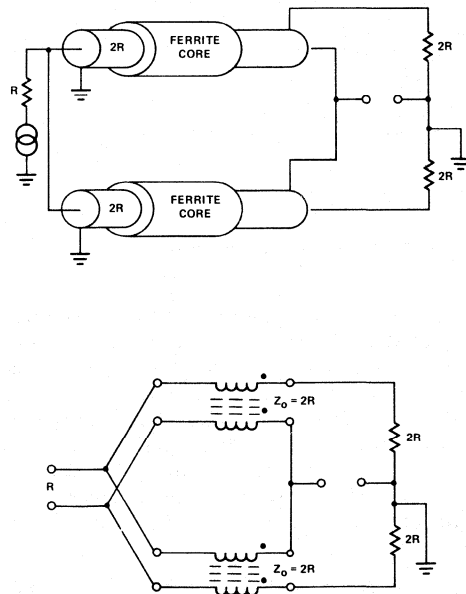
**Figure 10**



**4-Port Hybrid with Phase and Isolation**

**Figure 9**

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite.<sup>(12)</sup> The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff.<sup>(13)</sup>



Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis.<sup>(14)</sup> The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{\text{upper}}} \quad (\text{inches}) \quad (16)$$

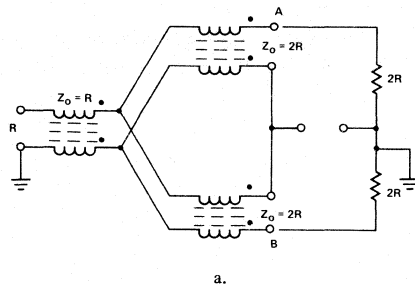
$$\text{min length} = \frac{20 R_L}{(1 + \mu/\mu_0) f_{\text{lower}}} \quad (\text{inches}) \quad (17)$$

where  $R_L$  = the load impedance,  $\mu/\mu_0$  = the relative permeability of the ferrite at the lower frequency, and  $n$  = a fractional wavelength determined by the amount of allowable phase error.

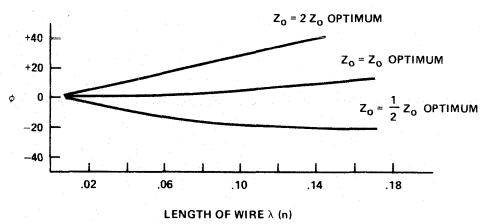
Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high  $Q$ .

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium.<sup>(15)</sup> A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line conductors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance,  $Z_0$ , is to be preferred over a higher  $Z_0$ . Both 50-ohm and 100-ohm transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45  $\Omega$  is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide  $Z_0 = 100$  ohms. Each core is wound with 2 inches of the proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 16, 17).

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated ( $C_2, C_4$ , Figure 2).<sup>(16)</sup> A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within  $\pm 2$  degrees (about  $180^\circ$ ) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.



a.



b.

Toroid Coil Winding Data  
Figure 11

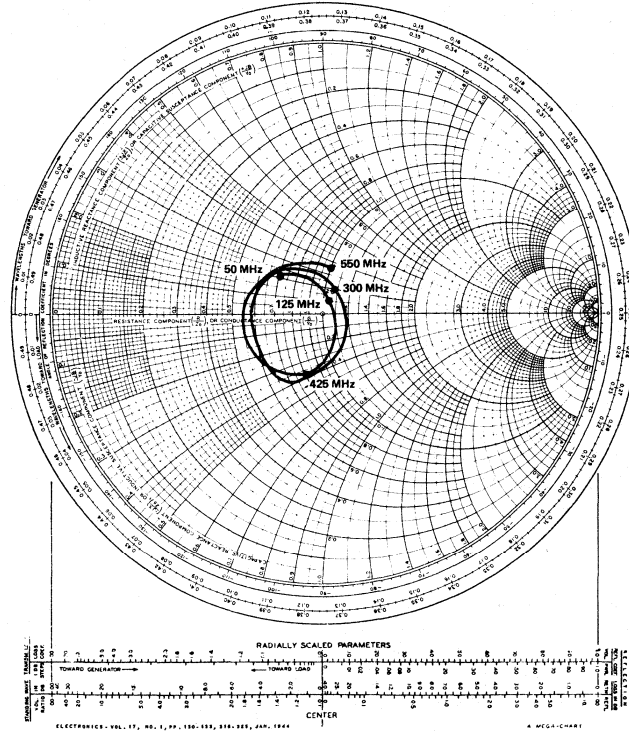
### Designing the IF Network

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi ( $\pi$ ) match structure from each FET drain to a common balanced output transformer network.<sup>(17)</sup> This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency,  $f_0$ .<sup>(18, 19)</sup> This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and crossmodulation will be



50Ω – 200Ω Balun  
Figure 12

both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors. (20) If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2 V_{GS(off)}}{i_d} \quad (18)$$

where

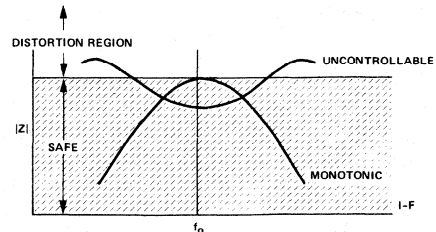
$$i_d = I_{DSS} \left[ 1 - \frac{v_{gs}}{V_{GS(off)}} \right]^2 \quad (19)$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \quad (20)$$

For the U310 FET, the optimum drain load impedance is established at slightly less than 2000 ohms, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-ohm CT to 50-ohm trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 ohms on each FET; excellent



Pi (π) Match Filter Function  
Figure 13

IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

### Mixer Performance

Tests of the operational prototype FET balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table IV (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point.<sup>(21)</sup> With two signals 300 kHz apart, the balanced mixer suppressed third-order products -89 dB with both signals at -10 dBm, representing an intercept point of +32 dBm.

Table IV

50-250 MHz Mixer Performance Comparison

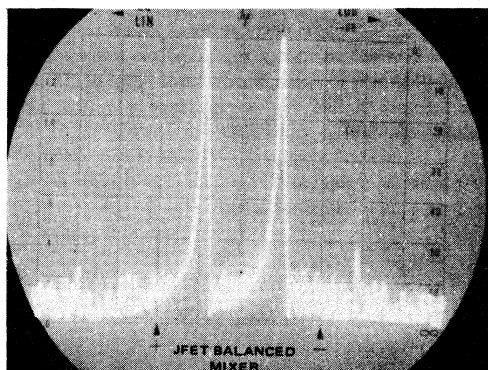
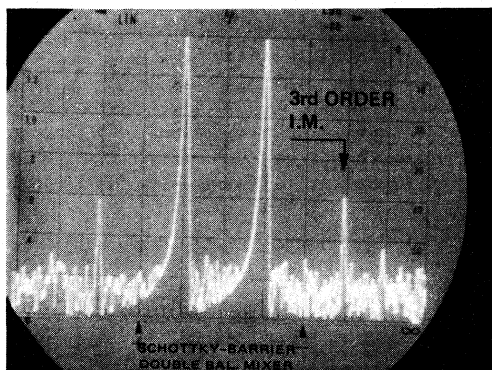
| Characteristic  | JFET     | Schottky | Bipolar  |
|---|----------|----------|----------|
| Intermodulation Intercept Point   | +32 dBm  | +28 dBm  | +12 dBm† |
| Dynamic Range   | 100 dB   | 100 dB   | 80 dB†   |
| Desensitization Level<br>(the level for an unwanted signal when the desired signal first experiences compression) | +8.5 dBm | +3 dBm   | +1 dBm†  |
| Conversion Gain   | +2.5 dB* | -6 dB    | +18 dB   |
| Single-sideband Noise Figure @ 50 MHz   | 7.2 dB   | 6.5 dB   | 6.0 dB   |

†Estimated

\*Conservative minimum

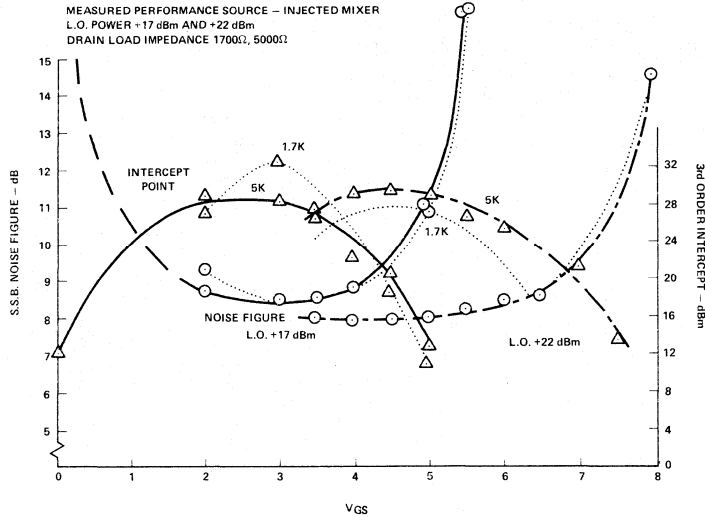
Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.



Comparison of 3rd Order IM Products

Figure 14



Noise Figure and Intercept Point Performance

Figure 15

## CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 16 and 17) are equally applicable to trifilar as they are for bifilar.

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- (11) Op. cit., "High-Frequency JFET Characterization."
- (12) O. Pitzalis and T. Couse, "Broadband Transformer Design for RF Transistor Power Amplifiers," ECOM-2989, July 1968. Also in Proc. Electronic Component Conference (1968).
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- (19) Op. cit., "The Solid State Receiver."
- (20) "Distortion in FET Amplifiers," J. Sherwin, ELECTRONICS, Dec. 12, 1966.
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# APPLICATION NOTE

## FETs As Voltage-Controlled Resistors

### INTRODUCTION

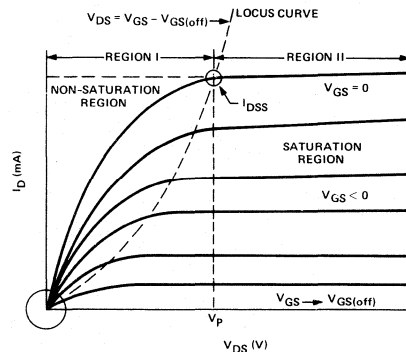
#### The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage,  $V_{GS}$ , and the net drain-source voltage,  $V_{DS}$ .

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.<sup>(1)</sup> Maximum drain-source current,  $I_{DSS}$ , and minimum resistance,  $r_{DS(on)}$ , will exist when the gate-source voltage is equal to zero volts ( $V_{GS} = 0$ ). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by  $V_{GS} = V_{GS(off)}$ . Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.<sup>(2)</sup> The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.

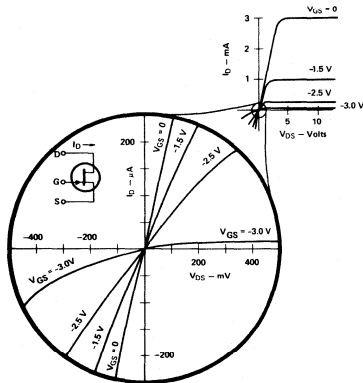


Typical N-Channel JFET Operating Characteristics  
Figure 1

**Resistance Properties of FETs**

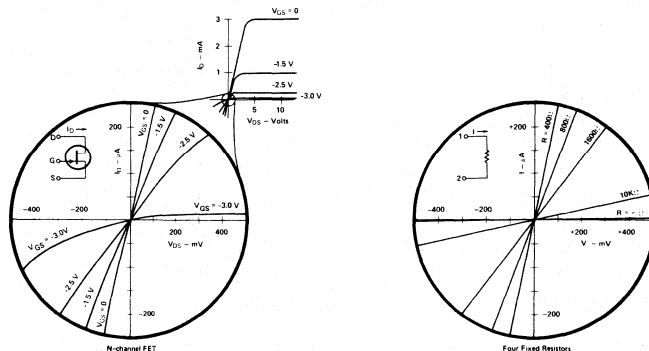
The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance,  $r_{ds}$ , is essentially the same as that of d.c. resistance,  $r_{DS}$ , and is a function of  $V_{GS}$ .<sup>(3)</sup>

Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of  $V_{DS}$  are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the  $V_{GS}$  bias line is equal to  $\Delta I_D / \Delta V_{DS} = 1/r_{DS}$ . This value is controlled by the amount of voltage applied to the gate. Minimum  $r_{DS}$ , usually expressed as  $r_{DS(on)}$ , occurs at  $V_{GS} = 0$  and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high  $r_{DS(on)}$  and a low  $I_{DSS}$ . Thus a FET with high  $I_{DSS}$  should be chosen where design requirements indicate the need for a low  $r_{DS(on)}$ .



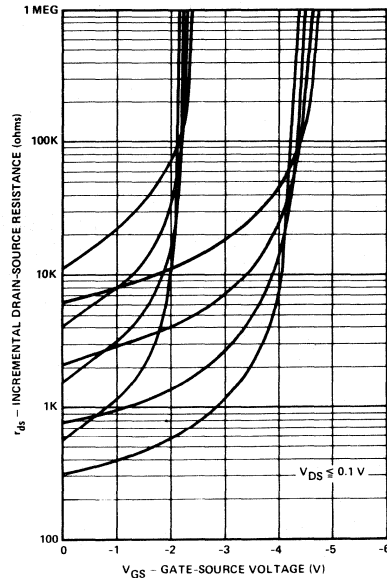
**N-Channel JFET Output Characteristic Enlarged Around  $V_{DS} = 0$**   
Figure 2

Figure 3 extends the  $r_{ds}$  characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.



**Comparison of FET and Resistor Characteristics**  
Figure 3

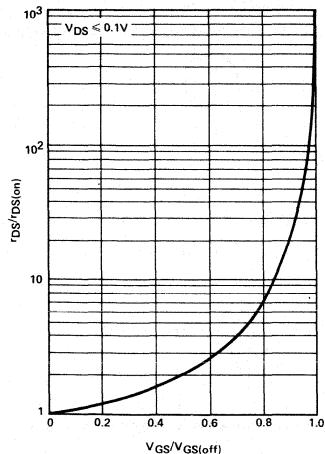
Typical  $r_{DS}$  curves for several Siliconix N-channel JFETs are plotted in Figure 4.<sup>(4)</sup> The graphs are useful in estimating  $r_{DS}$  values at any given value of  $V_{GS}$ . All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefore desirable to convert Figure 4 to a normalized plot. This



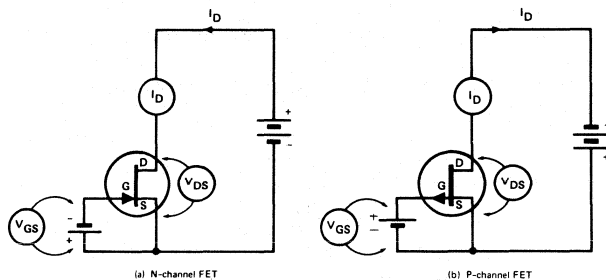
**Incremental Drain-Source Resistance for Typical N-Channel JFETs**  
Figure 4

has been done in Figure 5. The resistance is normalized to its specific value at  $V_{GS} = 0$  V. The dynamic range of  $r_{DS}$  is shown as greater than 100:1, although for best control of  $r_{DS}$  a range of 10:1 is normally used.

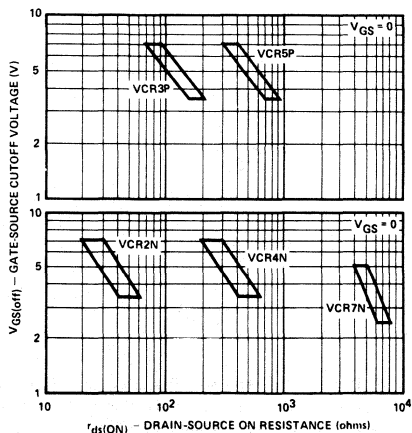
Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have  $r_{DS(on)}$  values ranging from 20  $\Omega$  to 4,000  $\Omega$  (Figure 7).



Normalized  $r_{DS}$  Data  
Figure 5



Circuit Arrangement for Both an N and P Channel FET  
Figure 6



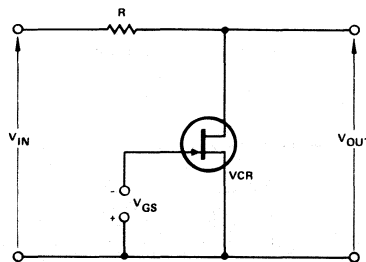
$r_{DS(ON)}$  (Drain-Source Resistance at  $V_{DS} = V_{GS} = 0$ )  
Varies as an Inverse Function of  $V_{GS(off)}$

Figure 7

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.<sup>(5)</sup>



Simple Attenuator Circuit  
Figure 8

The output voltage is

$$V_{OUT} = \frac{V_{in} r_{DS}}{R + r_{DS}} \tag{1}$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the  $r_{DS}$  is not shunted by the load.

The lowest value which  $V_{OUT}$  can assume is

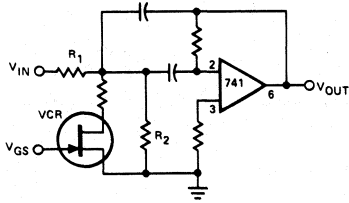
$$V_{OUT(min)} = \frac{V_{in} r_{DS(on)}}{R + r_{DS(on)}} \tag{2}$$

The highest value is

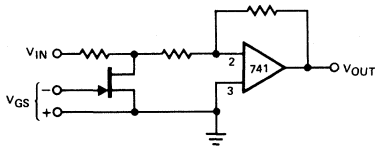
$$V_{OUT(max)} = V_{in} \quad (3)$$

since  $r_{DS}$  can be extremely large.

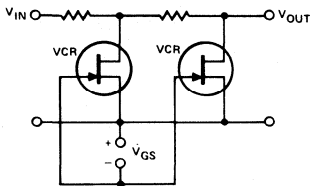
A number of other FET VCR applications are shown in Figures 9-16.



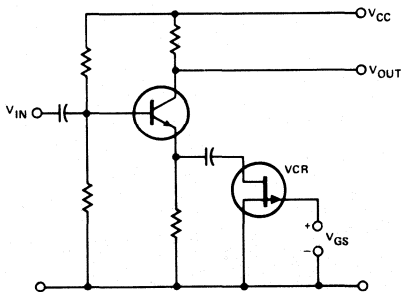
**Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET  $V_{GS(off)}$  and Tuned by  $R_2$ . Upper Frequency is Controlled by  $R_1$**   
Figure 9



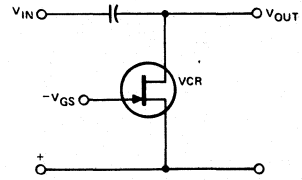
**Electronic Gain Control**  
Figure 10



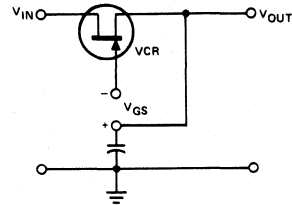
**Cascaded VCR Attenuator**  
Figure 11



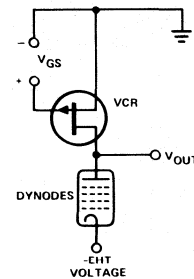
**Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level**  
Figure 12



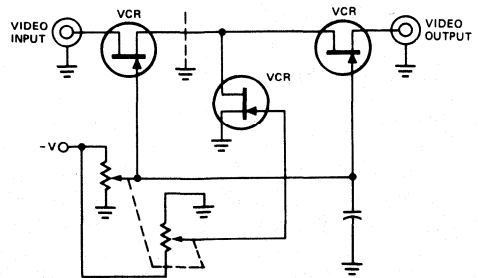
**VCR Phase Advance Circuit**  
Figure 13



**VCR Phase Retard Circuit**  
Figure 14



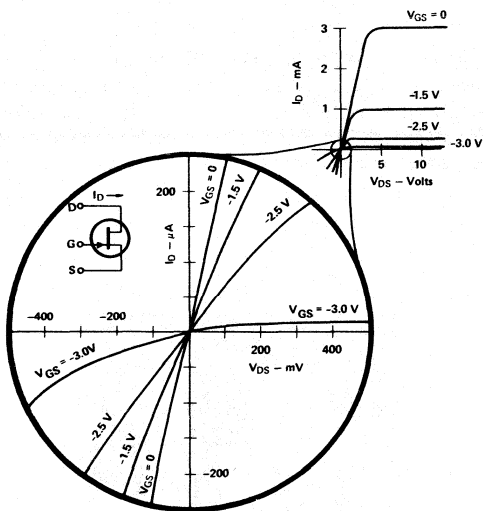
**P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually  $< 1 \mu A$ ) Implies that VCR will Always Perform in Linear Region Near Origin**  
Figure 15



**Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides for Optimum Dynamic Linear Range Attenuation**  
Figure 16

**Signal Distortion: Causes**

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as  $V_{DS}$  increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in  $r_{DS}$ , and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as  $V_{DS}$  reduces the drain current, so that a pinch-off condition is reached when  $V_{DS} = V_{GS} - V_{GS(off)}$ . Figure 17B shows how the current has an opposite effect



**N-Channel JFET Output Characteristic Enlarged Around  $V_{DS} = 0$**   
Figure 17A

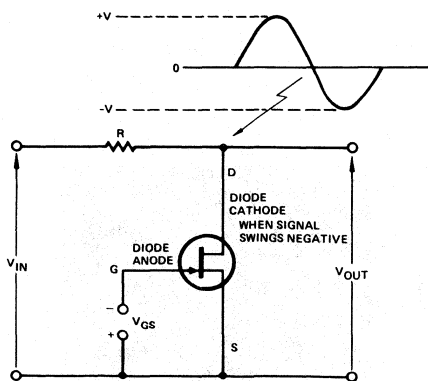


Figure 17B

in the third quadrant, rising negatively with an increasingly negative  $V_{DS}$ . This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.

**Reducing Signal Distortion**

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

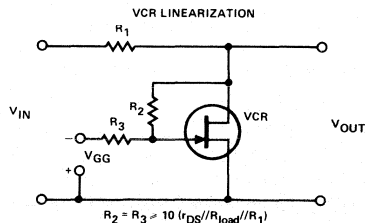


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the  $V_{GS}$  bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the  $V_{DS} = V_{GS} - V_{GS(off)}$  locus is approached. Resistors  $R_2$  and  $R_3$  in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geq 10 [R_1 \parallel r_{ds}(\max) \parallel R_L] \tag{4}$$

Typically, 470K  $\Omega$  resistors will work well for most applications.  $R_1$  is selected so that the ratio of  $r_{DS(on)} \parallel R_L$  to  $[(r_{DS(on)} \parallel R_L) + R_1]$  gives the desired output voltage, or:

$$e_o = e_i \frac{r_{DS(on)} \parallel R_L}{(r_{DS(on)} \parallel R_L) + R_1} \tag{5}$$

The feedback technique used in Figure 18 requires that the gate control voltage,  $V_{GG}$ , be twice as large as  $V_{GS}$  in Figure 17B for the same  $r_{DS}$  value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

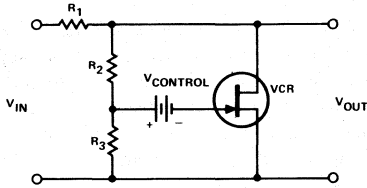


Figure 19

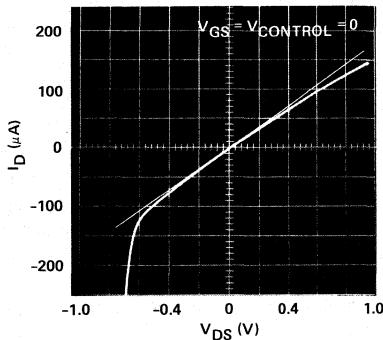
**Experimental Results**

Figures 20 through 23 show low voltage output characteristic curves for a typical Siliconix N-Channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 20 shows a two-volt peak-to-peak signal on the  $V_{GS} = 0$  V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.

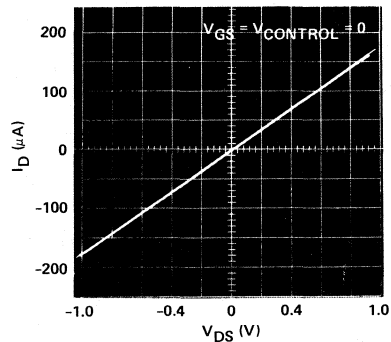
The forward-biased gate-drain PN junction may be seen at approximately  $-0.6$  V, and bending of the bias curve is apparent in the third quadrant. The photo also demonstrates the comparison between a fixed resistor (the linear line superimposed on the bias curve) and the distortion apparent in the VCR without feedback compensation; the VCR signal is unusable with the indicated amount of distortion.

In Figure 21, the same VCR7N FET is shown operating with the addition of the feedback resistors. Distortion has been reduced to less than 0.5%, and the characteristics of the VCR are now closely comparable to those of a fixed resistor.

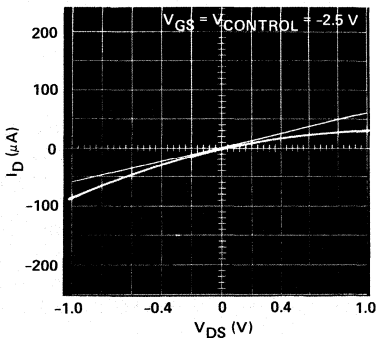
In Figures 22 and 23, the same VCR FET characteristics are shown, with  $V_{GS}$  adjusted for higher  $r_{DS}$ . No feedback network is employed in Figure 22, and measured distortion is greater than 8%. In Figure 23, the feedback resistors have been added and distortion has been reduced to less than 0.5%.



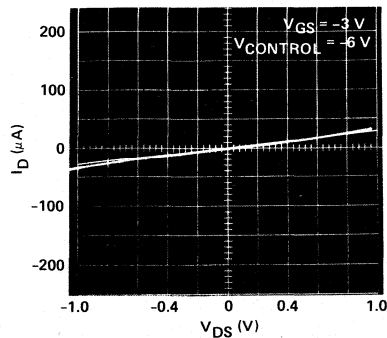
VCR7N with No Feedback  
Figure 20



VCR7N with Feedback  
Figure 21

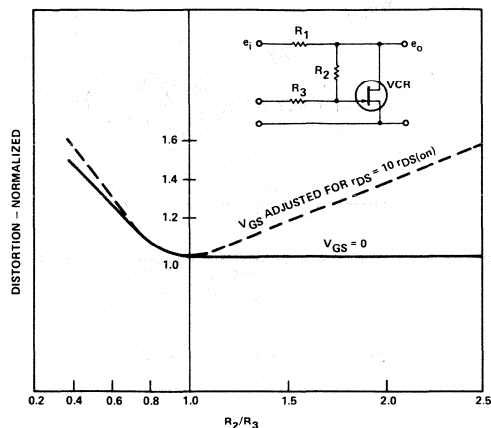


VCR7N with No Feedback  
Figure 22



VCR7N with Feedback  
Figure 23

Some degree of non-linearity will be experienced in both the first and third quadrants as  $V_{GS}$  approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants. Figure 24 shows a curve of distortion vs  $R_2/R_3$ , in both quadrants.



Distortion vs  $R_2/R_3$   
Figure 24

Distortion resulting from changes in temperature are also minimized by the feedback resistor technique.  $r_{DS}$  will change with temperature in an inverse manner to the behavior of FET drain current. Table I presents the result of VCR laboratory performance tests of distortion vs temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

Table I

| Temperature<br>(°C) | Without Feedback      |                          | With Feedback         |                          |
|---------------------|-----------------------|--------------------------|-----------------------|--------------------------|
|                     | $r_{DS} = r_{DS(on)}$ | $r_{DS} = 10 r_{DS(on)}$ | $r_{DS} = r_{DS(on)}$ | $r_{DS} = 10 r_{DS(on)}$ |
| +125                | >13%                  | >6%                      | <0.5%                 | <0.5%                    |
| + 25                | >10%                  | >5%                      | <0.5%                 | <0.5%                    |
| - 55                | 3.9%                  | 3.2%                     | <0.5%                 | <0.5%                    |

## SUMMARY

This Application Note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no DC bias voltage in the signal loop, an ideal characteristic for many applications.

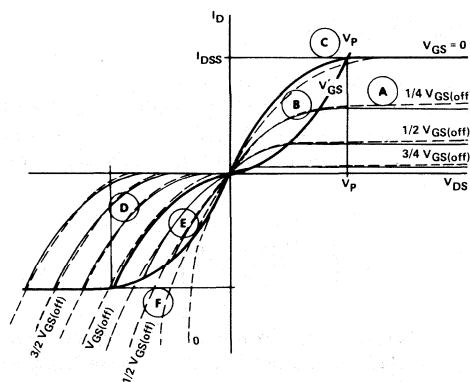
Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high  $V_{GS(off)}$  will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high  $V_{GS(off)}$  (compatible with the desired  $r_{DS}$  value) if large signal levels are to be encountered.

APPENDIX A — From proceedings of the IEEE, October, 1968, pp. 1718-1719.

Abstract — An analytical approximation of FET characteristics for positive and negative voltages is presented. The distortion in an application as a controlled attenuator is calculated, and a method of reducing distortion by a factor of more than 50 is described.

Controlled resistors are used in oscillators, controlled amplifiers, and attenuators.<sup>(6,7)</sup> The possible control range is much larger for field-effect transistors (FET) than for other elements with comparable time constants (e.g., diodes). The signal-to-noise ratio is considerably improved.



Comparison Between Mathematical Approximation of FET Characteristics (Solid Lines) and Measured Curves (Broken Lines) for a Typical N-Channel JFET  
Figure 25

Figure 25 shows idealized and real FET characteristics. In region A (above pinch-off)  $I_D$  is independent of  $V_{DS}$ .<sup>(8)</sup>

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (1)$$

Region B, where  $V_{DS} < (V_{GS} - V_P)$ , is the so-called triode region. (In the following discussion all the signs (+, -) will be valid for N-Channel FETs.) The characteristics can be

approximated by a quadratic function, of which the maximum and a second point (the origin) are known. The approximation is

$$I_D = I_{DSS} \left[ \left(1 - \frac{V_{GS}}{V_P}\right)^2 - \left(1 - \frac{V_{GS} - V_{DS}}{V_P}\right)^2 \right] \\ = \frac{2I_{DSS}}{(V_P)^2} V_{DS} \left( V_{GS} - V_P - \frac{V_{DS}}{2} \right) \quad (2)$$

This is the same function that can be found by a simple analysis based on semiconductor theory. The less negative of the two voltages across the junction ( $V_{GS}$ ,  $V_{GD}$ ) controls the channel conductance. Under the condition that the FET is symmetrical (drain and source interchangeable), the following consideration is true. If  $V_{GD}$  were the controlling voltage and  $V_{DS} < 0$ ,  $I_D < 0$ , then the characteristics would be the same as in the first quadrant:

$$-I_D = -\frac{2I_{DSS}}{V_P^2} V_{DS} \left( V_{GD} - V_P + \frac{V_{DS}}{2} \right) \quad (3)$$

Since the controlling voltage for both regions (B and E) is  $V_{GS}$ ,

$$V_{GD} = V_{GS} - V_{DS} \quad (4)$$

Substituting (4) into (3), we get (2); the same approximation can be used in B and E. The limits of region E where (2) is valid are  $V_{GD} = 0$  and  $V_{GD} = V_P$ . The characteristics in region D can be found from (1) with the same consideration:

$$I_D = -I_{DSS} \left(1 - \frac{V_{GS} - V_{DS}}{V_P}\right)^2 \quad (5)$$

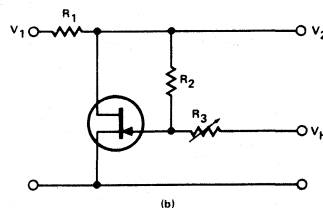
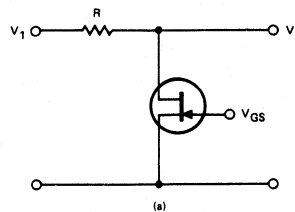
The mathematical approximation is compared with the measured characteristic in Figure 25. In the regions C and F the junction is forward biased. The characteristics are dependent on the internal resistance of the gate voltage source since gate current flows.

The FET as a controlled resistor works in region B and E. The higher the resistance, the more non-linear are the characteristics. For most applications this is undesirable. Based on the simple approximation (2), the relation between distortion, control range, and maximum to minimum attenuation will be described for a simple voltage divider [Figure 26(a)]. Most applications can be based on this simple example. The conductance in any point of region B or E is

$$G_{DS} = \frac{I_D}{V_{DS}} = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right) \\ - \frac{I_{DSS}}{(V_P)^2} V_{DS} = g_{DS} + \frac{g_{DSS} V_{DS}}{2V_P} \quad (6)$$

where  $g_{DS}$  is the differential conductance at the origin; when  $V_{GS} = 0$ , then  $g_{DS} = g_{DSS}$ . The attenuation for the circuit of Figure 26(a) is

$$\frac{V_2}{V_1} = \frac{1}{1 + Rg_{DS}} \\ = \left[ 1 + Rg_{DS} + \frac{Rg_{DSS} V_1}{2V_P \left(1 + Rg_{DS} + \frac{2Rg_{DSS} V_1}{2V_P (1 + Rg_{DS})}\right)} \right]^{-1} \quad (7)$$



(a) Controlled JFET Attenuator. (b) Controlled Attenuator with "Feedback" Making Characteristics Linear and Symmetrical  
Figure 26

To reduce (7) to a more tractable form, the following inequality is introduced:

$$\frac{V_1 Rg_{DSS}}{2V_P [1 + Rg_{DS}]^2} \ll 1$$

so that (7) can now be approximated by the expansion

$$V_2 = \frac{V_1}{1 + g_{DS}R} \left( 1 - \frac{Rg_{DS} V_1}{2V_P [1 + Rg_{DS}]^2} + \dots \right) \quad (8)$$

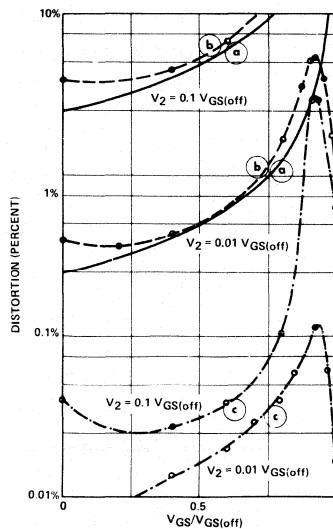
Only the second harmonic will be considered for the distortion since the third is much smaller. For small distortion ( $d \ll 1$  and  $Rg_{DSS} \gg 1$ ),

$$d = \frac{V_1 Rg_{DSS}}{4|V_P| [1 + Rg_{DS}]^2} \quad (9)$$

If  $V_2$  is held constant,

$$d = \frac{V_2 Rg_{DS}}{4|V_P| [1 + Rg_{DS}]} \approx \frac{V_2}{4|V_P - V_{GS}|} \quad (10)$$





**Distortion as a Function of  $V_{GS}/V_{GS(off)}$  for Two Different  $V_2/V_{GS(off)}$ .** (a) Theoretical for Figure 26(a). (b) Measured with Circuit of Figure 26(a). (c) Measured with Circuit of Figure 26(b)  
Figure 27

Figure 27 shows a comparison of measured and calculated distortion. If  $V_{GS}$  approaches  $V_P$ , the above restrictions are violated; the expression for the distortion can no longer be applied. If  $V_{DS} < 0$ ,  $V_{GS} = 0$ , then the FET works in region F; the distortion will be higher than predicted. From (10) we get for a prescribed maximum distortion a maximum amplitude as a function of  $V_{GS}$ :

$$V_{2max} = 4d_{max} |V_P - V_{GS}| \quad (11)$$

For a given  $d_{max}$  and  $V_{2max}$  the ratio of minimum to maximum attenuation is

$$\frac{A_{min}}{A_{max}} = m = \frac{1 + R_{gDSS}}{1 + R_{gDSS} \frac{V_{2max}}{4d_{max} |V_P|}} \approx \frac{4d_{max} |V_P|}{V_{2max}} \quad (12)$$

valid only for  $m > 1$ . Note that the maximum distortion is reached only for minimum attenuation. Examples:

$$d_{max} = 10 \text{ percent } V_{2max} = 0.001 V_P \quad m = 400$$

$$d_{max} = 1 \text{ percent } V_{2max} = 0.01 V_P \quad m = 4$$

Although these relations are only first-order approximations, they give a good estimate of FET attenuator characteristics. The maximum amplitude is proportional to  $V_P$ . FETs with high  $V_P$  are desirable for attenuator applications. Unfortunately, the majority of commercially available FETs are made with low  $V_P$  for use in amplifiers.

There are several means of reducing distortion. By connecting two identical FETs in antiparallel or antiseriess, nonlinearities can be cancelled out to a certain extent. A better linearization is possible by using one FET with "feedback". It has been shown above that the characteristics would be symmetrical if  $V_{GD}$  were the control voltage in the third quadrant. By adding  $0.5 V_{DS}$  to the control voltage, the two voltage  $V_{GS}$  and  $V_{GD}$  interchange when  $V_{DS}$  changes sign:

$$\begin{aligned} V_{GS} &= V_H + 0.5 V_{DS} \\ V_{GD} &= V_H - 0.5 V_{DS} \end{aligned} \quad (13)$$

then (13) used in (2) gives

$$I_D = \frac{2I_{DSS}}{V^2_P} V_{DS} (V_H - V_P) \quad (14)$$

The resulting characteristic is linear and symmetrical in B and E. The improvement in distortion performance can be seen in Figure 27. A distortion of 12 percent for  $V_2 = 0.1 V_P$  at  $V_{GS} = 0.8 V_P$  is reduced through linearization to 0.1 percent. Figure 26(b) shows a possible circuit. The frequency range of the controlled signal must be much higher than that of the controlling signal  $V_H$  to keep the direct interference of  $V_H$  on  $V_2$  small.  $R_3$  is set for minimum distortion. If  $V_2$  and  $V_H$  are in the same frequency range, a high impedance amplifier must be used.  $V_2$  is at the input; the output is connected to the FET gate. The amplification is approximately 0.5 (adjustable). The control voltage is introduced through a second input so that no direct interference with  $V_2$  occurs.

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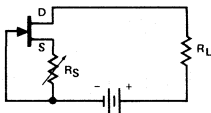


# DESIGN IDEA

## The FET Constant Current Source

### INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant current source. An adjustable current source may be built with a FET, a variable resistor and a small battery, Figure 1. For good thermal stability, the FET should be biased near the zero T.C. point.<sup>1</sup>



**Field-Effect Transistor Current Source**  
Figure 1

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage  $V_{DS}$  is significantly greater than the cut-off voltage  $V_{GS(off)}$ . The FET may be biased to operate as a constant current source at any current below its saturation current  $I_{DSS}$ .

For a given device where  $I_{DSS}$  and  $V_{GS(off)}$  are known, the approximate  $V_{GS}$  required for a given  $I_D$  is

$$V_{GS} = V_{GS(off)} \left[ 1 - \left( \frac{I_D}{I_{DSS}} \right)^{1/k} \right] \quad (1)$$

where  $k$  can vary from 1.7 to 2.0, depending upon device geometry. The series resistor  $R_S$  required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in supply voltage, or change in load impedance, will change  $I_D$  by only a small factor because of the low output conductance  $g_{oss}$ .

$$\Delta I_D = \Delta V_{DS} g_{oss} \quad (3)$$

The value of  $g_{oss}$  is an important consideration in the accuracy of a constant current source. As  $g_{oss}$  may range from less than  $1 \mu\text{mho}$  to more than  $50 \mu\text{mho}$  according to the FET type, the dynamic impedance can be greater than 1 megohm to less than 20K. This corresponds to a current stability range of  $1 \mu\text{A}$  to  $50 \mu\text{A}$  per volt. The value of  $g_{oss}$  depends also on the operating point, being highest at  $I_{DSS}$  and at low  $V_{DS}$ . Output conductance  $g_{oss}$  decreases approximately linearly with  $I_D$ , becoming less as the FET is biased toward cut-off. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \quad (4)$$

where

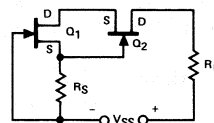
$$g_{oss} = g'_{oss} \quad (5)$$

when

$$V_{GS} = 0 \quad (6)$$

So as  $V_{GS} \gg V_{GS(off)}$ ,  $g_{oss} \gg \text{zero}$ . For best regulation,  $I_D$  must be considerably less than  $I_{DSS}$ .

It is possible to achieve much lower  $g_{oss}$  per unit  $I_D$  by cascading two FETs as shown in Figure 2.



**Cascade FET Current Source**  
Figure 2

Now,  $I_D$  is regulated by  $Q_1$  and  $V_{DS1} = -V_{GS2}$ . The d-c value of  $I_D$  is controlled by  $R_S$  and  $Q_1$ . However,  $Q_1$  and  $Q_2$  both affect current stability. The circuit output conductance is derived as follows:

Figure 2 is redrawn in Figure 3 for the condition  $V_{GS1} = 0$ .

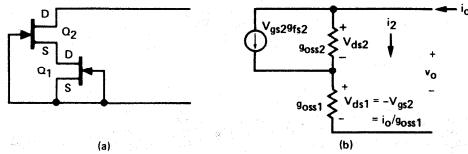


Figure 3

$$i_o = i_2 + v_{gs2}g_{fs2} = v_{ds2}g_{oss2} - i_o \frac{g_{fs2}}{g_{oss1}} \quad (7)$$

$$i_o = \frac{v_{ds2}g_{oss2}g_{oss1}}{g_{oss1} + g_{fs2}} \quad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \quad (9)$$

$$v_o = v_{ds2} \frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \quad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1}g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \quad (11)$$

If  $g_{oss1} = g_{oss2}$  (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs}/g_{oss}} \quad (13)$$

When

$R_S \neq 0$  as in Figure 2 (14)

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S(g_{fs}^2 + g_{oss}g_{fs} + g_{oss}^2)} \quad (15)$$

$$\approx \frac{g_{oss}^2}{g_{fs}(1 + R_Sg_{fs})} \quad (16)$$

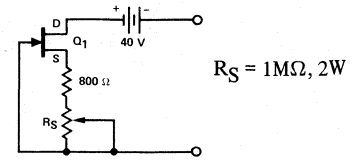
In either case ( $R_S = 0$  or  $R_S \neq 0$ ), the circuit output conductance is considerably less than the  $g_{oss}$  of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage  $V_{DG}$ . That is,

$$V_{DG} > V_{GS(off)}, \text{ preferably } V_{DG} > 2 V_{GS(off)} \quad (17)$$

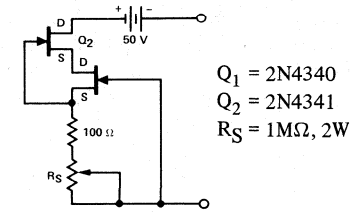
If  $V_{DG} < 2 V_{GS(off)}$ , the  $g_{oss}$  will be significantly increased, and circuit  $g_o$  will deteriorate. For example: A 2N4340 has typical  $g_{oss} = 4 \mu\text{mho}$  at  $V_{DS} = -20 \text{ V}$  and  $V_{GS} = 0$ . At  $V_{DS} \approx -V_{GS(off)} = 2 \text{ V}$ ,  $g_{oss} \approx 100 \mu\text{mho}$ .

The best FETs for current sources are those having long gates and consequently very low  $g_{oss}$ . The Siliconix 2N4869 exhibits typical  $g_{oss} = 1 \mu\text{mho}$  at  $V_{DS} = 20 \text{ V}$ . A single 2N4869 in the circuit of Figure 4 will yield a current source adjustable from  $5 \mu\text{A}$  to  $1 \text{ mA}$  with internal impedance greater than 2 megohms.



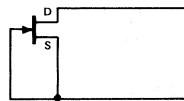
Adjustable Current Source  
Figure 4

The cascade circuit of Figure 5 provides a current adjustable from  $2 \mu\text{A}$  to  $1 \text{ mA}$  with internal resistance greater than 10 megohms.

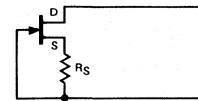


Cascade FET Current Source  
Figure 5

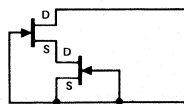
For each circuit discussed,  $g_{oss}$  is represented by the following equations:



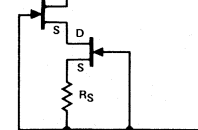
$$g_o = g_{oss}$$



$$g_o \approx \frac{g_{oss}}{1 + R_Sg_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}(1 + R_Sg_{fs})}$$

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## DESIGN IDEA

# Wideband UHF Amplifier with High-Performance FETs

Ed Oxner

### INTRODUCTION

A new freedom in UHF amplifier design is possible with high-performance "Super FETs" such as the Siliconix U310 Junction FET. Typical advantages include a closely-matched 75 ohm input for extremely low return loss in cable systems, and high spurious response rejection with the 3rd order IM intercept measured at +29 dB.<sup>(1)</sup>

Additionally, the high common-gate forward transconductance of the U310 (20,000  $\mu\text{mho}$  maximum) makes it possible to design an amplifier with wide bandwidth and good gain, since the figure of merit ( $g_m/C$ ) of the FET is  $2.35 \times 10^9$  typical – higher than any other known UHF Junction FET.

The amplifier circuit in Figure 1 is designed for 225 MHz center frequency, 1 dB bandwidth of 50 MHz, low input VSWR in a 75-ohm system, and 24 dB gain. Three stages of U310 FETs are used, in a straight forward design.

Typical parameters are taken from the U310 data sheet:

|                              |           |            |
|------------------------------|-----------|------------|
| Forward Transconductance     |           | 14 mmhos   |
| Input Admittance at 225 MHz  | $g_{igs}$ | 13 mmhos   |
|                              | $b_{igs}$ | 4 mmhos    |
| Output Admittance at 225 MHz | $g_{Ogs}$ | 0.27 mmhos |
|                              | $b_{Ogs}$ | 2.6 mmhos  |

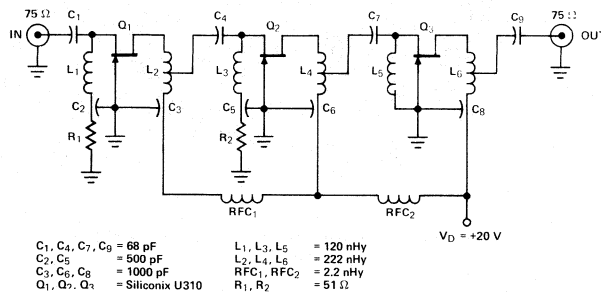


Figure 1

Input match is simplified because the FET input (real) impedance is nearly 77 ohms. A coupling capacitor is used in the amplifier, rather than a tuned circuit, and thus the values may be determined:

$$R_s \sqrt{\frac{R_{ig}}{R_s}} - 1 = X_s = 75 \sqrt{\frac{77}{75} - 1} = 11.85 \Omega$$

$$C_s = \frac{1}{\omega X_s} \approx 68 \text{ pF}$$

$$X_p = \frac{R_s R_p}{X_s} = \frac{75 \times 77}{11.85} = 488 \Omega$$

$$C_p = 1.47 \text{ pF}$$

$$C_T = 4.4 \text{ pF} (C_T = C_p + C_{igs})$$

$$L_s = \frac{1}{\omega^2 C_T} = 120 \text{ nHy}$$

Figure 2 shows that the measured input VSWR in the 75-ohm system indicated an available bandwidth considerably greater than that required for the amplifier design criteria.

Three cascaded synchronous single-tuned stages are used to achieve the desired gain, and thus stage bandwidth and Q are determined:<sup>(2)</sup>

$$\frac{B/W}{f} = \frac{1}{Q} \sqrt{\left(\frac{E_o}{E}\right)^2 - 1}$$

where:

$$\frac{\text{Bandwidth of 3 Stages}^{(3)}}{\text{Bandwidth of 1 Stage}} = \sqrt{2^{1/3} - 1}$$

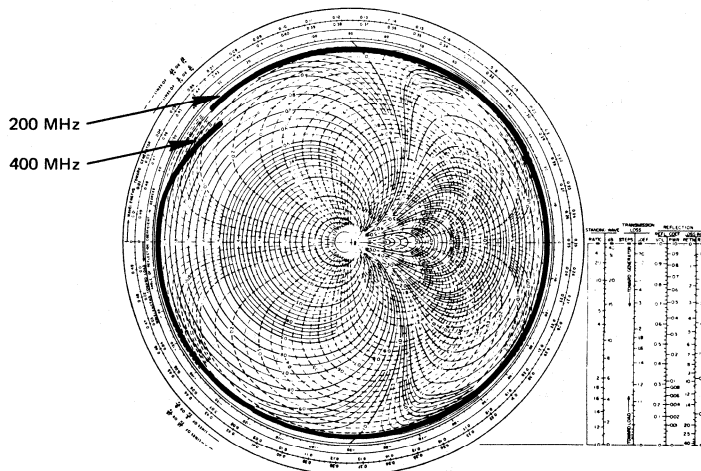
and

$$\left(\frac{E_o}{E}\right) = 1.122 \text{ (1 dB)}$$

giving

$$B/W \text{ (1 dB)} = 98 \text{ MHz}$$

$$Q = 1.15$$



Blanchard Chart (Inverted Circle Impedance Chart)  
Figure 2

With a FET output impedance of 3700 ohms shunted by approximately 2.5 pF (with 0.5 pF allowed for stray capacitance), the total parallel resistance necessary to obtain the desired bandwidth is:

$$Q = \omega CR_t$$

$$R_t = \frac{1.15}{1.415 \times 10^9 \times 2.5 \times 10^{-12}} = 330 \Omega$$

The tank circuit impedance appearing in shunt with the FET, is therefore calculated to be about 365 ohms. From this, the inductance is:

$$L = \frac{R}{\omega Q} = \frac{365}{\omega 1.15} = 222 \text{ nHy}$$

with a turns ratio of 2.3:1 to match to 75 ohms. Since each stage is designed for 75 ohm input and output, three cascaded stages complete the amplifier design.

The computed voltage gain per stage is approximately  $g_{fs} R_t/n$  or 2.22 (7 dB). Measured gain for all three stages is 24 dB. The U310 FET in the final stage operates at  $I_{DSS}$ , and thus accounts for the higher measured gain. The gain/bandwidth response of the amplifier is shown in Figure 3.

The 3rd order spurious intercept point is plotted graphically in Figure 4.<sup>(4)</sup> The importance of a high intercept point becomes apparent in a crowded high-level area of the spectrum where signal purity is of utmost priority.

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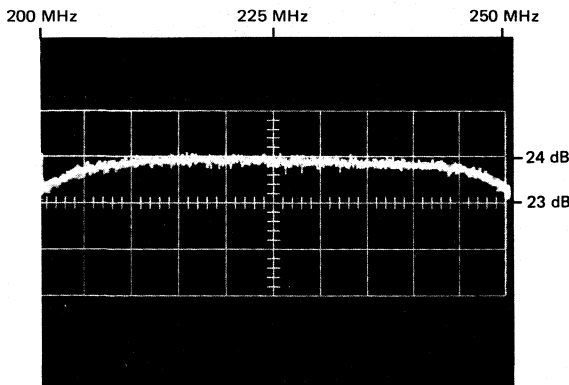


Figure 3

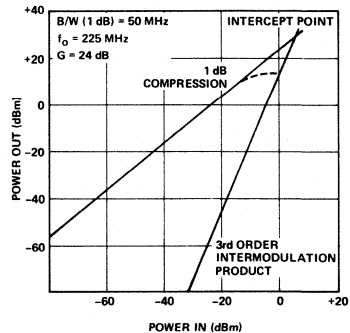


Figure 4





# DESIGN IDEA

## High-Performance FETs In Low-Noise VHF Oscillators

Ed Oxner

Most communications receivers are limited in their dynamic range because of saturation in the early stages of RF amplifiers or mixers. However, some receiver designs are available which overcome this limitation by using parametric amplifiers and converters to achieve spectacular increases in dynamic range. There still remain certain limitations in dynamic range which cannot be remedied by parametric devices. In these cases, the problem lies in the heterodyning of noise sidebands which appear on the receiver local oscillator, entering the passband through strong interfering signals.

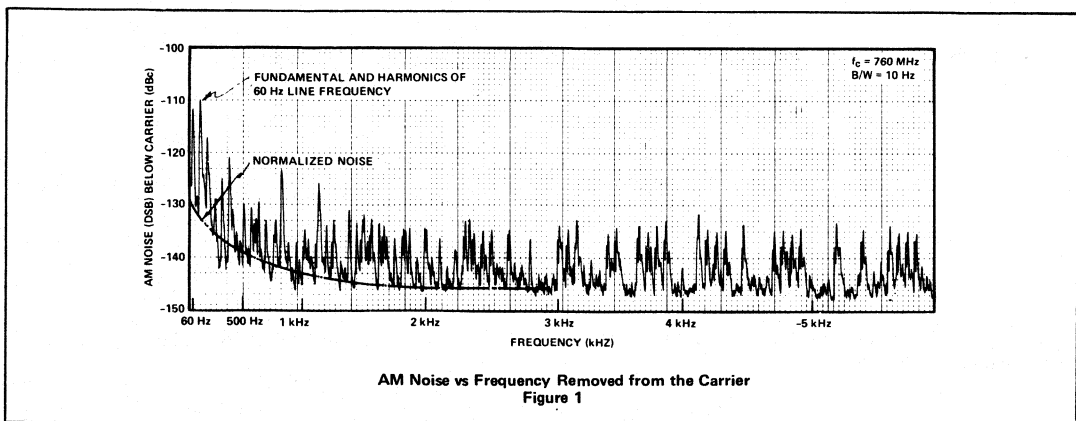
### Common Types of Noise

Although noise is often difficult to characterize because of its random or nondeterministic nature, it is possible to differentiate various forms of noise through an understanding of the Gaussian distribution of noise about an RF carrier. Briefly stated, the three major forms of noise are (1) low-frequency noise ( $1/f$ ); (2) thermal noise ( $4kTRB$ ); and "shot" noise ( $i_n$ ). Further, these types of noise can be identified from their relationship to the main RF carrier. For example, low-frequency noise predominates very close to the carrier, and falls to insignificant levels when it is displaced more than 250 Hz from the carrier. Low-frequency noise is associated with surface contamination and other irregularities, such as gate current leakage.

Thermal noise plays the predominant role in the region from the  $1/f$  decay point to approximately 20 kHz from the carrier, and is commonly associated with equivalent resistance where the rms value of noise voltage of the Thevenin generator becomes the classic  $(4kTBR)^{1/2}$ . Noise appearing beyond the 20 kHz is known as Shot noise, and is directly attributable to noise current. Because of the typically uniform distribution of shot noise it is also referred to as "white noise."

### Origins of Oscillator AM Noise

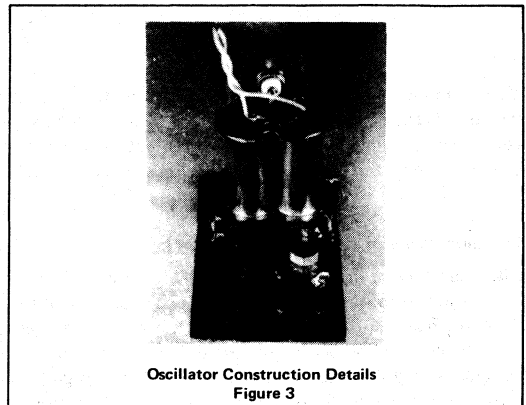
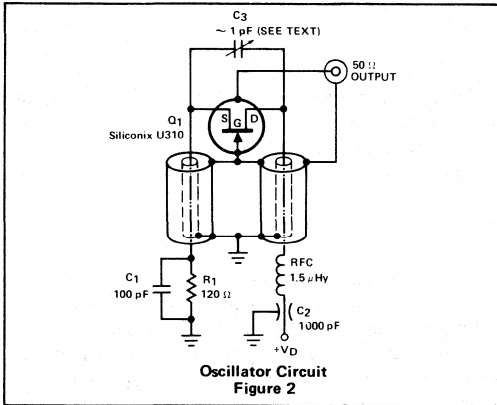
Although an oscillator tends to produce a wave that is nearly sinusoidal, there are other fluctuations present. When the energy in the frequency domain close to the carrier is observed on a spectrum analyzer, noise appears as a modulation phenomenon. This observation would be greatly enhanced if the noise contribution was coherent and consisted of discrete sideband frequencies. Without a doubt, the major component of AM noise is the contribution of low-frequency noise ( $1/f$ ). Both thermal and shot noise are relatively insignificant segments of AM noise when compared to  $1/f$ . A graph of AM noise vs frequency removed is shown in Figure 1.



**Design of a VHF Oscillator**

The important design considerations for best oscillator performance include using a FET with high forward transconductance, maintaining the gate at ground potential, and keeping a high unloaded tank Q. The high transconductance is necessary to reduce the effective noise resistance. The grounded gate reduces the noise voltage contributions to those of the gate leakage current and the series gate resistance. The high tank circuit Q serves as an effective filter for the sideband noise energy.

The oscillator design is somewhat extraordinary for a circuit employing a FET. The FET chosen was the Siliconix U310, which has a forward transconductance value higher than 18 mmho at zero bias ( $V_{GS} = 0$ ). The oscillator basically consists of two coaxial resonators, one for the FET source and the other for the drain. Oscillation is established by capacity coupling between the two resonators; output coupling is derived from the magnetic coupling which exists at the open ends of the resonators. Optimum resonator Q is achieved by designing the coaxial resonators for a characteristic impedance of 75 ohms. The oscillator circuit is shown in Figure 2, and construction details are shown in Figure 3.



The technique to establish the proper resonator length for the desired frequency is somewhat tricky, and requires a first-order approximation of the anticipated capacitive fringing which derives from both the FET and the feedback network. A short circuited coaxial transmission line is theoretically resonant at a quarter-wave length of the resonating frequency, except for the effects of fringe field capacitance. At resonance

$$X_L = X_C \tag{1}$$

If the fringe capacitance is known,  $X_C$  can be calculated as

$$X_C = \frac{1}{\omega C} \tag{2}$$

From this, the resonator length can be determined as

$$X_C = \tan \beta l \tag{3}$$

In making these calculations, a Smith chart is invaluable, as is shown in the following illustration:

|  |                           |
|--|---------------------------|
| Frequency of oscillation                             | = 760 MHz                 |
| FET $b_{igs}$ (from data sheet)                      | = 16 mmho                 |
| Capacitance from $b_{igs}$                           | $C_{gs} = 3.4 \text{ pF}$ |
| Allow for stray capacitance and the feedback network | $C_s = 1.5 \text{ pF}$    |
|  | 4.9 pF                    |

Thus  $X_C = j 0.57$  (normalized to 75  $\Omega$ )

Locate 0.57 on the Smith chart. The wavelength toward the load = 0.081  $\lambda$ . Since a wavelength at 760 MHz is 39.5 cm., then the resonator cavity length is simply

$$39.5 \times 0.081 = 3.20 \text{ cm (1.26 inches)} \tag{4}$$

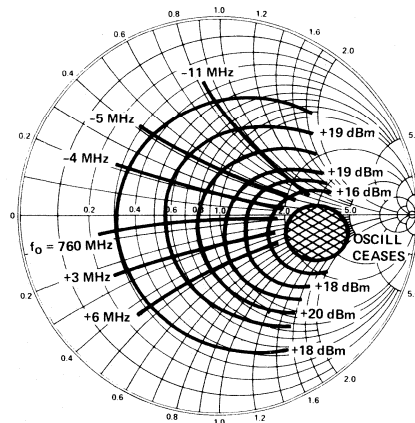
In the completed FET coaxial oscillator circuit, the output coupling loop consists of a single turn made fast to the cavity by the BNC flange and the FET itself. Although the feedback network appears somewhat crude, it can be replaced by a small trimmer capacitor for similar operation.

**Conclusions**

Measured performance of the oscillator is shown in Table IA; AM noise measurements in a 10 Hz bandwidth are shown in Table IB.

| TABLE IA<br>Oscillator Measured Performance @ 25°C |      |       |       |       | TABLE IB<br>AM Noise Measurement |        |  |
|--|------|-------|-------|-------|----------------------------------|--------|--|
|  |      |       |       |       | Frequency Displaced From Carrier | dBc    |  |
| V <sub>DD</sub> (V)                                | +10  | +15   | +20   | +25   | 50 Hz                            | -130   |  |
| I <sub>D</sub> (mA)                                | 15   | 16.2  | 18.2  | 21    | 500 Hz                           | -139   |  |
| P <sub>out</sub> (dBm)                             | +6.6 | +15.2 | +18.3 | +20   | 1 kHz                            | -143.5 |  |
| Frequency (MHz)                                    | 725  | 742.7 | 754.7 | 762.9 | 5 kHz                            | -146   |  |

The Reike diagram shown in Figure 4 makes possible the accurate prediction of expected power output and operating frequency with the oscillator feeding directly into a mismatched load. Expansion of the Reike diagram to show frequency vs transmission line length (in degrees) will allow prediction of the long-line effect on oscillator stability.



Reike Diagram  
Figure 4



# TECHNICAL ARTICLE

## FET Biasing

James Sherwin

### INTRODUCTION

Engineers often design FET amplifiers that are unnecessarily sensitive to device characteristics because they may not be familiar with proper biasing methods.

One way to obtain consistent circuit performance in spite of wide device variations is to use a combination of constant-voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

### Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme, particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the  $V_{GS} = -0.4$  V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage,  $V_{DD}$ , of 30 V and a drain resistance,  $R_D$ , of 39K  $\Omega$  are being used.

The quiescent drain-to-source voltage,  $V_{DSQ}$ , is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of  $\pm 0.2$  V will produce output voltage swings of  $\pm 7.0$  V — a voltage gain of 35.

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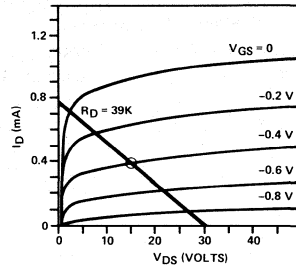


Figure 1. A large dynamic range is provided by the operating point at  $V_{DSQ} = 15$  V,  $I_{DQ} = 0.39$  mA and  $V_{GSQ} = -0.4$  V. The output characteristics are for a typical 2N4339.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for  $V_{GG} = \text{constant}$  on the transfer characteristic of the FET.

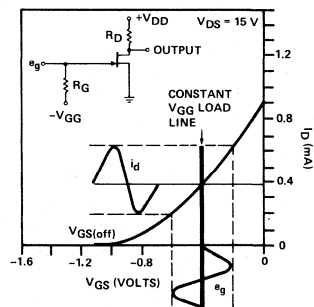


Figure 2. Constant-voltage bias is maintained by the  $V_{GG}$  supply as shown on this typical 2N4339 transfer curve. Input signal  $e_g$  moves the load line horizontally.

The transfer characteristic is a plot of  $I_D$  vs  $V_{GS}$  for constant  $V_{DS}$ . Since the curve doesn't change much with changes in  $V_{DS}$ , it is quite useful in establishing operating bias points. In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

The heavy vertical line at  $V_{GS} = -0.4$  V establishes the Q-point of Figure 1. No voltage is dropped across resistor  $R_G$  because the gate current is essentially zero.  $R_G$  serves mainly to isolate the input signal from the  $V_{GG}$  supply.

Excursions of the input signal,  $e_g$ , combine in series with  $V_{GS}$  so that they add algebraically to the fixed value of  $-0.4$  V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. For an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no resultant gate-source voltage excursion. This bias technique is therefore limited to source followers, source-coupled differential amplifiers, and to ac amplifiers where the source terminal is bypassed to ground at the signal frequency.

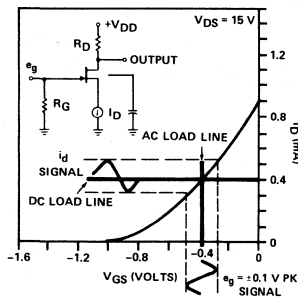


Figure 3. Constant-current bias fixes the output voltage for any  $R_D$ . Hence, input signals cannot affect the output unless the current source is bypassed.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to  $-(1/X_C) = -\omega C$  (Figure 4).

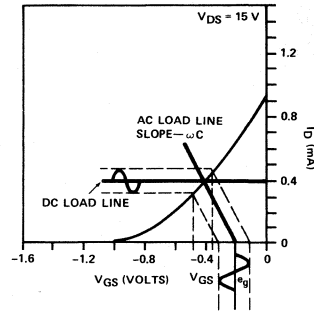


Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from  $e_g$ .

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal,  $e_g$ , is reduced by the drop across the capacitor:

$$v_{gs} = e_g - v_S = e_g - i_S X_C \quad (1)$$

It is clear from Figure 4 that the input signal only shifts the operating point by an amount equal to  $V_{gs}$ , the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

#### Self Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor,  $R_S$ , to the gate. Since no voltage is dropped across  $R_S$  when  $I_D = 0$ , the self-bias load line passes through the origin. Its slope is given by  $-1/R_S$ . Therefore, the desired Q-point is established by setting  $-1/R_S = I_{DQ}/V_{GSQ}$ .

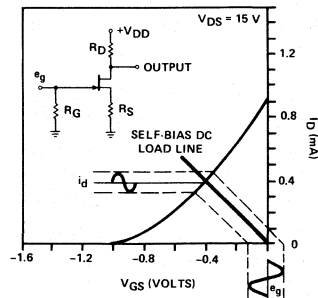


Figure 5. The self-bias load line passes through the origin with a slope  $-1/R_S$ . Bypassing  $R_S$  will steepen the slope and increase the gain of the circuit.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equation 1 with  $X_C$  replaced by  $R_S$ . The ac gain of the circuit can be increased by shunting  $R_S$  with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope  $-(1/Z_S) = -(\omega C + 1/R_S)$ .

The circuit is biased automatically at the desired Q-point, requires no extra power supply and provides a degree of current stabilization not possible with constant-voltage biasing.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing  $V_{GG}$ . (The bias line intercepts the  $V_{GS}$  axis at  $V_{GG}$ .) The larger  $V_{GG}$  is made, the larger  $R_S$  will be and the better will be the approximation to constant-current biasing.

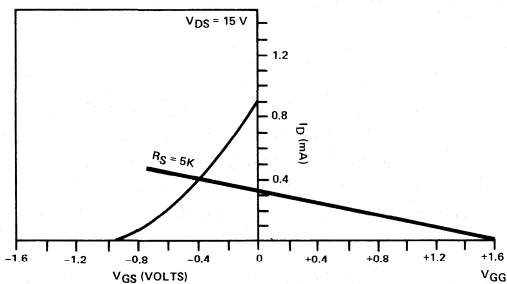
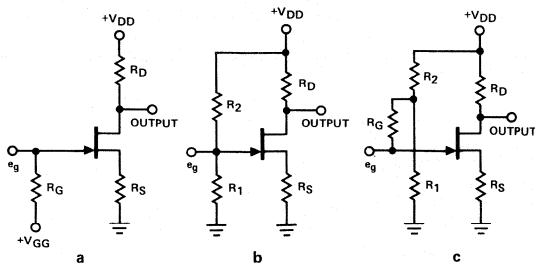


Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

All three circuits in Figure 6 are equivalent. Circuit 6(a) requires an extra power supply. The need for an additional supply is avoided in 6(b) by deriving  $V_{GG}$  from the drain supply.  $R_1$  and  $R_2$  are simply a voltage divider. To maintain the high input impedance of the FET,  $R_1$  and  $R_2$  must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired  $V_{GG}$  in every circuit application. Circuit 6(c) overcomes this problem by placing a large  $R_G$  between the center point of the divider and the gate. This allows  $R_1$  and  $R_2$  to be small, without lowering the input impedance.

One point of caution worth remembering is that as  $V_{GG}$  is increased,  $V_S$  increases, and  $V_{DS}$  decreases. Therefore with low  $V_{DD}$ , there may be a significant decrease in the allowable output voltage swing.

**Biasing for Device Variations**

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7

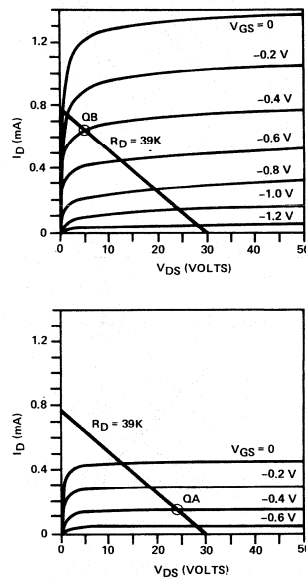


Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

where two limiting sets of output characteristics, representing the actual min-max spread of the Siliconix 2N4339, are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8. (See next page.)

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance — for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating  $I_{DQ}$  for the extreme limit devices. At  $V_{GS} = -0.4$  V, the range of  $I_{DQ}$  is 0.13 to 0.69 mA, and  $V_{DSQ}$  for a given  $R_D$  will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with  $R_D = 39K \Omega$  and  $V_{DD} = 30$  V,  $V_{DSO}$  varies from near saturation (5 V) to 25 V.

An apparently excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets  $V_{DSQ}$  to  $V_{DD} - I_{DQ}R_L$  for any device in the production spread.  $V_{GS}$  automatically finds a value to set the appropriate  $I_{DQ} = \text{constant}$  for all devices. For the constant-current bias plot of Figure 8, with  $I_{DQ} = 0.39$  mA,  $V_{GS}$  would range from  $-0.11$  to  $-0.67$  V.

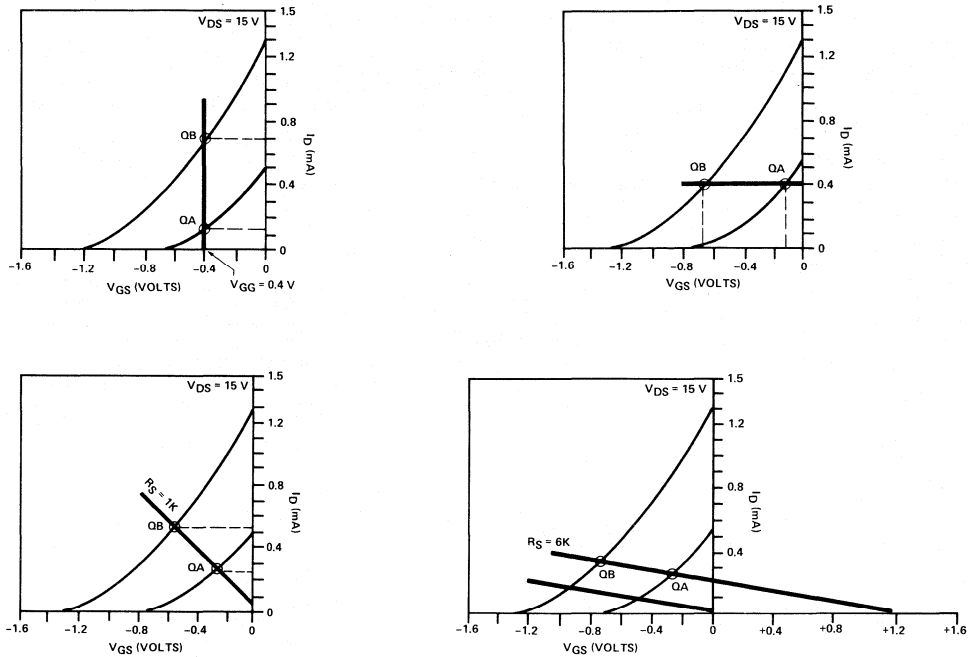


Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Output characteristics are not needed as long as  $I_{DQ}$  is chosen to be below the minimum  $I_{DSS}$ . With  $R_D = 39K \Omega$  and  $V_{DD} = 30V$ ,  $V_{DSQ}$  is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance,  $g_{fs}$ , of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high  $R_S$ .

An appropriate choice of  $I_{DQ}$  limits can be made by using the pair of limiting transfer curves. For example, for  $R_S = 1K \Omega$ , the load line shown on the self-bias curve of Figure 8 is established. The maximum  $I_D$  is 0.52 mA, and the minimum  $I_D$  is 0.24 mA. The operating range of  $V_{DSQ}$  may be calculated for any value of  $V_{DD}$  and  $R_D$ . Clearly, for  $R_D = 39K \Omega$ , the maximum-limit device (device B) would operate with  $V_{DSQ} = 9.8V$  and the minimum-limit device (device A) would operate with  $V_{DSQ} = 20.6V$ . This results in fairly satisfactory operation for all devices. However, such a variation in  $I_{DQ}$  imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with  $V_{GG} = 1.2V$ . The range of  $I_{DQ}$  for

this bias condition is 0.25 mA to 0.32 mA. A similar minimum difference in  $I_{DQ}$  could be achieved with  $R_S = 6K \Omega$  and  $V_{GG} = 0$ , (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows  $v_{gs} = \pm 1.8V$  (limited by  $I_{DSSA}$ ), while the lower line allows a  $v_{gs}$  of only  $\pm 0.7V$  (limited by  $V_{GS(off)A}$ ). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with  $R_D = 62K \Omega$ , the  $V_{DSQ}$  would range only between 10 and 15 V.

For this circuit,  $R_D$  should be chosen to allow the largest output signal swing for  $I_{DQ}$  midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across  $R_D$  at one-half of  $(V_{DD} - 2V_{GS(off)typ})$  or 14 V, yields  $R_D = (14V/0.285mA) = 49K \Omega$ .

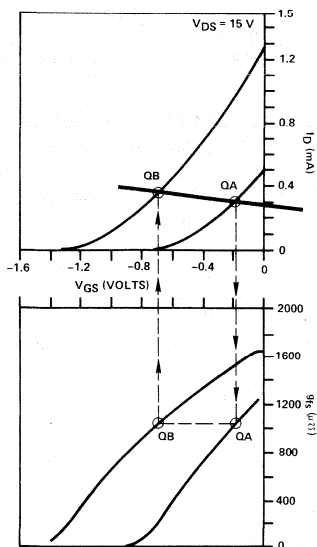
It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.



### Minimize the Gain Variations

Leaving  $R_S$  unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).



**Figure 9.** Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal  $g_{fs}$  (bottom).

As Figure 9 shows, it is possible to find an  $R_S$  and a  $V_{GG}$  that will set  $I_{DQA}$  and  $I_{DQB}$  to values so that  $g_{fsQ}$  will be the same for both devices. The  $g_{fsQ}$  of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

The design procedure is as follows:

- Step 1.** Select a desired  $I_{DQA}$  below  $I_{DSSA}$ . A good value, allowing for temperature variations, is 60% of  $I_{DSSA}$ . This will allow for decreasing  $I_{DSS}$  due to temperature variation and for reasonable signal excursions in load current.
- Step 2.** Enter the transfer curves at  $I_{DQA} \cong 0.6 I_{DSSA}$  (0.3 mA) to find  $V_{GSQA}$ . This  $V_{GSQA} \cong 0.2$  V for the 2N4339.
- Step 3.** Drop vertically at  $V_{GSQA}$  to the minimum limit transconductance curve to find  $g_{fsQA}$ . The value as read from the plot is approximately 1000  $\mu\text{mho}$ .
- Step 4.** Travel across the  $g_{fs}$  plot to the maximum curve to find  $V_{GSQB}$  at the same value of  $g_{fs}$ . This is  $V_{GSQB} \cong -0.7$  V.

**Step 5.** Travel vertically up to the maximum limit transfer curve to find  $I_{DQB}$  at  $V_{GSQB}$ . This is  $I_{DQB} \cong 0.36$  mA.

**Step 6.** Construct an  $R_S$  bias line through points  $Q_A$  and  $Q_B$  on the transfer curves. The slope of the line is  $1/R_S$ , and the intercept with the  $V_{GS}$  axis is the required  $V_{GG}$ .

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can then be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB}) / (I_{DQB} - I_{DQA}) \quad (2)$$

and the bias voltage is

$$V_{GG} = R_S I_{DQB} + V_{GSQB} \quad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. (For n-channel FETs,  $V_{GS}$  is negative and  $I_D$  is positive. For p-channel units, the signs are reversed.)

If the transconductance curves of Figure 9 are not available,  $g_{fs}$  can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the  $I_D$  and  $V_{GS}$  axes. The slope and  $g_{fs}$  are given by:

$$\text{slope} = g_{fs} = I_D(\text{intercept}) / -V_{GS}(\text{intercept}) \quad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point  $Q_A$  and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is  $Q_B$ .

### Designing Without Output Curves

Although the transfer characteristic has been seen to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish  $V_{DSQ}$ . However, if a set of output curves is not available,  $V_{DSQ}$  can be determined or selected from the transfer curve by using the following procedure:

- Step 1.** Establish  $R_S$  and limiting values of  $I_{DQ}$ ,  $V_{GSQ}$  and  $g_{fsQ}$  from the transfer curve.
- Step 2.** Establish  $V_{DD}$  as available, but in no case greater than  $BV_{GSS}$  nor less than several times  $V_{GS(\text{off})}$ . There are special cases where  $V_{DD}$  will be below this limit, but in no case should instantaneous  $v_{dg}$  be allowed to fall below  $2 \times V_{GS(\text{off})}$  if minimum distortion is to be achieved.
- Step 3.** Set  $V_{DSQ}$  approximately midway between  $V_{DD}$  and  $2 \times V_{GS(\text{off})}$ ; lower if large output signals will not be handled.
- Step 4.** Select  $R_D$  to give the appropriate  $V_{DSQ}$ . The formula is:

$$R_D = [(V_{DD} - V_{DSQ}) / 0.5 I_{DQA} + I_{DQB}] - R_S \quad (5)$$

In the example of Figure 8, this procedure would have yielded  $V_{DSQ} = (30-3)/2 = 13.5$  V and  $R_D = (30 - 13.5)/0.5$  (0.52 + 0.24) mA - 1K  $\Omega = 42.5$ K  $\Omega$ .

- Step 5.* Check to ensure that with this  $R_D$ , device B is not in a saturated condition -  $V_{DQB} = V_{DD} - I_{DBQ} R_D > 2V_{GS(off)} + R_S I_{DBQ}$ .  
Decrease  $R_D$  if this condition is not met.

An alternate method, that selects  $R_D$  to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

- Step 3.* Determine required stage gain,  $A_v$ , and set  $R_D = A_v/g_{fsQ}$ .  
*Step 4.* Calculate  $V_{DSQ}$  to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S) I_{DQ} \quad (6)$$

- Step 5.* If necessary, change  $I_{DQ}$ ,  $V_{DD}$ ,  $A_v$  and/or  $R_D$  to obtain an optimum compromise. ■■

### FET SOURCE-FOLLOWER CIRCUITS

Too little knowledge of biasing methods for FET amplifiers sometimes keeps engineers from making maximum use of FETs in circuit designs. The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors.

By considering 10 circuits, which represent virtually every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10(a) through 10(e) have no gate feedback; their input impedances, therefore, are equal to  $R_G$ . Circuits 10(f) through 10(k) employ feedback to their gates to increase the input impedance above  $R_G$ .

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, d and f can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current ( $I_D$ ) stability and increase gain.
- Circuits d, e and k employ FETs as current sources. In circuit d,  $Q_2$  must have a lower cut-off voltage,  $V_{GS(off)}$ , and a lower zero gate-voltage drain current,  $I_{DSS}$ , than  $Q_1$ .
- Circuits e, g, h and k employ a source resistor,  $R_S$ , which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs.  $R_S$  is selected to set  $I_D$  near the specified low-drift operating current. The input-output offset is zero.

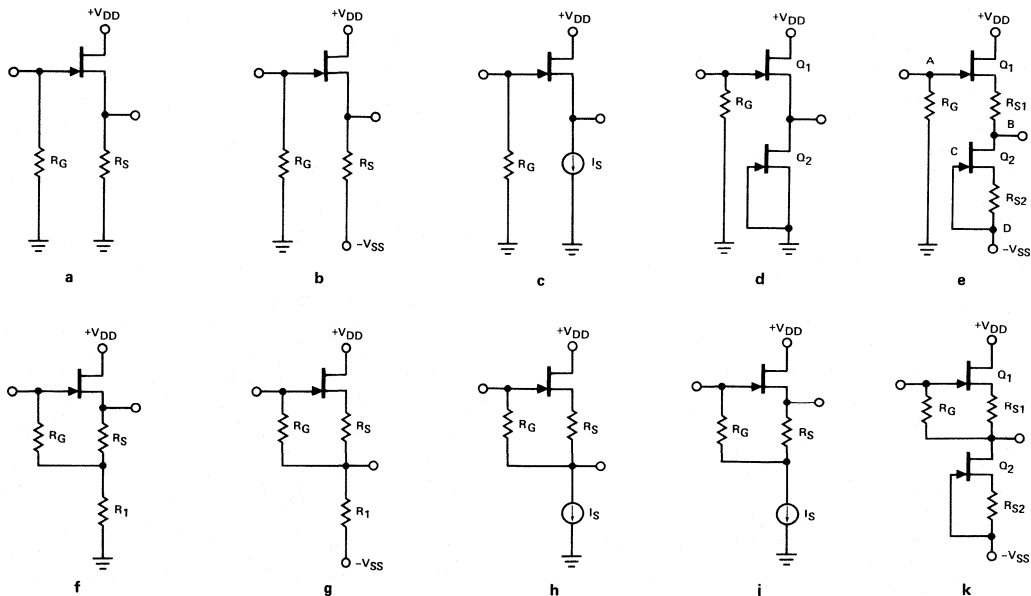
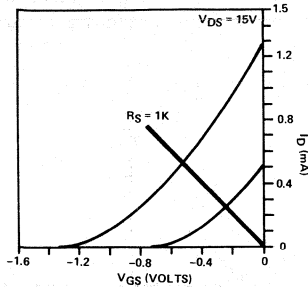


Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

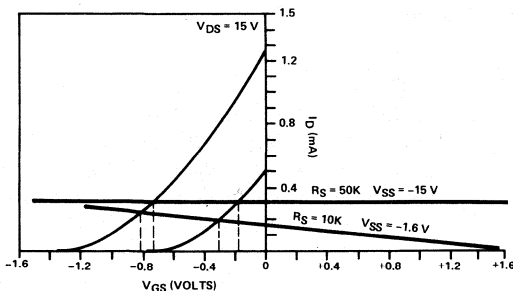
### Biasing Without Feedback is Simple

The no-feedback circuits of Figure 10 (circuits 10(a) through 10(e)) use simple biasing techniques (see the earlier article). Circuit 10(a) is a self-bias configuration; the voltage drop across  $R_S$  biases the gate (which draws essentially zero current) through resistor  $R_G$ . Since no gate-to-source voltage,  $V_{GS}$ , can be developed when  $I_D = 0$ , the self-bias load line passes through the origin (Figure 11). For the 2N4339 FET, whose limiting transfer characteristics are used throughout this article, the quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1K  $\Omega$  source resistor is used. The quiescent output voltage lies between +0.25 and +0.55 V.



**Figure 11.** Self biasing (Figure 10a) uses the voltage dropped across the source resistor,  $R_S$  to bias the gate. The load line passes through the origin and has a slope of  $-1/R_S$ .

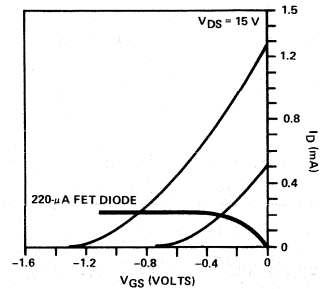
Circuit 10(b) is another example of source-resistor biasing with a  $-V_{SS}$  supply added. The advantage over circuit 10(a) is that the signal voltage can swing negative to approximately  $-V_{SS}$ . Two bias lines are shown in Figure 12, one for  $V_{SS} = -15$  V and the other  $V_{SS} = -1.6$  V. For the first case, the quiescent output voltage lies between +0.18 and +0.74 V. For the second, it lies between +0.3 and +0.82 V.



**Figure 12.** Adding a  $V_{SS}$  supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the  $V_{GS}$ -axis is at  $V_{GS} = -V_{SS}$ . Bias lines are shown for  $V_{SS} = -15$  V and  $V_{SS} = -1.6$  V.

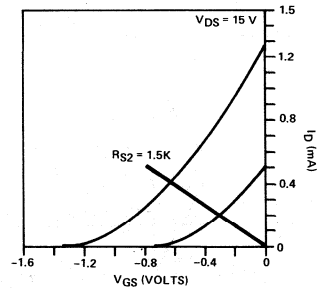
The bias load line for circuit 10(c) is just a horizontal line ( $I_D = \text{constant}$ ). The quiescent output voltage is between +0.15 and 0.7 V for  $I_D = 0.3$  mA.

Circuit 10(d) is similar to 10(c) except that the  $V_{GS} = 0$  output characteristic of FET  $Q_2$  is used as a current source. As seen in Figure 13,  $Q_2$  does not supply constant current when its  $V_{DS}$  gets very small. This technique should therefore be used only to bias FETs whose  $V_{GS(\text{off})}$  is significantly higher than the equivalent  $V_{GS(\text{off})}$  of the current-source FET diode.



**Figure 13.** FET  $Q_2$  doesn't behave like an ideal current source when its  $V_{DS}$  gets very small (Figure 10d). Therefore,  $Q_1$  should have a significantly larger  $V_{GS(\text{off})}$  than  $Q_2$  does.

A pair of matched FETs is used in the circuit of Figure 10(e), one as a source follower and the other as a current source. The operating drain current ( $I_{DQ}$ ) is set by  $R_{S2}$ , as indicated by the load line of Figure 14. The drain current may be anywhere from 0.20 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however,  $V_{GS1} = V_{GS2}$  because the FETs are matched.



**Figure 14.** This load line is set by  $R_{S2}$  and  $Q_2$  which acts as a current source (Figure 10e). If its components are properly matched, the circuit will have zero or near-zero offset.

Since  $I_{D1} = I_{D2}$  and  $V_{GS1} = V_{GS2}$ , choosing  $R_{S1} = R_{S2}$  will ensure that the voltage from point A to B equals the voltage point from point C to D (Figure 10(e)). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating  $I_D$ , the source follower will exhibit zero or near-zero temperature drift.

### Biasing With Feedback Increases $Z_{in}$

Each of the feedback-type source followers (Figure 10(f) through 10(k)) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case,  $R_G$  is returned to a point in the source circuit that provides almost unity feedback to the lower end of  $R_G$ . If  $R_S$  is chosen so that  $R_G$  is returned to zero dc volts (except in circuit 10(f), then the input/output offset is zero.  $R_1$  is usually much larger than  $R_S$ .

Circuit 10(f) is useful principally for ac-coupled circuits.  $R_S$  is usually much less than  $R_1$  to provide near-unity feedback. The bias load line is set by  $R_S$  (Figure 15). The output load line, however is determined by the sum of  $R_S + R_1$ . The feedback voltage  $V_{FB}$ , measured at the junction of  $R_S$  and  $R_1$ , is determined by the intercept of the  $R_S + R_1$  load line with the  $V_{GS}$  axis. The quiescent output voltage is  $V_{FB} - V_{GS}$ .

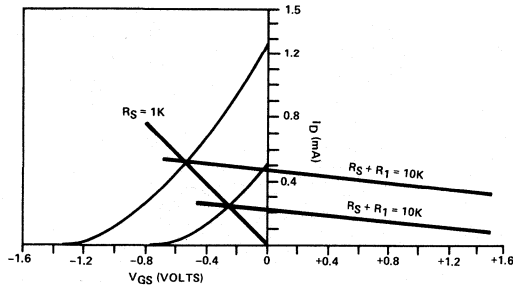


Figure 15. The bias load line is set by  $R_S$  but the output load line is determined by  $R_S + R_1$  when gate feedback is employed (Figure 10f). The feedback  $V_{fb}$  is determined by the intercept of the  $R_S + R_1$  load line and the  $V_{GS}$  axis.

In the circuit of Figure 10(g),  $R_S$  can be trimmed to provide zero offset. As the curves show (Figure 16),  $R_S$  will be between 670 ohms and 2.5K  $\Omega$ .  $R_S$  is much less than  $R_1$ . The source load line intercepts the  $V_{GS}$  axis at  $V_{SS} = -V_{GG} = -15$  V.

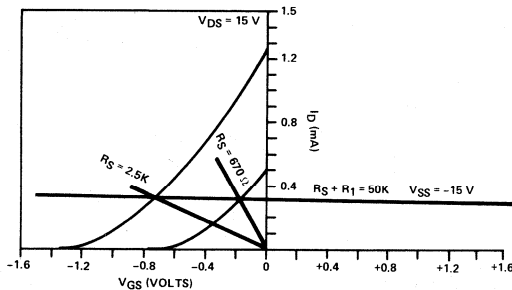


Figure 16.  $R_S$  can be trimmed to provide zero offset at some point between 670 ohms and 2.5K  $\Omega$  (Figure 10g). The source load line intercepts the  $V_{GS}$  axis at  $V_{SS} = V_{GG} = -15$  V. Note that this load line is not perfectly flat. It has a slope of  $-1/50K$ , because the current source is not perfect; it has a finite impedance.

Circuit 10(h) is almost the same as 10(g); the difference is that resistor  $R_1$  is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of

circuit 10(h) differs from that of Figure 10(g) (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of  $-1/50k$ .

Circuit 10(j) is similar to 10(h) except that the output is taken from the top of  $R_S$  to reduce the output impedance.  $R_S$  must be trimmed if the circuit is to work at all properly.

In Figure 17, the constant-current load line represents a 0.3-mA current source, and the effect of a 1K  $\Omega$  source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the  $R_S$  load line and the  $V_{GS}$  axis sets the voltage at the junction of  $R_S$  and the current source ( $V_{FB}$ ). For  $R_S = 1K \Omega$ ,  $V_{FB}$  will be between  $-0.1$  V and  $+0.45$  V. Since  $V_{FB}$  appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

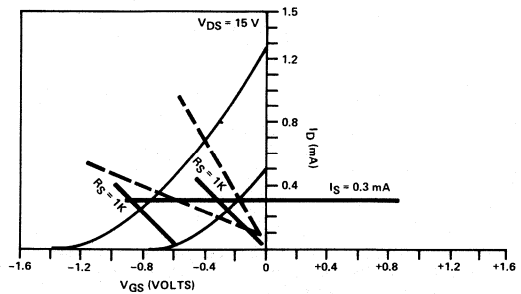


Figure 17. If  $R_S$  is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

This can be done by trimming  $R_S$ , as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10(h).

Biasing for circuit 10(k) is identical to that for circuit 10(e) (Figure 14) except that feedback is added to raise the input impedance. ■

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- (1) Sherwin, J.S., "How, Why and Where to Use FETs," *Electronic Design*, May 17, 1966, p. 94.
- (2) Sherwin, J.S., "Knowing the Cause Helps to Cure Distortion in FET Amplifiers," *Electronics*, Dec. 12, 1966, pp. 99-105.

## APPLICATION NOTE

# Don't Trade Off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches

Walt Heinzer

### INTRODUCTION

For analog switches, Vertical MOS (VMOS) transistors give you a nearly ideal combination of characteristics—without the tradeoffs required by the more conventional components. These devices are now available from two American suppliers: Siliconix and its licensee, Semtech.

Unlike the commonly used N-channel JFETs, VMOS chips that handle more than a few hundred milliamps are also small enough for economical production. Smaller chips lead to lower inherent capacitances. Moreover, the basic VMOS structure provides lower ON resistance.

Some analog switches use relays, bipolar transistors and even triacs. Although electromechanical relays offer the lowest ON resistance initially, their ON resistance will vary with current and degrade with use. Also, relays suffer from mechanical limitations.

Bipolar transistors require base-drive current that causes offset in the switched analog signal. Triacs are only suitable for switching raw power; for analog switching, they introduce too much offset and non-linearity although they easily handle high power.

### VMOS Offers High Performance

VMOS devices aren't limited by any of these disadvantages. They can switch 10 W, linearly, over a wide dynamic range. In addition, VMOS input impedance is very high, and only input voltage (no current) turns the transistors OFF or ON.

And since the drain-to-source channel is purely resistive while ON, you get low distortion.

VMOS transistors in analog switches offer several more advantages, including

- 1.8  $\Omega$  ON resistance, which results in low insertion loss in low-impedance systems
- 2.0 A DC current capability—paralleling three VMOS devices increases this capability to 6.0 A and unlike other devices, paralleled VMOS do not require power-wasting ballast resistors
- 3 A peak current, which makes VMOS super for driving capacitive lines and quickly charging and discharging capacitors in high speed A/D converters, sample and hold circuits, and integrators
- 60 dB isolation at 10 MHz and 500 nA DC leakage in the OFF state
- Enhancement-mode operation with a 0.8 to 2.0 V threshold, which gives VMOS direct compatibility with CMOS and TTL. And the logic gates aren't loaded by the VMOS.
- Linear ON resistance, which results in low total harmonic and intermodulation distortion

What's more, all these capabilities come in a TO-202AA package.

Examine the output characteristics of a low resistance VMOS device like the Siliconix VN46AF. A look at the transfer characteristic in Figure 1A reveals that varying the gate-to-source voltage from 0 to +10 V switches the VN46AF from OFF to ON—with a 3  $\Omega$  ON resistance. From the curve you can see that the device turns OFF well before zero volts, which eases interfacing with logic.

In the VN46AF schematic in Figure 1B, note that the body and source are internally connected. Figure 1C and 1D, respectively, show simplified models of the VN46AF's OFF and ON states. Diode D<sub>1</sub> is the body-to-drain PN junction. When the VN46AF is OFF, its drain current vs drain-to-source voltage characteristics (Figure 1E) is essentially the curve for D<sub>1</sub>.

The breakdown for D<sub>1</sub> is 40 V, and the diode exhibits forward conduction for drain-to-source potential as low as -0.6 V. This diode therefore constrains the analog voltage, which a simple switch (one VMOS transistor) can handle, to between -0.6 and +40 V.

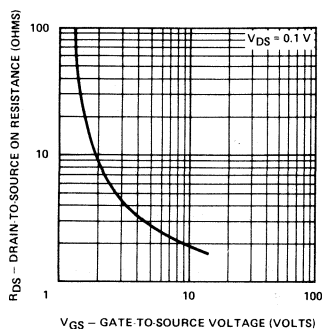
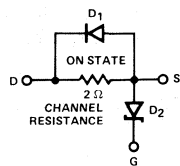
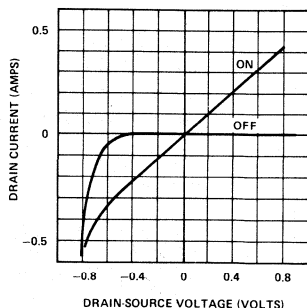
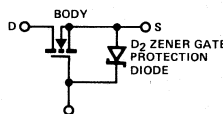
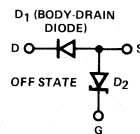


Figure 1A

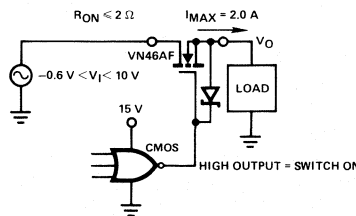
Equivalent ON Condition  
( $V_{GS} = 10\text{ V}$ )  
Figure 1DSmall Signal Characteristics of VN46AF  
Figure 1ESchematic Symbol of VN46AF  
Figure 1BEquivalent OFF Condition ( $V_{GS} = 0$ )  
Figure 1C

When the VN46AF is ON, a 2  $\Omega$  resistance is in parallel with D<sub>1</sub>. Maximum continuous current in either direction is 2.0 A, even though the diode is forward-biased for currents over 0.5 A.

### One VMOS Device Makes an Analog Gate

VMOS characteristics are put to good use in the analog switch of Figure 1F. In the ON state, the gate of the VN46AF is positive with respect to the source. In the OFF state, the gate-to-source voltage is zero. The 2.0 A capability and the 3  $\Omega$  ON resistance of the VMOS transistor can be fully exploited in this circuit. The input signal, however, is restricted to positive voltages and must always be greater than the output voltage. Otherwise, OFF isolation is impaired.

Both ON and OFF switching takes 200 ns; charge feed-through during the ON-to-OFF transition is 80 pC with a 50  $\Omega$  load. Charge transfer is, of course, especially important in sample and hold systems. For example, 80 pC into 0.01  $\mu$ F causes an offset of 8 mV.

A Simple Unidirectional VMOS Analog Switch ( $v_i > v_o$ )  
Figure 1F

The VN46AF switches from OFF to ON with a 3  $\Omega$  drain-to-source resistance, when its gate-to-source potential swings from 0 to +10 V. The device turns OFF at about 1 V(A). Some VMOS transistors (B) carry an on-board zener diode that protects the gate-to-source junction. A VMOS transistor is equivalent to two diodes in the OFF state (C), when the gate-to-source voltage is less than the threshold value. The equivalent diode, D<sub>1</sub> is shunted by 3  $\Omega$  when the VMOS device is ON (D), with the gate-to-source potential at +10 V. The small signal drain-to-source voltage vs current characteristic (E) is essentially determined by the body-to-drain diode. The input is restricted to positive voltages in the single-VMOS analog gate (F).

Figure 1

**In Series, They Switch Both Polarities**

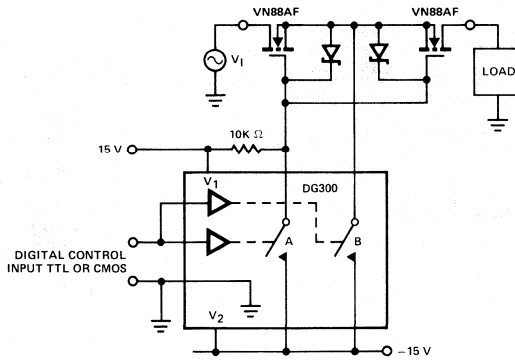
To increase the switch's dynamic range, connect two VN88AF's in series (Figure 2A). In the ON state, both halves of the DG300 analog switch are open, so the gates of both VN88AF's are pulled to +15 V through the 10K  $\Omega$  resistor. The ON resistance of this analog switch is twice as high as the drain-to-source resistance of a single VN88AF. The maximum current that this two-transistor switch can handle is the same as that for a single-transistor switch (2.0 A).

The switch is turned OFF by shorting the gates to the negative supply, thereby reducing the gate-to-source voltage to less than the threshold of 0.8 V. The second section of the DG300 adds 30 dB OFF isolation by shunting the signal-leakage path (through both sources) to the negative

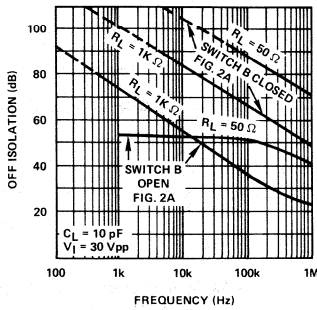
supply. OFF-isolation curves (Figure 2B) show that the DG300 raises the circuit's isolation and that decreasing the load resistance increases isolation.

Since the two transistors are back-to-back, one body-to-drain diode is always reverse-biased. This eliminates the OFF-state problem caused by forward-biasing the diode.

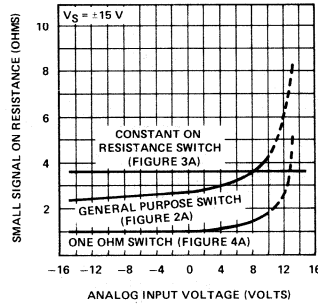
Since the bidirectional switch's gate drive is referenced to a fixed supply, its ON resistance varies with the input analog voltage (Figure 2C). This variation introduces distortion when you're driving low-impedance loads such as speakers or transmission lines. For constant ON resistance, use the circuit in Figure 3A.



**A General Purpose Bidirectional Analog Switch**  
Figure 2A



**OFF Isolation vs Frequency**  
Figure 2B



**Small Signal ON Resistance vs Analog Input Voltage**  
Figure 2C

ON resistance is doubled in the two-VMOS switch (A), but inputs of both polarities are handled without losing isolation. The DG300 analog gate (B) raises the circuit's isolation by 30 dB. Decreasing load resistance also improves isolation. With the gate drive referenced to a fixed voltage (C), the ON resistance varies undesirably with the input, and generates distortion, especially with low impedance loads like speakers and transmission lines.

Figure 2

## Bootstrapping Adds Linearity

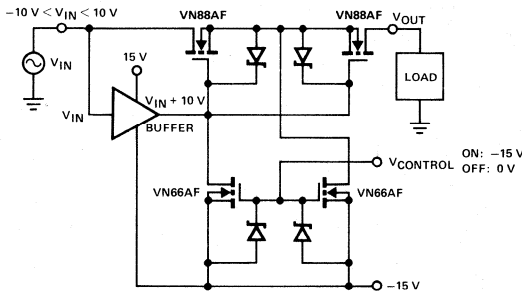
In the ON state, a bootstrap voltage that tracks the input drives the gates of the VN88AF's. This bootstrapping keeps the VMOS's gate-to-source voltage constant and independent of the input signal. So, changes in the input-signal level do not modulate the ON resistance of the switch.

The buffer circuit reduces the computed total harmonic distortion from 1.5% to 0.005%, for 8 Vrms at 1 kHz into 50  $\Omega$  (Figure 3B). The popular 10  $\Omega$  DG186 JFET analog switch generates a higher total harmonic distortion of about 2%.

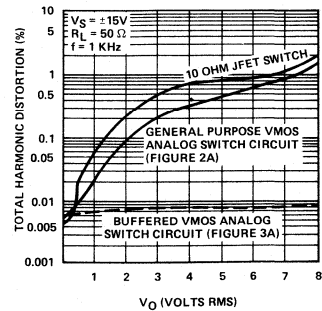
The two buffer circuits shown in Figures 3C and 3D isolate the input signal and employ a zener diode to provide a fixed gate-to-source voltage. The general-purpose buffer of

Figure 3C has a flat frequency response of up to 300 kHz and accepts inputs ranging between  $\pm 15$  V. The buffer of Figure 3D, VN66AK source follower, has its frequency response extended to 50 MHz and, when operated from  $\pm 30$  V supplies, increases the signal range to  $\pm 30$  V.

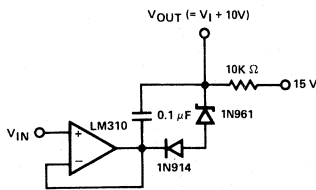
The VN66AK and VN88AF do not have on-board zener diodes like the VN66AF transistor. At the expense of the diode protection, the VN66AK and VN88AF gain lower capacitance from gate-to-source and reduced DC "see through" from driver to signal path. Bootstrapping the switch's gate circuits with a buffer permits the switch to operate with low distortion even as the signal amplitude comes close to the positive supply voltage.



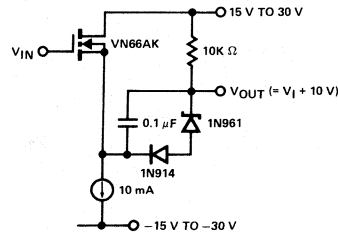
Low Distortion Constant ON Resistance Switch  
Figure 3A



Distortion Improvement Using  
the Buffered Analog Switch  
Figure 3B



General Purpose Buffer  
Figure 3C



High Speed Buffer  
Figure 3D

Bootstrapping the gate and input cuts distortion by holding the ON resistance constant (A). The buffered bootstrap circuit (A) distorts less than either a JFET or a nonbootstrapped VMOS analog switch (B). A general-purpose buffer (C) using the LM310 op amp is suitable for low speed switches, but when you need a fast analog switch, use the VN66AK buffer (D). In addition to speed, this buffer gives you increased isolation.

Figure 3



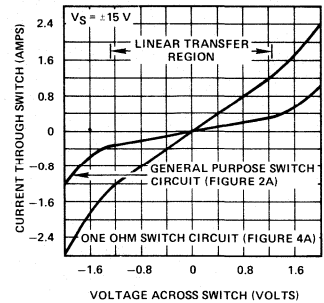
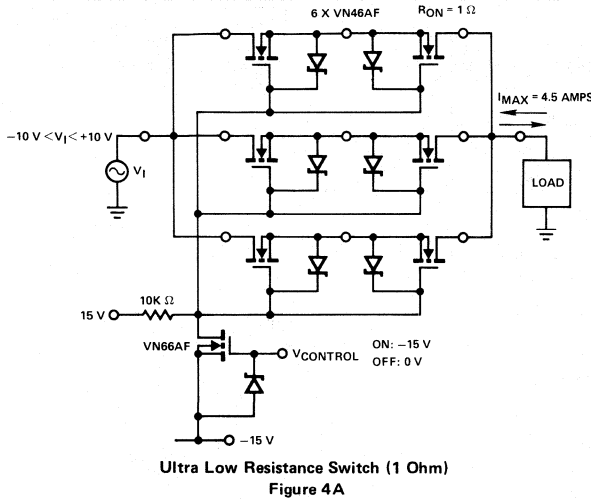
**VMOS Devices Parallel Without Padding**

Paralleling devices lowers the total ON resistance. For example, three paralleled legs, each with two VN46AF's in series, make a 1 Ω switch (Figure 4A). Because VMOS devices are immune to current hogging, no ballast or balance resistors are needed. Negative tempcos, a VMOS feature, cause these devices to draw less current as they heat up. As a result, excess current is automatically shared by paralleled VMOS devices.

Paralleling three VN46AF's not only decreases ON resistance, but also increases the current capability to 6.0 A

and extends the linear range of the large signal transfer characteristic from 0.3 to 1.2 A (Figure 4B).

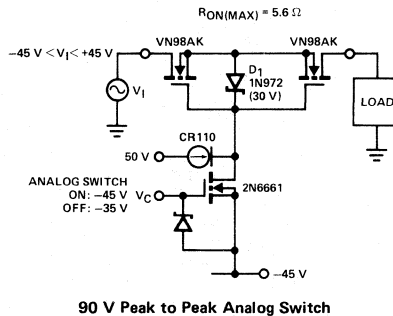
The voltage range of the basic analog switch can also be increased. Simply use a higher breakdown VMOS unit (Figure 5). The VN98AK's have a 90 V breakdown, which allows up to ±40 V of voltage swing capability. However, these higher voltage devices do carry a penalty—the ON resistance is higher: 3.5 Ω vs 3.0 Ω for the VN46AF. Zener diode D<sub>1</sub> limits the gate-to-source potential to 30 V, and thereby prevents a possible gate-oxide rupture. Diode CR110 limits the current from the 50 V gate-bias supply.



**Large Signal Transfer Characteristics**  
Figure 4B

No ballast or balance resistors are needed when VMOS devices are paralleled (A) because negative tempcos immunize them from current hogging. Paralleling extends the linear range from 0.3 to 1.2A (B) as it decreases the ON resistance of the analog switch to 1 Ω and increases its current-handling capability to 4.5 A.

Figure 4



You pay for 90 V breakdown in the VN98AK with 3.0 Ω ON resistance, which allows swings of ±40 V. The zener diode limits the gate-to-source potentials to 30 V.

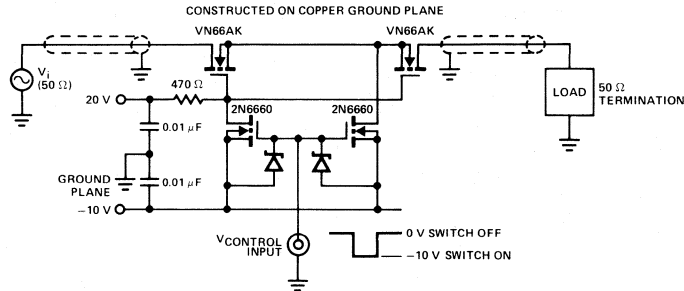
Figure 5

For the Ultimate in Switching Speed

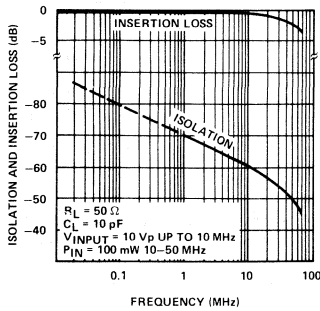
The high power RF switch shown in Figure 6A performs very well up to 50 MHz—with turn-ON and turn-OFF times of 50 ns. At 10 MHz, isolation is 60 dB with a 20 V pk-pk input signal. Insertion loss is only 1 dB with a 50 Ω load (Figure 6B). The gain vs input power curve in Figure 6C shows that the RF analog switch using VN66AK's can put 1 W into a 50 Ω load at 14 MHz. The two-tone, third order, intermodulation product curves show a 42 dB

intercept point with 1 dB of gain compression at 25 dBm input power.

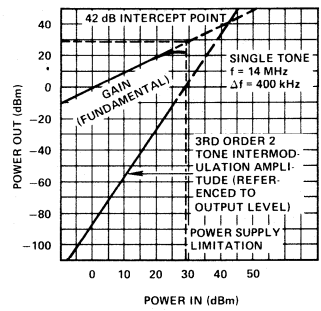
Turn-ON time of the switch (Figure 6D) is determined by the passive pull-up resistor combined with the capacitance at the gates of the VN66AK's. The negative turn-OFF transient is caused by charge-coupling to the output through the output capacitance of the VN66AK.



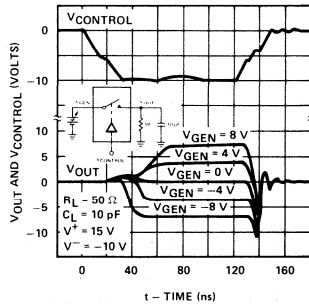
RF Analog Switch  
Figure 6A



Insertion Loss and Isolation vs Frequency of RF Analog Switch  
Figure 6B



Gain and Two Tone 3rd Order Intermodulation  
Figure 6C



Switching Response of RF Switch into 50 Ohm Load  
Figure 6D

The VN66AK switches high power at RF (A). At 10 MHz, a 20 V pk-pk signal is attenuated by 60 dB and the insertion loss is only 1 dB into 50 Ω and 10 pF (B). Third-order intermodulation distortion is given by the 42 dB intercept point, and 1 dB gain compression occurs at 25 dBm input for 14 MHz (C). The negative turn-OFF transient (D) is caused by charge-coupling to the output through the output capacitance of the VN66AK.

# APPLICATION NOTE

## Driving VMOS Power FETs

Dave Hoffman  
January 1979

### INTRODUCTION

Using VMOS Power FETs you can achieve performance never before possible—if you drive them properly. This article describes circuits and suggests design methods to be used in order to obtain the performance from VMOS that you need.

When designing with VMOS there are some facts that must be kept in mind in order to get optimum results with every circuit. The first fact is that VMOS is a very high frequency device. The cut-off frequency for all VMOS FETs is several hundred megahertz. Most power designers are not used to designing with extremely high frequency devices because with bipolars the frequency response decreases as the power increases. The very high frequency response of VMOS is the basis for many of its advantages but it must be kept in mind while designing. With improper circuit design VMOS can oscillate. This oscillation can be eliminated, though, by exercising two simple precautions. First, minimize lead and trace lengths whenever possible, especially leads associated with the gate of the FET. If it is not possible to have short leads to the gate place a ferrite bead on the gate lead or a small resistor in series with the gate. The ferrite bead or the resistor must be very close to the gate. Second, because of the extremely high input impedance of VMOS (in excess of  $10^{12} \Omega$ ) drive circuits may be designed which are very high impedance. Under these conditions it is possible for the gate node to get enough positive feedback from the gate-to-drain capacitance or just from stray fields in the circuit to cause oscillation. This must be kept in mind in the design of the circuit.

When driving VMOS it must be kept in mind that the dynamic input impedance is very different than the static input impedance. The input of a VMOS device is capacitive. The DC input impedance is very high but the AC input impedance varies with frequency. Because of this effect, the rise and fall times of VMOS are dependent on the output impedance of the circuit driving it. The first approximation of the rise or fall time is simply

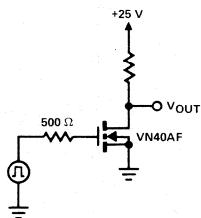
$$t_r \text{ or } t_f = 2.2 \cdot R_{OUT} \cdot C_{iss} \quad (1)$$

where  $R_{OUT}$  is the output impedance of the drive circuit. This equation is valid only if the drain load resistance is much larger than  $R_{OUT}$ . Knowing this fact, along with the fact that there is no storage or delay time with VMOS, it is very easy to calculate the rise and fall times and set them to any desired value. For example, if you wanted to calculate the 10% to 90% rise or fall time for the circuit shown in Figure 1 using Equation 1 the rise time is equal to:

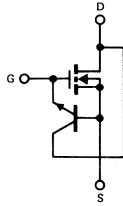
$$t_r = (2.2) (500) (50 \times 10^{-12}) = 55 \text{ nsec}$$

The dynamic input characteristics of VMOS are covered very thoroughly in Siliconix' application note AN79-3.<sup>1</sup>

A last thing to remember when you are driving VMOS is the input protection zener diode. When putting a positive voltage on the gate with respect to the source, the maximum voltage rating of the zener diode should not be exceeded. It is more important, however, that you do not forward bias the zener diode by putting a negative voltage on the gate while the VMOS is operating in a circuit. The reason for this is most easily explained by referring to Figure 2. As can be seen in the figure, the zener diode is actually the base-emitter junction of a bipolar transistor. If a negative voltage greater than 0.6 V is placed on the gate, the base-emitter junction of the bipolar will be forward biased which will turn on the bipolar transistor. When the bipolar is turned on, current will flow from the drain through the bipolar and out the gate. This operating condition is very likely to be destructive. If negative voltages must be placed on the gate it is recommended that you use a VMOS part that does not have an input zener diode. Non-zenered equivalents are available for most of Siliconix' zenered devices.

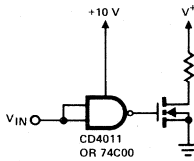


**A Typical VMOS Switching Circuit**  
Figure 1

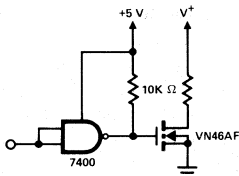


**A Parasitic NPN Transistor in Zener Protected MOSFETS**  
Figure 2

Of all operating modes the common-source configuration is the simplest to drive. Because of the high input impedance of VMOS it can be driven directly from many logic families. When driving from a CMOS gate as shown in Figure 3, rise and fall times of about 60 nsec can be expected due to the limited source and sink currents available from the CMOS gate.<sup>2</sup> If faster rise and fall times are required there are several ways to obtain them. One easy way is if there are extra gates in the package that is driving the VMOS simply put the extra gates in parallel with the gate already being used. The additional current available will cut down the rise and fall times. If no extra gates are available an emitter-follower buffer can be used as shown in Figure 4. With this circuit the current available to the VMOS will be the output current of the CMOS multiplied by the beta of the bipolars. Because the bipolars are operating as emitter-followers there will still be no storage time to worry about and the frequency limit will be determined by either the CMOS gate or the  $f_T$  of the bipolars, whichever comes first.



**Driving VMOS with a CMOS Gate**  
Figure 3

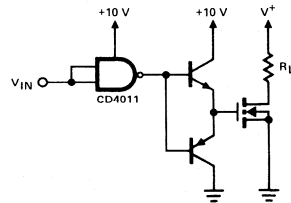


**Pulling Up a TTL Output Will Increase the Sink Current of the VMOS**  
Figure 5

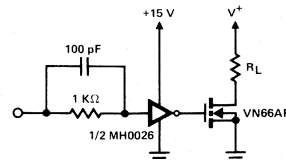
VMOS can also be driven directly from TTL gates. Because the output voltage of TTL is limited, the output current of the VMOS will be limited to some value less than its maximum rated current. The output current that can be expected can be determined from the transfer characteristic of the device being used. For example, if a TTL gate is driving VN46AF the minimum output current of the VMOS will be approximately 250 mA. This value was obtained by using the minimum output voltage of the TTL gate (3.2 V) for a high level output and referring to the transfer characteristic for the VN46AF which is the VMOS geometry used in the VN46AF. If more than 250 mA is required the output of a standard VMOS gate can be pulled up to the 5 V rail as shown in Figure 5. With a full 5 V on the gate the VN46AF will typically sink 600 mA.

For very high speeds a capacitive driver such as the MH0026 can be used as shown in Figure 6. With this drive configuration typical rise and fall times are less than 10 nsec.

When operated in the common-drain mode VMOS is somewhat more difficult to drive than when in the common-source mode. Because of VMOS' high input impedance, though, it is considerably easier to drive common-drain than a bipolar would be when operated common collector. Common-drain circuits can be used when the load needs to be connected to ground, when an active pull-up and pull-down is required (totem pole circuit), or in bridge type circuits. For the purpose of this discussion all examples will be shown with totem pole circuits.

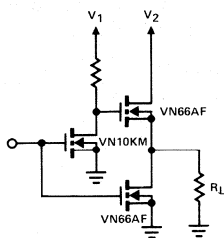


**An Emitter-Follower Circuit Will Decrease VMOS Rise and Fall Times**  
Figure 4



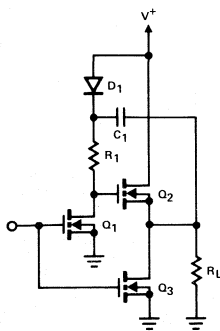
**Using an MOS Clock Driver to Drive VMOS**  
Figure 6

The difficulty with common-drain circuits occurs because as the voltage across the load increases the enhancement voltage of the common-drain device decreases. Referring to Figure 7, as the voltage across  $R_L$  approaches  $V_2$  the enhancement voltage for the upper VN66AF decreases. If  $V_1$  is not greater than  $V_2$  then the voltage across  $R_L$  can never reach  $V_2$ . For this reason whenever a common-drain circuit is used it is always necessary to have or to generate a voltage that is greater than the voltage which is desired to be impressed across the load. The amount the voltage has to be above the desired drain voltage is dependent upon the current the VMOS must source and can be determined from the transfer characteristic of the VMOS being used. If no supply voltage is available other than the one the load is to be pulled up to, one can be generated. This can be done very easily because of the very low drive current requirements of the VMOS.



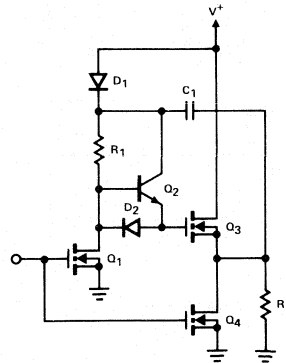
VMOS in Totem-Pole Configuration  
Figure 7

One way of generating the required gate voltage is the bootstrap circuit shown in Figure 8. In the circuit, when  $Q_1$  and  $Q_3$  are on,  $C_1$  is charged to the supply rail through  $D_1$ . When  $Q_1$  and  $Q_3$  are turned off, the gate voltage on  $Q_2$  goes to the supply rail. As the source of  $Q_2$  begins to pull  $R_L$  up, the voltage across  $C_1$  will be maintained, therefore, the gate-to-source voltage of  $Q_2$  will be maintained. The size of  $C_1$  should be large enough so that when it charges the gate capacitance of  $Q_2$  a minimum voltage equal to the required enhancement voltage of  $Q_2$  will be

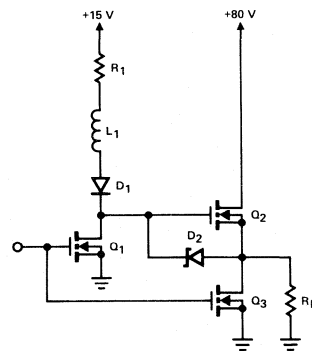


VMOS Bootstrap Circuit  
Figure 8

maintained across it. A good rule of thumb is to make  $C_1$  equal to ten times the  $C_{ISS}$  of the FET. Figure 9 shows the same bootstrap circuit with some added components to improve the rise and fall times. In the circuit  $Q_2$  acts as an emitter-follower to increase the peak gate current to  $Q_3$ .  $D_2$  will be forward biased when  $Q_1$  turns on and serves as a low impedance path to discharge the gate of  $Q_3$ .



Bootstrap Circuit with Emitter-Follower  
for Improved Rise Times  
Figure 9

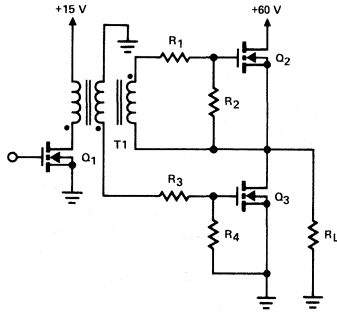


Inductive Kickback Drive Circuit  
Figure 10

Another method to drive a common-drain VMOS FET is shown in Figure 10. Rather than charging a capacitor and then feeding a signal back from the output as was done in the bootstrap circuit, this circuit stores the required charge in an inductor. When  $Q_1$  is turned off a flyback voltage is generated across the inductor. This voltage is used to maintain an enhancement voltage equal to the voltage of zener diode  $D_2$  across the VMOS FET. Once the  $Q_2$  has been fully turned on and the voltage on  $R_L$  is at the rail a negligible amount of energy is required to keep  $Q_2$  on.  $Q_2$  will remain on until  $Q_1$  is turned on, or until the leakage currents of  $Q_1$  and  $D_2$  discharge the gate capacitance of  $Q_2$ .

Another method that can be used to drive a common-drain VMOS is transformer drive. A transformer drive circuit is shown in Figure 11. In this circuit the transformer is used in the flyback mode when turning on the upper FET.  $R_1$  and  $R_3$  are used to suppress ringing and  $R_2$

and  $R_4$  are used to assist with turn-off of the FETs. When driving with a transformer, care must be taken to design the transformer so that the secondary inductance in conjunction with the input capacitance of the FET does not create ringing of oscillation problems.



Transformer Drive Circuit for VMOS  
Figure 11

### SUMMARY

The very high input impedances of VMOS Power FETs greatly simplify the drive requirements as compared to bipolars. The input drive requirements for both common-source and common-drain configurations were discussed in detail. With common-source circuits the requirement that needs to be kept in mind is the rise and fall time required. With common-drain circuits a method of maintaining an adequate enhancement voltage must be considered in addition to required rise and fall time requirements.

### REFERENCES

1. A. Evans, D. Hoffman, "Dynamic Input Characteristics of a VMOS Power Switch" AN79-3.
2. D. Hoffman, L. Schaeffer, "VMOS — A Breakthrough in Power MOSFET Technology" AN76-3.

**Document  
Number**

**Title**

**Application Notes**

- AN70-1 FET Cascade Circuits Reduce Feedback Capacitance
- \* AN70-2 FETs for Video Amplifiers
- AN71-1 A High Resolution CMRR Test Method
- \* AN72-1 FETs in Balanced Mixers
- \* AN72-2 FETs as Analog Switches
- AN73-1 FETs as Voltage-Controlled Resistors
- AN73-2 IC Multiplexer Increases Analog Switching Speeds
- AN73-3 Switching High-Frequency Signals With FET Integrated Circuits
- AN73-4 Junction FETs in Active Double-Balanced Mixers
- AN73-5 Driver Circuits for the JFET Analog Switch
- \* AN73-6 Function/Application of the L144 Programmable Micro-Power Triple Op Amp
- \* AN73-7 An Introduction to FETs
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- AN74-3 Designing Junction FET Input Op Amps
- \* AN74-4 Audio-Frequency Noise Characteristics of Junction FETs
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- \* AN76-3 VMOS—A Breakthrough in Power MOSFET Technology
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- \* AN77-1 Function/Application of the LD120/LD121 4½ Digit A/D Converter Set in Measurement Systems
- \* AN77-2 Don't Trade off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches
- \* AN77-3 Function/Application of the LD120/LD121 4½ Digit A/D Converter Interfaced with an 8080A Microprocessor
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- \* AN79-1 A 500 KHz Switching Inverter for 12 V Systems
- \* AN79-2 Stepping Motor Controller
- \* AN79-3 Dynamic Input Characteristics of VMOS Power Switch
- \* AN79-4 Driving VMOS Power FETs

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**Design Aids**

- \* DA74-1 Design Aid of the LD110/LD111 3½ Digit DVM Demonstrator Board
- \* DA76-1 The VMOS Power FET Audio Amplifier
- \* DA76-2 Design Aid of the LD130 ±3 Digit DVM Demonstrator Board
- DA76-3 Design Aid of the LD130 ±3 Digit Auto-Ranging DMM
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- \* DA77-4 Design Aid to Build a Piezoelectric Smoke Alarm Demonstrator with the SM110 Detector IC
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- \* DA78-2 Considerations for the Filtering of Analog Signals in DF331/DF332/DF334 CODEC Converter Applications
- DA78-4 Design Aid to Build a Smoke Detector with the SM110 IC

**Design Ideas**

- DI71-1 The FET Constant Current Source
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**Technical Articles**

- TA70-1 High Frequency Junction FET Characterisation and Application
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- \* TA73-1 Multiplexer Adds Efficiency To 32-Channel Telephone System
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- \* TA76-1 VMOS Power FETs in your next Broadband Driver
- \* TA76-2 A New Technology: Application of VMOS Power FETs for High Frequency Communications
- \* TA78-1 Designing with CODECs: Know your A's and μ's
- \* TA78-2 Designing a VMOS 250 Watt Off-Line Inverter

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**Catalogs**

- \_\_\_\_\_ Analog Switch Data Book
- \_\_\_\_\_ Analog Switches and Their Applications (\$4.00 charge)
- \_\_\_\_\_ DG300 Series Design Catalog
- \_\_\_\_\_ FET Data Book
- \_\_\_\_\_ LSI Design Catalog
- \_\_\_\_\_ Telecommunications Data Book
- \_\_\_\_\_ VMOS Power FET Design Catalog
- \_\_\_\_\_ OEM Pricing/Product Information Selector Guide

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**Reprints & Reports**

- \_\_\_\_\_ Designing a VMOS 250 Watt Off-Line Inverter. David C. Hoffman, *Power Con* 3/78
- \_\_\_\_\_ Designing with Codec's: Know your A's and  $\mu$ 's. Thomas J. Mroz, *EDN* 5/76
- \_\_\_\_\_ Log Data under  $\mu$  Control. Gary Grandbois, *Electronic Design* 5/76
- \_\_\_\_\_ Higher Power Ratings Extend VMOS FETs' Dominion. Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics* 6/78
- \_\_\_\_\_ Siliconix, Inc. Annual Report. 1979



# glossary of terms and abbreviations



1. Upper case letters indicate DC voltages and currents.
2. Lower case letters indicate AC voltages and currents.
3. Subscripts can refer to the terminals used in the measurements, i.e.,  $V_G$  = Gate Voltage; or simply help define the symbol, i.e.,  $t_f$  = Fall Time,  $t_r$  = Rise Time.
4. Triple subscripts are used for terminal references only. The first subscript is the object terminal. The second subscript is the common terminal. The third gives the condition of the remaining terminal(s). S = Short, 0 = open and X = neither open nor short (refer to the test conditions). Example:  $BV_{GSS}$  = Breakdown Voltage from gate to source with the drain shorted to the source.

|             |                                      |                   |   |
|-------------|--------------------------------------|-------------------|---|
| $b_{fg}$    | = Common-Gate Forward Susceptance    | $C_{rss}$         | = Common-Source Reverse Transfer Capacitance            |
| $b_{fs}$    | = Common-Source Forward Susceptance  | $C_{sb}$          | = Source-Body Capacitance                               |
| $b_{igs}$   | = Common-Gate Input Susceptance      | $C_{sd}$          | = Source-Drain Capacitance                              |
| $b_{iss}$   | = Common-Source Input Susceptance    | $C_{sgo}$         | = Source-Gate Capacitance                               |
| $b_{ogs}$   | = Common-Gate Output Susceptance     | $D$               | = Drain   |
| $b_{oss}$   | = Common-Source Output Susceptance   | $\bar{e}_N$       | = Equivalent Short Circuit Input Noise Voltage          |
| $b_{rg}$    | = Common-Gate Reverse Susceptance    | $f_m$             | = Figure of Merit                                       |
| $b_{rs}$    | = Common-Source Reverse Susceptance  | $G$               | = Gate  |
| $BV_{DGO}$  | = Drain-Gate Breakdown Voltage       | $g_{fg}$          | = Common-Gate Forward Transconductance                  |
| $BV_{DSS}$  | = Drain-Source Breakdown Voltage     | $g_{fs}$          | = Common-Source Forward Transconductance                |
| $BV_{SDX}$  | = Drain-Source Breakdown Voltage     | $g_{fso}$         | = Common-Source Forward Transconductance @ $V_{GS} = 0$ |
| $BV_{G1G2}$ | = Gate-Gate Breakdown Voltage        | $g_{fs1/g_{fs2}}$ | = Common-Source Forward Transconductance Ratio          |
| $BV_{G1SS}$ | = Gate 1 to Source Breakdown Voltage | $g_{ig}$          | = Common-Gate Input Conductance                         |
| $BV_{G2SS}$ | = Gate 2 to Source Breakdown Voltage | $g_{is}$          | = Common-Source Input Conductance                       |
| $BV_{GBS}$  | = Gate-Body Breakdown Voltage        | $g_{og}$          | = Common-Gate Output Conductance                        |
| $BV_{GSS}$  | = Gate-Source Breakdown Voltage      | $g_{os}$          | = Common-Source Output Conductance                      |
| $BV_{SDS}$  | = Source-Drain Breakdown Voltage     | $g_{oss}$         | = Common Source Output Conductance @ $V_{GS} = 0$       |
| $BV_{SGO}$  | = Source-Gate Breakdown Voltage      | $g_{os1-g_{os2}}$ | = Differential Output Conductance                       |
| $C_{db}$    | = Drain-Body Capacitance             | $G_{pg}$          | = Common-Gate Power Gain                                |
| $C_{dgo}$   | = Drain-Gate Capacitance             | $G_{ps}$          | = Common-Source Power Gain                              |
| $C_{gb}$    | = Gate-Body Capacitance              | $I_{D(off)}$      | = Drain Cutoff Current                                  |
| $C_{gd}$    | = Gate-Drain Capacitance             | $I_{D(on)}$       | = Drain ON Current                                      |
| $C_{gs}$    | = Gate-Source Capacitance            | $I_{DGO}$         | = Drain-Gate Leakage                                    |
| $C_{iss}$   | = Common-Source Input Capacitance    |                   |   |
| $C_{oss}$   | = Common-Source Output Capacitance   |                   |   |

## glossary of terms and abbreviations (cont'd)

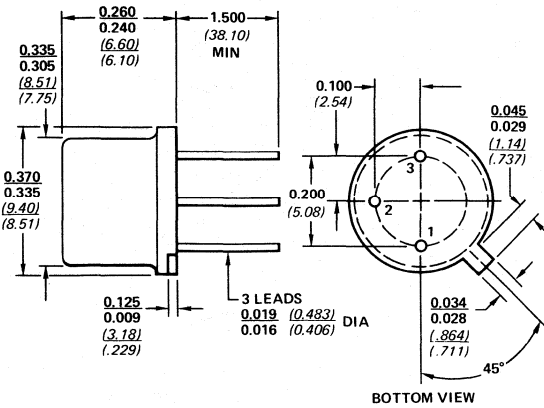
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|--|--|--|--|
| <b>I<sub>DSS</sub></b>                   | = Saturation Drain Current                 | <b>t<sub>d(on)</sub></b>                                     | = Turn-On Delay Time                                       |
| <b>I<sub>DSS1</sub>/I<sub>DSS2</sub></b> | = Saturation Drain Current Ratio           | <b>t<sub>f</sub></b>   | = Fall Time  |
| <b>I<sub>F</sub></b>                     | = Forward Current                          | <b>T<sub>j</sub></b>   | = Junction Temperature                                     |
| <b>I<sub>G</sub></b>                     | = Gate Operating Current                   | <b>t<sub>off</sub></b>                                       | = Turn-Off Time  |
| <b>I<sub>G1G2</sub></b>                  | = Gate to Gate Leakage Current             | <b>t<sub>on</sub></b>  | = Turn-On Time   |
| <b> I<sub>G1</sub>-I<sub>G2</sub> </b>   | = Differential Gate Operating Currents     | <b>T<sub>l</sub></b>   | = Lead Temperature   |
| <b>I<sub>GBS</sub></b>                   | = Gate to Body Leakage Current             | <b>t<sub>r</sub></b>   | = Rise Time  |
| <b>I<sub>G(f)</sub></b>                  | = Gate Forward Current                     | <b>T<sub>stg</sub></b>                                       | = Storage Temperature                                      |
| <b>I<sub>GSS</sub></b>                   | = Gate Reverse Current                     | <b>V<sub>B</sub></b>   | = Body Voltage   |
| <b>I<sub>G1SS</sub></b>                  | = Gate 1 to Source Leakage Current         | <b>V<sub>BB</sub></b>  | = Body Supply Voltage                                      |
| <b>I<sub>G2SS</sub></b>                  | = Gate 2 to Source Leakage Current         | <b>V<sub>D</sub></b>   | = Drain Voltage  |
| <b>I<sub>G1SSR</sub></b>                 | = Gate 1 to Source Reverse Leakage Current | <b>V<sub>DD</sub></b>  | = Drain Supply Voltage                                     |
| <b>I<sub>G2SSR</sub></b>                 | = Gate 2 to Source Reverse Leakage Current | <b>V<sub>DS(on)</sub></b>                                    | = Drain-Source ON Voltage                                  |
| <b><math>\bar{i}_n</math></b>            | = Equivalent Open-Circuit Noise Current    | <b>V<sub>G</sub></b>   | = Gate Voltage   |
| <b>I<sub>p</sub></b>                     | = Pinch-Off Current                        | <b>V<sub>GG</sub></b>  | = Gate Supply Voltage                                      |
| <b>NF</b>                                | = Noise Figure                             | <b>V<sub>GS</sub></b>  | = Gate-Source Voltage                                      |
| <b>P<sub>D</sub></b>                     | = Continuous Power Dissipation             | <b> V<sub>GS1</sub>-V<sub>GS2</sub> </b>                     | = Differential Gate-Source Voltage                         |
| <b>POV</b>                               | = Peak Operating Voltage                   | <b>ΔV<sub>GS</sub></b>                                       | = Differential Gate-Source Voltage                         |
| <b>r<sub>ds(on)</sub></b>                | = Drain-Source ON Resistance               | <b><math>\frac{\Delta V_{gs1}-V_{gs2} }{\Delta T}</math></b> | = Differential Gate-Source Voltage Change with Temperature |
| <b>r<sub>DS(on)</sub></b>                | = Static Drain-Source ON Resistance        | <b>V<sub>GS(f)</sub></b>                                     | = Gate-Source Forward Voltage                              |
| <b>Re (Y<sub>fg</sub>)</b>               | = Common-Gate Forward Transconductance     | <b>V<sub>GS(th)</sub></b>                                    | = Gate Threshold Voltage                                   |
| <b>Re (Y<sub>fs</sub>)</b>               | = Common-Source Forward Transconductance   | <b>V<sub>GS(off)</sub></b>                                   | = Gate Source Cutoff Voltage                               |
| <b>Re (Y<sub>ig</sub>)</b>               | = Common-Gate Input Conductance            | <b>V<sub>G1S(off)</sub></b>                                  | = Gate 1 to Source Cutoff Voltage                          |
| <b>Re (Y<sub>is</sub>)</b>               | = Common-Gate Output Conductance           | <b>V<sub>G2S(off)</sub></b>                                  | = Gate 2 to Source Cutoff Voltage                          |
| <b>Re (Y<sub>os</sub>)</b>               | = Common-Source Output Conductance         | <b>V<sub>S</sub></b>   | = Source Voltage   |
| <b>Re (Y<sub>rg</sub>)</b>               | = Common-Gate Reverse Transconductance     | <b>V<sub>SS</sub></b>  | = Source Supply Voltage                                    |
| <b>Re (Y<sub>rs</sub>)</b>               | = Common-Source Reverse Transconductance   | <b>Z<sub>d</sub></b>   | = Dynamic Impedance  |
| <b>r<sub>GS</sub></b>                    | = Common-Source Input Resistance           | <b>Z<sub>k</sub></b>   | = Knee AC Impedance  |
| <b>S</b>                                 | = Source                                   | <b>θ<sub>l</sub></b>   | = Current Temperature Coefficient                          |
| <b>t<sub>d</sub></b>                     | = Delay Time                               | <b>θ<sub>J-A</sub></b>                                       | = Junction to Ambient Thermal Resistance                   |
| <b>t<sub>d(off)</sub></b>                | = Turn-Off Delay Time                      | <b>θ<sub>J-C</sub></b>                                       | = Junction to Case Thermal Resistance                      |

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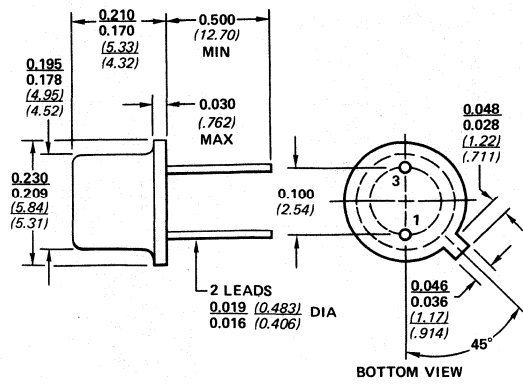
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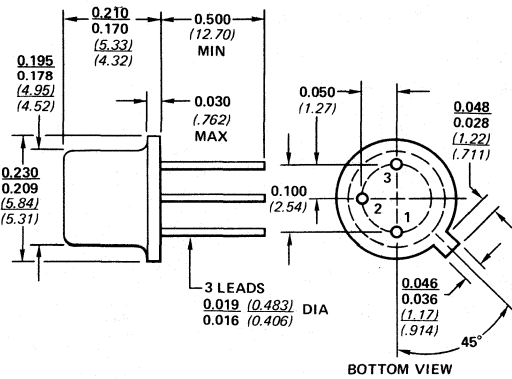
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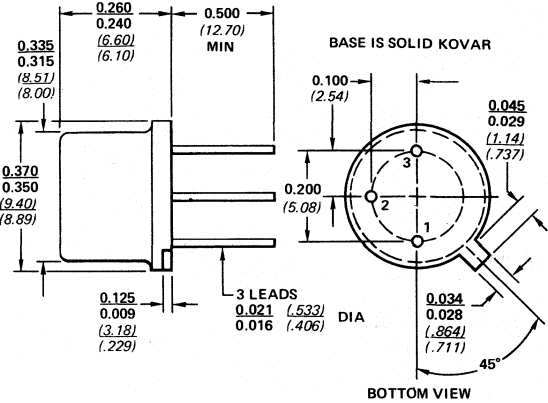
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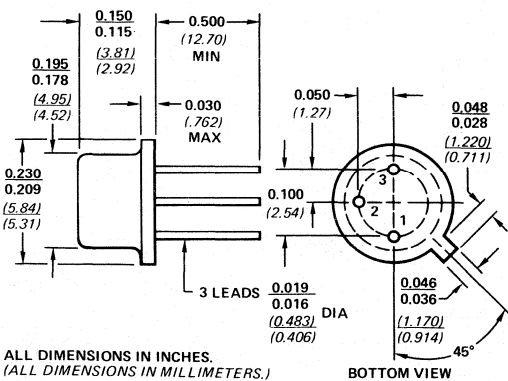
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(3 PIN)

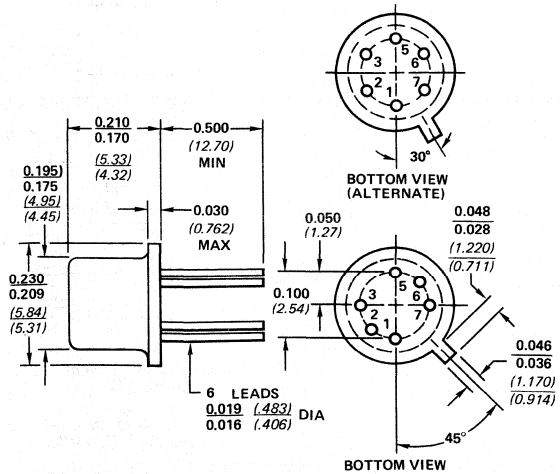


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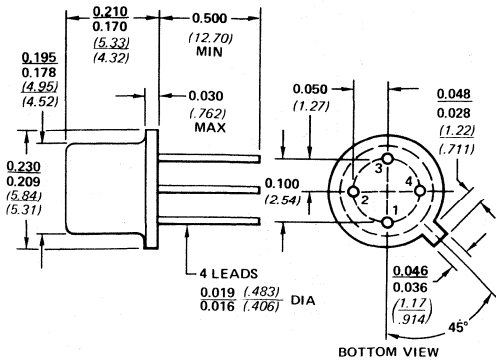
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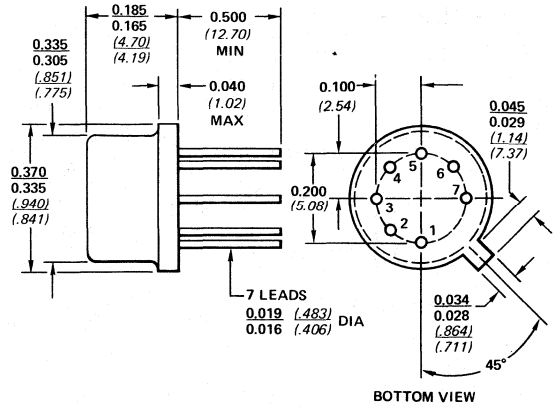


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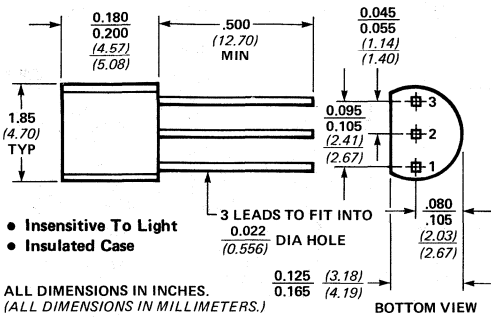
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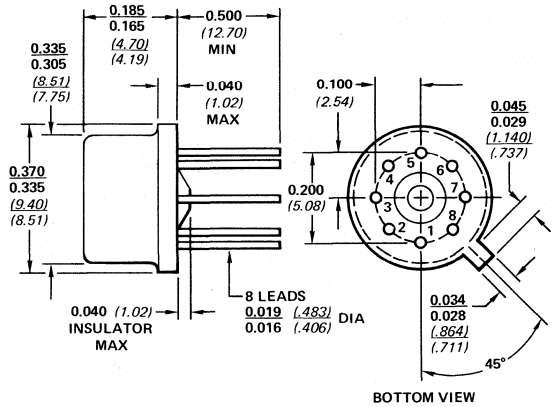
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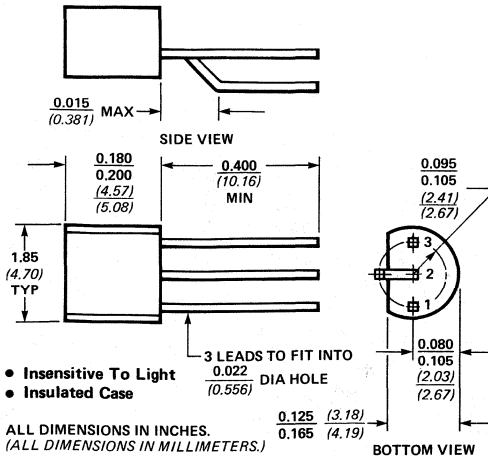
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- Insulated Case

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TO-92



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(317)844-8462  
Twx: 810-260-2631

**INDIANA, Fort Wayne (46804)**  
Rich Electronic Marketing  
3448 W. Taylor St.  
(219)432-5553  
Twx: 810-332-1404

**KANSAS, Shawnee Mission (66212)**  
BC Electronics  
P. O. Box 12485  
(913)888-6680  
Twx: 910-749-6414

**KANSAS, Wichita (67207)**  
BC Electronics  
5405 E. Kellogg, Suite 14  
(316)894-0051

**MARYLAND, Baltimore (21227)**  
Coulbourn DeGref, Inc.  
5205 East Drive  
(301)247-4646  
Twx: 710-236-9011

**MASSACHUSETTS, Reading (01867)**  
Kanan Associates  
100 Main Street  
(617)944-8484  
Twx: 910-393-6552

**MICHIGAN, Bloomfield Hills (48013)**  
Enco Marketing Inc.  
860 West Long Lake Road  
(313)642-0203  
Twx: 810-232-1669

**MINNESOTA, Minneapolis (55435)**  
KELCOM  
5200 West 73rd Street  
(612)835-0242  
Twx: 910-576-2740

**MISSOURI, Hazelwood (63042)**  
BC Electronics  
300 Brookes Dr., Suite 206  
(314)731-1255  
Twx: 910-762-0600

**NEW YORK, Syracuse (13206)**  
TI Electronics  
4054 New Court Ave.  
(315)463-8592  
Twx: 710-541-0554

**NEW YORK, Victor (14564)**  
TI Electronics  
2 E. Main St.  
(716)924-9101  
Twx: 510-254-8542

**NORTH CAROLINA, Cary (27511)**  
Montgomery Marketing  
P.O. B. 520, 1212 Lane Dr.  
(919)467-6319  
Twx: 510-920-0634

**OHIO, Dayton (45414)**  
Lyons Corporation  
4812 Frederick, Suite 101  
(513)278-0714

**OHIO, Highland Heights (44143)**  
Lyons Corporation  
6151 Wilson Mill Rd., Suite 101  
(216)461-8288

**PENNSYLVANIA, Erdenheim (19118)**  
GCM Associates  
1014 Bethlehem Place  
(215)233-4600  
Twx: 510-661-9170

**TENNESSEE, Jefferson City (37760)**  
Rep. Inc.  
P.O. B. 287  
(615)475-4105  
Twx: 810-570-4203

**TEXAS, Houston (77022)**  
Semiconductor Sales Associates  
4101 N. Freeway, Suite 202  
(713)661-0681

**TEXAS, Richardson (75080)**  
Semiconductor Sales Associates  
P.O. Box 2618  
(214)231-6181

**VIRGINIA, Charlottesville (22901)**  
Coulbourn DeGref, Inc.  
1616 Ingleswood Dr.  
(804)977-0031  
Twx: 710-236-9011

**WASHINGTON, Seattle (98107)**  
Blair Hirsch Co.  
4013 Leary Way NW  
(206)783-3423

**WISCONSIN, Milwaukee (53220)**  
JM Sales  
6522 W. Forest Home Ave.  
(414)546-0040  
Twx: 910-576-2778

## Canada

**ONTARIO, Etobicoke (M9C 1E7)**  
R.F.O. Ltd.  
385 The West Mall, Suite 209  
(416)528-1445  
Twx: 810-492-2540

**QUEBEC, (H9G 2H8)**  
R.F.O. Ltd.  
P.O. Box 213, Dollard Des Ormeaux  
(514)694-5724  
Tlx: 05821762

## U.S. Chip Distributor

**FLORIDA, ORLANDO (32807)**  
Chip Supply Inc.  
1607 Forsyth Road  
(305)275-3610  
Tlx: 810-850-0103



## International Sales Offices

### European Sales Offices

**FRANCE**

Siliconix S.A.R.L.  
7072 Avenue du General de Gaulle  
Echat 660  
94022 Creteil Cedex  
Tel: 377 12 51  
Tlx: Silicon 230389F

**WEST GERMANY**

Siliconix GmbH  
Postfach 1340  
Johannesstrasse 27  
D-7024 Pfriderstadt 1  
Tel: (0711) 702066  
Tlx: 7 255 553

**UNITED KINGDOM**

Siliconix Ltd.  
Brook House  
Northbrook Street  
Newbury, Berks  
RG13 1AH  
Tel: (0635) 64846  
Tlx: 849357

Siliconix Ltd.  
Morrison, Swansea  
United Kingdom SA6 6NE  
Tel: (0792) 74681  
Tlx: 48197

**HONG KONG**

Siliconix (H. K.) Ltd.  
5/6/7H Floors  
Liven House  
61-63 King Yip Street, Kwun Tong  
Kowloon, Hong Kong  
Tel: 3-427 151  
Tlx: 74449 SILX HX

**JAPAN**

Siliconix DISC Japan Branch  
101 Daigo Tanaka Bldg  
4-4 Iidabashi, 3-Chome  
Chiyoda-Ku, Tokyo, Japan 102  
Tel: 03-262-4777  
Tlx: J23411

**TAIWAN**

Siliconix (Taiwan) Ltd.  
Nantze Export Processing Zone  
Kaohsiung  
Tel: 362010, 362019  
Tlx: 785 712 35

### European Distributors/Representatives

**AUSTRIA**

Ing. Ernst Steiner  
A-1130 Wien  
Geylinggasse 16  
Tel: 222/822674  
Tlx: 136026

**BELGIUM**

Ritro Electronics BV  
172 Plantin en Moretuslei  
B-2000 Antwerpen B  
Tel: 031-353272  
Tlx: 33637

**DENMARK**

Diiz Schweitzer A.S.  
Valiensbaekvej 51  
DK-2600 Glostrup  
Tel: (01) 45 30 44  
Tlx: 33257

**FINLAND**

Oy Finnip AB  
Teollisuuskie 7 P.O. B. 34  
SF-02700 Kauniainen  
Tel: 90 502255  
Tlx: 12-3129

**FRANCE**

Aimax  
46 Rue de L'Aubepine  
92160 Antony  
Tel: 666 21 12  
Tlx: 250067

**Alrodas**

40 Rue Villon  
69008 Lyon  
Tel: (78) 695952  
Tlx: 330174

**Aquitaine Composants**

30 Rue Denfert Rochereau  
33400 Talence  
Tel: (56) 80 24 70

**A. Baltzinger**

18-26 Route du General de Gaulle  
67300 Schiltigheim  
Tel: (88) 331852  
Tlx: 879952F

**Ouest Composants**

5 rue Lesage  
3500 Rennes  
Tel: (99) 360058  
Tlx: 730004

**Sanelec Electronique**

7 Rue de la Couture  
Z. 1, de la Pilaterie  
59700 Marcq-en-Baroeuil  
Tel: (20) 98 92 13  
Tlx: 160 143F

**SCAIB**

80 Rue d'Arceuil  
Z. Silic 137  
Rungis, 94523 Cedex  
Tel: 687 23 13  
Tlx: 204 674F

**GERMANY**

Ditronic GmbH  
IM Asemwald 48  
7000 Stuttgart 70  
Tel: (0711) 724844  
Tlx: 07 255638

**Ing. Buro K.H. Dreyer**

Fiensburger Strasse 3  
2380 Schleswig  
Tel: (04621) 23121  
Tlx: 02-21334

**EBV Elektronik GmbH**

Gabriel-Max Strasse 72  
8000 Munchen 90  
Tel: (089) 644055  
Tlx: 05-24535

**INDIA**

Zenith Electronics  
541 Panchratna  
Mama Parmanand Marg  
Bombay 400004  
Tel: 384214  
Tlx: 011-3152

**ISRAEL**

Talviton Electronics, Ltd.  
9 Billmore St.  
Tel Aviv  
Tel: 44 45 72  
Tlx: Vitko 33400

**EBV Elektronik GmbH**

Alexanderstrasse 42  
7000 Stuttgart 1  
Tel: (0711) 247481  
Tlx: 07-22271

**EBV Elektronik GmbH**

Oststrasse 129  
4000 Dusseldorf  
Tel: (0211) 848467  
Tlx: 08-587267

**EBV Elektronik GmbH**

In der Meinenweg 9A  
3006 Burgwedel 1/Hannover  
Tel: (05139) 4570  
Tlx: 09-23694

**EBV Elektronik GmbH**

Myllusstrasse 54  
6000 Frankfurt 1  
Tel: 0611/7204 167  
Tlx: 04-15590

**iw-electronic**

Klaus Vespermann Kg  
Bachstrasse 30a  
6380 Bad Homburg V.D.H.  
Tel: (06172) 23061-5  
Tlx: 0415864

**Ultronik GmbH**

Munchner Strasse 6  
6031 Operating Seefeld  
Tel: (08152) 7774  
Tlx: 05-27832

**Unitronic Schlueter GmbH u. Co. KG**

Manskestrasse 29  
3160 Lerbhe  
Tel: (05132) 53001  
Tlx: 09-22084

**GREECE**

General Electronics, Ltd.  
209 Thevon St.  
Nikaia, Piraeus 77  
Tel: 361-8145  
Tlx: 212949 GELT GR

**JAPAN**

Teijin Advanced Products Corp.  
131 Uchisawa-cho, 2-Chrome  
Chiyoda-Ku, Tokyo, 100  
Tel: (03) 506-4670  
Tlx: J-23548

**KOREA**

Yeonil & Co. Ltd.  
KPO Box 1112  
Seoul  
Tel: 65-0461  
Tlx: K24123

**MEXICO**

Mexel  
Tlacoquemacatl No. 139-401  
Mexico 12, D.F.  
Tel: 575-78-68, y 575-79-24  
Tlx: MEXEL 0177 3197

**HOLLAND**

Patron BV  
P.O. Box 75  
1243ZH S-Graveland NL.  
Tel: 035-60834  
Tlx: 4 3943

**Ritro Electronics BV**

Getieweg 22  
Postbox 123  
3770 AC Barneveld NL  
Tel: 03420-5041  
Tlx: 40553

**ITALY**

Adelys  
Via Domenichino 12  
20149 Milano  
Tel: (02) 4985051  
Tlx: 33 2423

**Dott. Ing. Giuseppe DeMico**

Via Manzoni 31  
20121 Milano  
Tel: 653131  
Tlx: (02) 312035

**NORWAY**

A. S. Kjell Bakke  
Postbox 143  
2010 Strommen, Nygatan 48  
Tel: (02) 71 18-72 71 53 50  
Tlx: 19407

**SPAIN**

ATAIO  
Enrique Larreta 10Y12  
Madrid 16  
Tel: 733 05 62 or 733 37 00  
Tlx: 27249

**SWEDEN**

Komponentbiolaget NAXAB  
Box 4115  
S-17104 Solna  
Tel: 08-885140  
Tlx: 17912 KOMP

**NEW ZEALAND**

Electronic Component Services  
Div. of Airspares NZ Ltd.  
P. O. B. 1046, Palmerston North  
Tel: 77 407  
Tlx: NZ3786

**SOUTH AFRICA**

Electrolink (Pty) Ltd.  
P.O. Box 1020  
Capetown  
Tel: 457656/7  
Tlx: 57-7320

**TAIWAN**

Don Business Corp.  
No. 265 Chang Chung Rd.  
Taipei  
Tel: 571-2911  
Cable: "DONBC" TAIPEI  
Tlx: 25641 DONBC

**SWITZERLAND**

Kontron Electronic AG  
Bernstrasse Sud 169  
8048 Zurich  
Tel: 01-62-82-82  
Tlx: 58836

**UNITED KINGDOM**

Dage Eurosem Ltd  
Haywood House  
High Street  
Pinner  
MIDDLESEX  
Tel: 01-888-0028  
Tlx: 24506

**Limbreg Electronics Ltd**

Hillend Industrial Estate  
Dunfermline  
SCOTLAND  
Tel: (0383) 823222  
Tlx: 727438

**Macro Marketing Ltd**

396 Bath Road  
Slough, Berks  
Tel: (06286) 4422  
Tlx: 847945

**Semiconductor Specialists (UK) Ltd**

Premier House, Fairfield Road  
Yewley, West Droyton  
MIDDLESEX  
Tel: (08954) 45522  
Tlx: 21958

**Woolley Components Ltd**

Tudor Road, Broadheath Ind. Est.  
Aittrincham, CHESHIRE WA145RZ  
Tel: (061941) 1911  
Tlx: 669735

**YUGOSLAVIA**

Belram S.A.  
83 Avenue des Mimosas  
1150 Brussels, Belgium  
Tel: (061941) 1911  
Tlx: 21790

### Other International Distributors/Representatives

**ARGENTINA**

Corte & Cia. S.R.L.  
San Juan 1301  
Buenos Aires  
Tel: 27-0101  
Tlx: 012-1992

**EMSE Electronica S.A.**

Div. Semiconductores  
Ayacucho No. 311  
1025 Buenos Aires  
Tel: 40-2071

**AUSTRALIA**

STC Cannon Components PTY LTD  
248 Wickham Road - P.O. Box 62  
Moorabbin, Victoria 3189, Australia  
Tel: Melbourne 95-1566  
Tlx: Melbourne AA 30877  
Cable: CANNONLEC - MELBOURNE

**BRAZIL**

Cosete LTDA  
Rua da Consolacao,  
867-CJ 22  
01310 Sao Paulo  
Tel: 257-3535 or 258-4325  
Tlx: 1130869 CSEL-BR

**INDIA**

Zenith Electronics  
541 Panchratna  
Mama Parmanand Marg  
Bombay 400004  
Tel: 384214  
Tlx: 011-3152

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9 Billmore St.  
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Tlx: Vitko 33400

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Chiyoda-Ku, Tokyo, 100  
Tel: (03) 506-4670  
Tlx: J-23548

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Yeonil & Co. Ltd.  
KPO Box 1112  
Seoul  
Tel: 65-0461  
Tlx: K24123

**MEXICO**

Mexel  
Tlacoquemacatl No. 139-401  
Mexico 12, D.F.  
Tel: 575-78-68, y 575-79-24  
Tlx: MEXEL 0177 3197

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P. O. B. 1046, Palmerston North  
Tel: 77 407  
Tlx: NZ3786

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Capetown  
Tel: 457656/7  
Tlx: 57-7320

**TAIWAN**

Don Business Corp.  
No. 265 Chang Chung Rd.  
Taipei  
Tel: 571-2911  
Cable: "DONBC" TAIPEI  
Tlx: 25641 DONBC

**VENEZUELA**

IBARS & Cia. S.A.  
Centro Ciudad Comercial Tamanaco  
Nivel C2, Local 53-C03  
Chacao-Caracas  
Apartado 68493  
Caracas 106  
Tel: 828053  
Tlx: 21795 Teletipos a/c IBARS  
Cables: IBARS-CARACAS







## MANUFACTURING FACILITIES

### UNITED STATES

Siliconix Incorporated  
2201 Laurelwood Rd.  
Santa Clara, CA 95054  
Tel: (408) 246-8000  
Tlx: 910-338-0227

### UNITED KINGDOM

Siliconix Ltd.  
Morrison SWANSEA SA6 6NE  
Tel: (0792) 74681  
Tlx: 48197

### HONG KONG

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5/6/7th Floors  
Liven House  
61-63, King Yip Street  
Kwun Tong, Kowloon  
Hong Kong  
Tel: 3-427151  
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### TAIWAN

Siliconix (Taiwan) Ltd.  
Nantze Export Processing Zone  
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Tlx: 78571235

